



## Using ACKS Mode To Control Converter Sampling Rate

ACKS (Auto Clock Setting) mode can be utilized to change converter sample rates from normal speed mode (22kHz to 54kHz), double speed mode (54kHz to 108kHz), and quad speed mode (108kHz to 216kHz) by scaling the internal delta-sigma modulator rates and digital filter coefficients appropriately without the need for register or pin changes. ACKS mode allows the design to control the speed operation mode of the converter by the clocks that are provided to the device. In each AKM datasheet, there is a table that shows the accepted clock frequency to run when using ACKS – examples are shown in the tables below.

ACKS mode greatly simplifies a design by eliminating the need for a user interface to set converter sample rates that match the incoming sample rate. The sample rate detection circuit has been integrated to ensure the accuracy of the auto setting mode. No microcontroller, FPGA, or manual switches are required to change the converter sampling rate, simplifying the design and shortening time-to-market. The product's end user has a simpler set-up, less to learn, and the converters are guaranteed to be in the right sampling mode to get optimal performance for every sample rate.

Table 1 illustrates that MCKO1 and MCKO2 are outputs that will drive the ADC and DAC with the proper master clock enabled by ACKS mode.

Mode	MCKO1	MCKO2	Sampling Frequency Range
Normal Speed	512fs	256fs	22kHz to 48kHz
Double Speed	256fs	128fs	64kHz to 96kHz
Quad Speed	128fs	64fs	128kHz to 216kHz

**Table 1. AK4115 Master Clock Frequency Select (Master Clock Auto Setting Mode)**

Table 2 illustrates the AK4396 MCLK input requirements to enable the use of ACKS mode. The MCLK for the AK4396 should be connected to MCKO1 of the AK4115. N/A means that this MCLK frequency is not supported.

LRCK	MCLK (MHz)							Sampling Speed
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32kHz	N/A	N/A	N/A	N/A	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	
48kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

**Table 2. System Clock Example for AK4396 (Manual Setting Mode in Parallel Control Mode)**

Table 3 illustrates the MCLK input frequency requirements of the AK5359 ADC for each mode when MCLK is connected to MCKO1 of the AK4115.

Fs (kHz)	MCLK (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
32	N/A	N/A	8.1920	12.2880	16.3840	24.5760
44.1	N/A	N/A	11.2896	16.9344	22.5792	33.8688
48	N/A	N/A	12.2880	18.4320	24.5760	36.8640
96	N/A	N/A	24.5760	36.8640	N/A	N/A
192	24.5760	36.8640	N/A	N/A	N/A	N/A

**Table 3. System Clock Example for AK5359**

Tables 4 and 5 illustrate the MCLK input frequency for the AK5494A in each mode. This should be connected to MCKO2 of the AK4115. Although the AK5394A does not support ACKS mode, by simple control of the sampling speed selection pins it can be connected to an ACKS-enabled receiver.

Sampling Speed	Normal	Double	Quad	
	DFS0	L	H	L
	DFS1	L	L	H
LRCK (fs)	~54kHz	~108kHz	~216kHz	
SCLK (Slave Mode)	~128fs	~64fs	~64fs	
SCLK (Master Mode)	128fs	64fs	64fs	
MCLK	256fs	128fs	64fs	

**Table 4. System Clocks for AK5394A**

LRCK (fs)	MCLK(MHz)	SCLK (MHz)
32kHz	8.1920	~4.0960
44.1kHz	11.2896	~5.6448
48kHz	12.2880	~6.1440
96kHz	12.2880	~6.1440
192kHz	12.2880	~12.2880

**Table 5. System Clock Frequency for AK5394A**