

Applications Note

AK4528 creates “perfect” brick wall filter.

Brick wall filters are desirable in a number of audio, instrumentation and data acquisition applications. Creating these filters in the analog domain presents many cost and implementation challenges, especially when a number of precisely matched filters are required. A high-performance delta-sigma audio codec or a discrete analog-to-digital/digital-to-analog converter (ADC/DAC) combination can be used to create a near-perfect brick wall filter that has many appealing features.

Theory of Operation

As Figure 1 shows, the internal structure of the codec consists of both an analog-to-digital converter and a DAC. In this example the AKM AK4528 high-performance codec is used. This codec features a signal-to-noise ratio of 110dB on the DAC and a 108dB SNR on the ADC, providing outstanding performance and signal integrity. Creating the brickwall filter with this part is simple. The analog signal to be filtered is fed into the codec’s input.

The ADC’s digital output is then wired directly to the DAC’s digital input (SDATA OUT to SDATA IN). The DACS’s analog output then provides the filtered signal. The delta-sigma converter’s digital filters provide the characteristic brickwall filter. The filter’s passband is calculated as being a –3dB corner at $0.454 * f_s$.

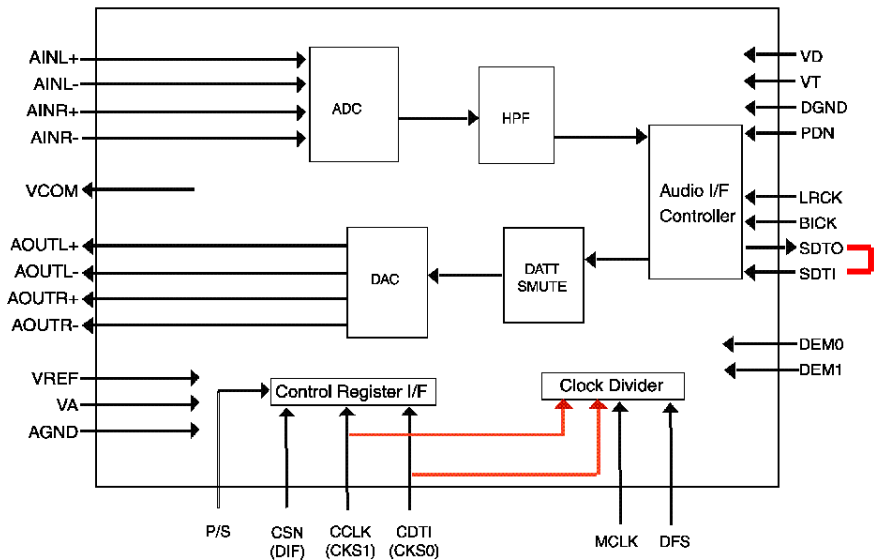


Figure 1 - AK4528 Codec Internal Architecture. Connect SDTO to SDTI to create the filter.

While the actual architecture of these digital filters is a trade secret, the performance is listed as –80dB on the A/D and –75dB on the DAC. The design of these digital filters is such that they scale with sampling frequency (MCLK). This ensures that the 2x Nyquist performance criteria are met. For example, when the sample frequency f_s is set to 48KHz, the digital filters begin to roll off at 21.8KHz ($0.454 * f_s$), thereby providing a 24KHz frequency response while eliminating any aliasing noise above this frequency. This 24KHz bandwidth would be inappropriate should f_s be changed to 96KHz, as it would limit the frequency response of the sample

operation to 24KHz when the correct value should be 48KHz. From this we can see that the digital filters scale with f_s , creating a convenient mechanism for controller the digital filter's characteristics. In summary, change the cut-off frequency of the filter by changing the frequency of the sample clock. The internal filters will adjust accordingly.

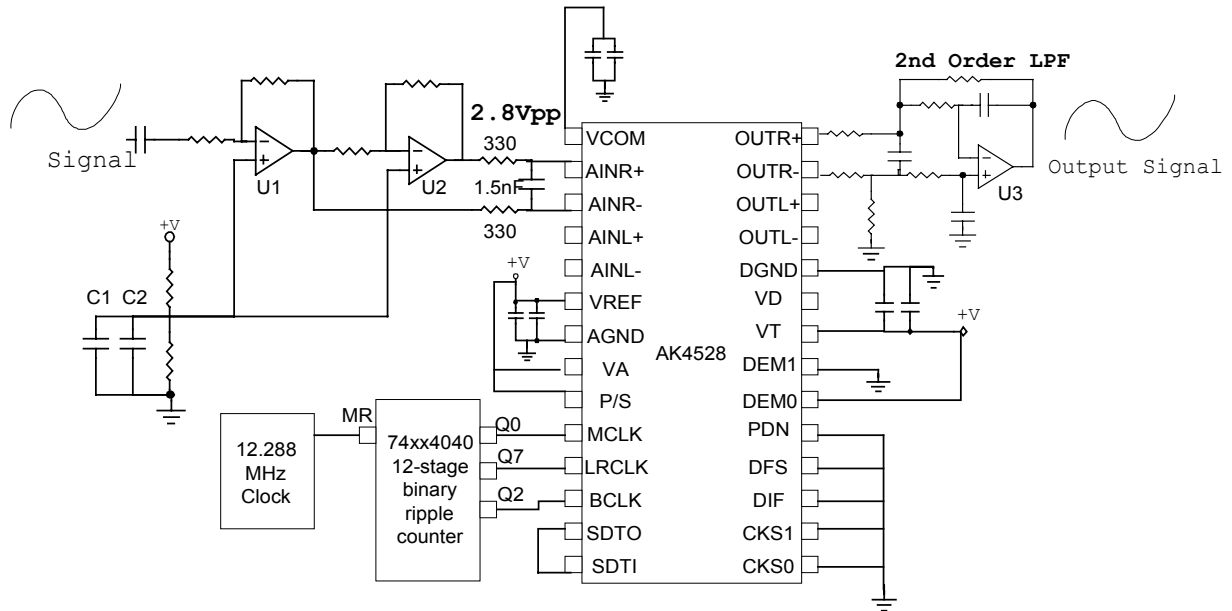


Figure 2 - Schematic for AK4528 used as a brick wall filter

Circuit Description

Figure 2 shows the schematic for this design. This figure shows the AK4528 set up as a brickwall filter with a 24KHz cutoff and 48KHz sample rate ($f_s = 12.288\text{MHz}/256$). The AK 4528 has a pair of differential inputs, maximizing Common Mode Rejection Ratio (CMRR). If you do not have a differential signal, U1 and U2 are used to turn a single-ended input into a differential input (AINR+, AINR-). If two input channels are required, duplicate this input circuit for AINL+ and AINL-. A 321.5KHz input filter created by the 330-ohm resistors and 1.5nF capacitor completes the input circuit and reduces high-frequency input noise. The only requirement for this input filter is to remove a 6MHz frequency component that may couple in from planet Hemorrhoid.

The output circuit consists of a 2nd order filter (U3) and removes the artifacts created by the internal 6MHz delta-sigma modulator. Since these frequencies are far above the sample frequencies, the slope of this filter is not critical.

The clock circuit works in conjunction with the DFS, DIF, CKS1 and CKS0 pins to select the internal sample frequency via the on-board clock dividers. This allows the AK4528 to be used without an external CPU. The sample schematic is set for a 48KHz sample rate, (24KHz filter cutoff) so the 12.288MHz MCLK requires a divisor of 256. The CKS0,

CKS1 and DFS pins are strapped to reflect this, as shown in Figure 3. In this circuit a 74HC4040 is used to provide the MCLK, BCLK (MCLK/4) and LRCLK (MCLK/256).

CKS1	CKS0	MCLK Normal Speed (DFS pin=L)	MCLK High Speed (DFS pin=H)
0	0	256fs	N/A
0	1	512fs	256fs
1	0	384fs	N/A
1	1	1024fs	512fs

Figure 3 - Pin settings for clock frequencies

Decoupling capacitors are used for various supply and bias voltages. The bypass capacitor circuit consisting of C1 and C2 is duplicated for Vcc, Vcom and Vref and the Bias point. This capacitor pair has one small (0.1uF typ.) and one large (10uF typ.) in parallel. Proper filtering of high and low frequency noise on the power supply ensures good THD performance.

System Benefits

This design is very simple and compact, the performance is predictable, reproducible and temperature independent. The left-right channel performance is perfectly matched and is always in phase. Using a high-performance 24-bit, 108KHz audio codec like the AK4528 provides a filter range from 15Hz to 54KHz with -80dB of attenuation. With the addition of a microprocessor for register control of the AK4528, the lowpass filter can become a bandpass filter with performance all the way down to DC levels.

One of the appealing features of this design is the steep filter slope. Designing such a filter in the analog domain is very expensive from both a design and a parts count point of view. Another benefit in this design is that there is no temperature drift associated with this filter, as there would be with an analog filter. Creating a bank of identical performance filters is now within the realms of affordability and practical implementation, important considerations in multi-channel audio and data acquisition. Using the approach outlined, channels can be perfectly matched without inducing phase shift.

The design is not without compromise. There is a slight delay caused by the conversion steps ($31 \times 1/f_s$). At a 48KHz sample rate the delay is typically about 0.6 milliseconds. Also an analog filter (U3) is still required to remove the high frequency aliasing created by the delta-sigma conversion process. However it is a fairly simple 2- or 3-pole filter whose performance is not overly critical.

Performance

Analog vs. Digital Filter

The following charts compare the performance of AKM's AK4528 codec wired as a digital filter to the performance of a 7th order Elliptical filter. Both filters are set to have a 20KHz pass band. The blue line shows the amplitude vs. frequency plot of the analog filter. The green line shows the amplitude vs. frequency plot of the digital filter using the AKM codec. The digital filter achieves a sharp roll off and great attenuation. One interesting fact that is not immediately apparent from the graph is that the digital filter was swept in stereo. The two channels out of the CODEC are both shown but because of the identical performance between the channels the differences cannot be distinguished.

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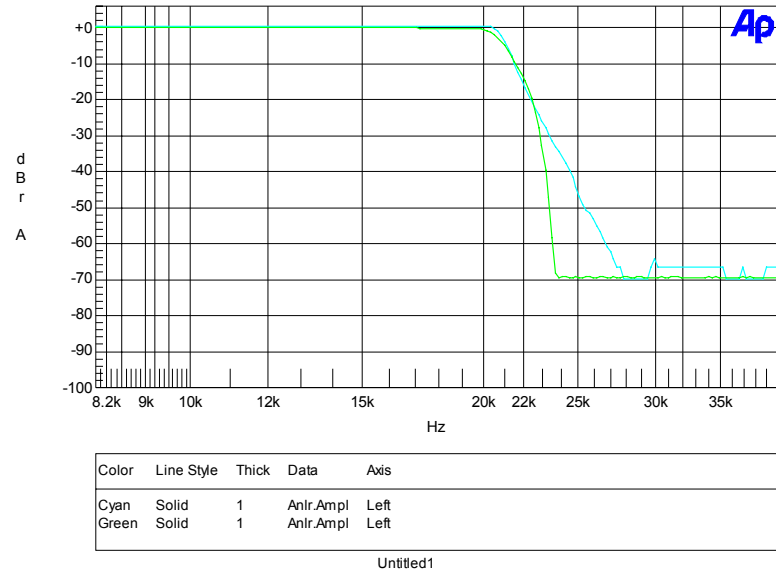


Figure 4 - Digital vs. Analog filter performance

Performance at various frequencies

Corners band pass – Figure 3 shows the filter characteristics at different sample clock settings. Starting with a 100KHz sample clock (108KHz being the maximum for the AK4528) there is a 50KHz pass band all the way to having the sample clock run at 16KHz only allowing an 8KHz pass band. This plot also shows the noise shaping that is inherent in delta sigma converters. This shaping is the rise in noise at higher frequencies outside the filter corner and outside the pass band. A simple 2- or 3-pole analog filter on the output of the CODEC can eliminate this shaping. Even though this analog filter will drift with temperature, its performance is not critical to the performance of the digital brickwall filter, since it is only eliminating the rise in noise at higher frequencies. Since we have eliminated temperature drift inherent in discrete analog

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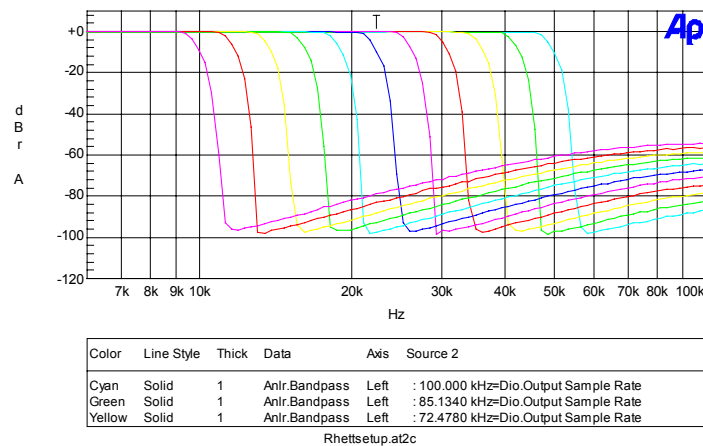


Figure 5 - Filter curves for various Fs.

circuits from the critical portion of the design, it is possible to match as many channels as required.

Filter corners – Taking the bandpass filter off around the input signal we see the flat noise floor after the attenuation. This attenuation level can be improved by adding the second or third order filter stage to the output of the CODEC. This also shows the introduction of the Alias. Converting the analog signal to digital creates this.

Modifications

This circuit can also filter signals all the way down to DC if the input capacitor is removed and the on-board high-pass filter of the AK4528 is disabled. This would require a microprocessor with I2C interface to change the value of the HPF register in the AK4528.

Balanced/differential inputs and outputs are also supported on the AK4538. This modification would require a removal of the input op amps and the addition of coupling capacitors on the AINL+ and AINL- inputs. The input and output filters would still be required. Using balanced inputs would improve Common Mode Rejection Response (CMRR) and provide an extra 3dB of performance.

The codec as a digital filter has some compelling cost and performance advantages and is a useful addition to any designer's toolbox.

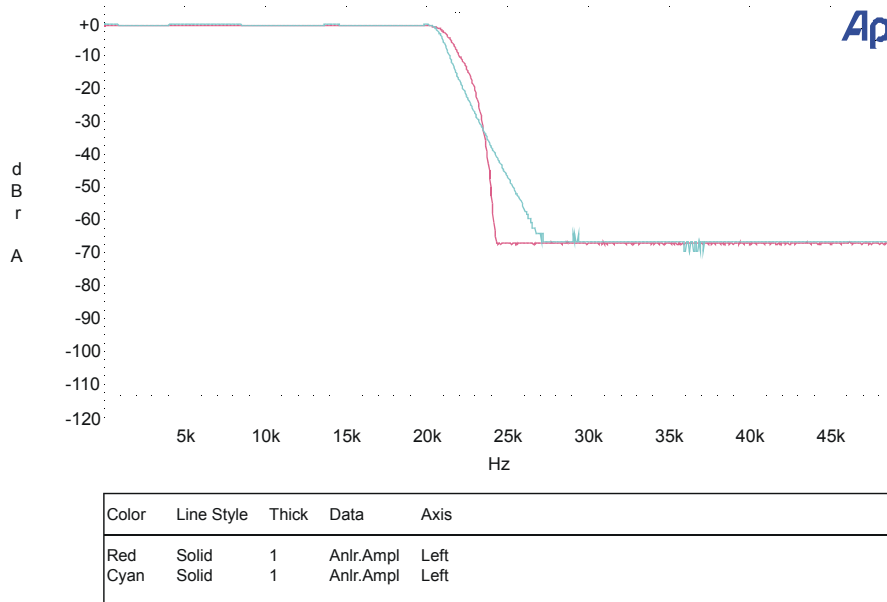


Figure 6

A-D VIEW WAVEFORM.at2c