

Synchronizing Multiple A/D Converters

Synchronizing multiple A/D converters in a system is a common issue that must be addressed to ensure that all channels are sampled simultaneously. A/D converters from AKM have fixed internal calibration timing, allowing for exact synchronization of sampling between multiple devices (this also applies to AKM CODEC's). It is essential to be certain that all A/D converters in the system initiate calibration at the same time.

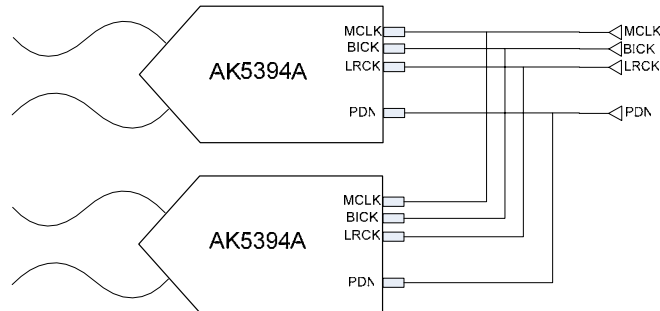


Figure 1. Multiple A/D converter system with common clocks

The A/D converters start calibration on the initial rising edge of the master clock after the device is taken out of reset by the PDN pin. The PDN assertion should be triggered on the falling edge of the master clock to ensure that all A/D converters in the system initiate calibration on the same rising edge of the master clock.

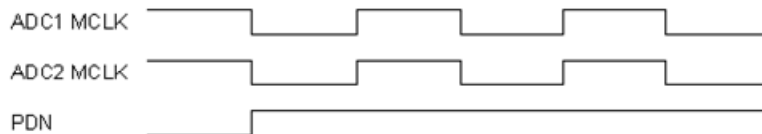


Figure 2. PDN assertion triggered by falling edge of MCLK

If the PDN assertion is not triggered on the falling edge of the master clock, the A/D converters may not initiate calibration simultaneously, and sampling may be asynchronous among the different A/D converters.

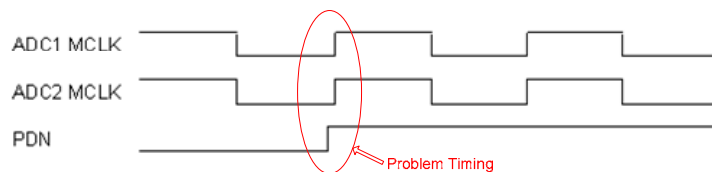


Figure 3. PDN assertion triggered after falling edge of MCLK