

## Automatic Reset Circuit

AKM converters require a reset signal after power-on, and when the audio clocks have been interrupted. This is usually executed by an external controller. If there are no pins available on the external controller to provide a dedicated reset signal to the AKM converter, a simple circuit can provide the reset signal for either power-on or interrupted clocks. For this Tech Tip, the AK4384 will be used as the example device, but reset characteristics are similar for all AKM converters. Reset is initiated by taking the PDN pin low (<math><V\_{IL}</math>) for at least 150ns.

### Power-on reset

Figure one illustrates a simple power-on reset circuit. If the master clock (MCLK) is always present before the converter is powered up, this circuit may be used. It may also be used when MCLK is present before the RC time constant allows the PDN threshold voltage to reach  $V_{IL}$  (0.8V). In this example,  $V_{IL}$  will be reached in approximately 2ms.

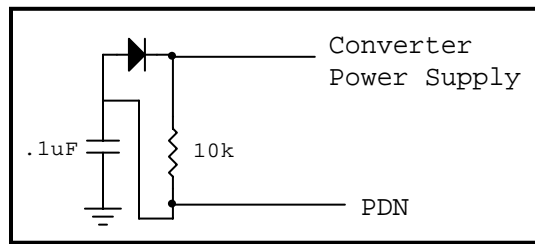


Figure 1

### MCLK reset

If power is applied, but MCLK is stopped, the converter must be reset. An example of an MCLK-based reset circuit is shown in Figure 2. The inverters connected to MCLK are used as buffers, and are only required if the drive capability of MCLK is load-dependent. The two inverters driving PDN are used to buffer the clock, since the output of the RC circuit will have a charge and discharge curve characteristic. Schmitt trigger buffers may also be used to eliminate uncertainty caused by metastable output states. Both sets of buffers are optional, depending upon system conditions and performance requirements.

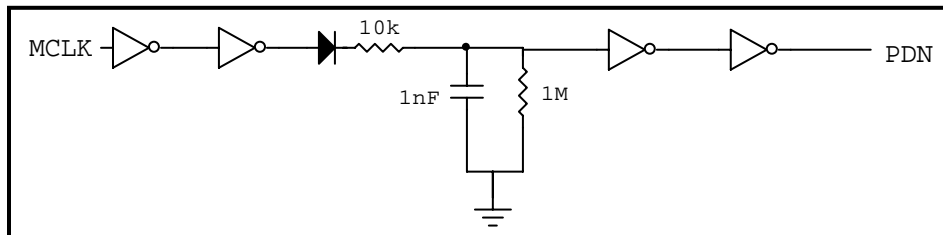


Figure 2

Figure 3 illustrates a complete reset circuit that can be used either on power-up or when MCLK is stopped. Use this circuit when there is a possibility of power and MCLK cycling asynchronously. The NAND gate is a 74LS132, selected for the Schmitt trigger output, which negates metastable clock states.

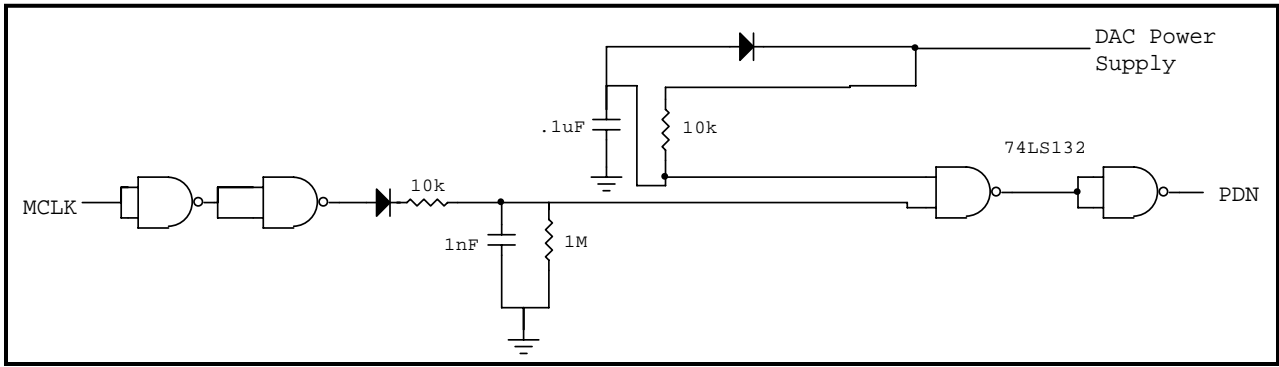


Figure 3