AK2303LV

Dual PCM CODEC for PBX Analog Line Card

GENERAL DESCRIPTION

AK2303LV is a 3.3V dual PCM CODEC-Filter most suitable for analog line card of PBX switch.

CODEC-Filter is compliant with G711/G712 recommendations.

It includes Selectable A-law/u-law function, Internal Gain Adjustment from +6dB to –18dB by 1dB step control. All of these functions are controlled by the internal register accessed through the serial interface. Additionally, channel mute and A-law/u-law selection is controlled by the hard pin.

PCM interface of AK2303LV supports Long Frame, Short Frame clock formats and GCI format. 4.096MHz, 2.048MHz bit clock input is available for PCM interface.

FEATURE

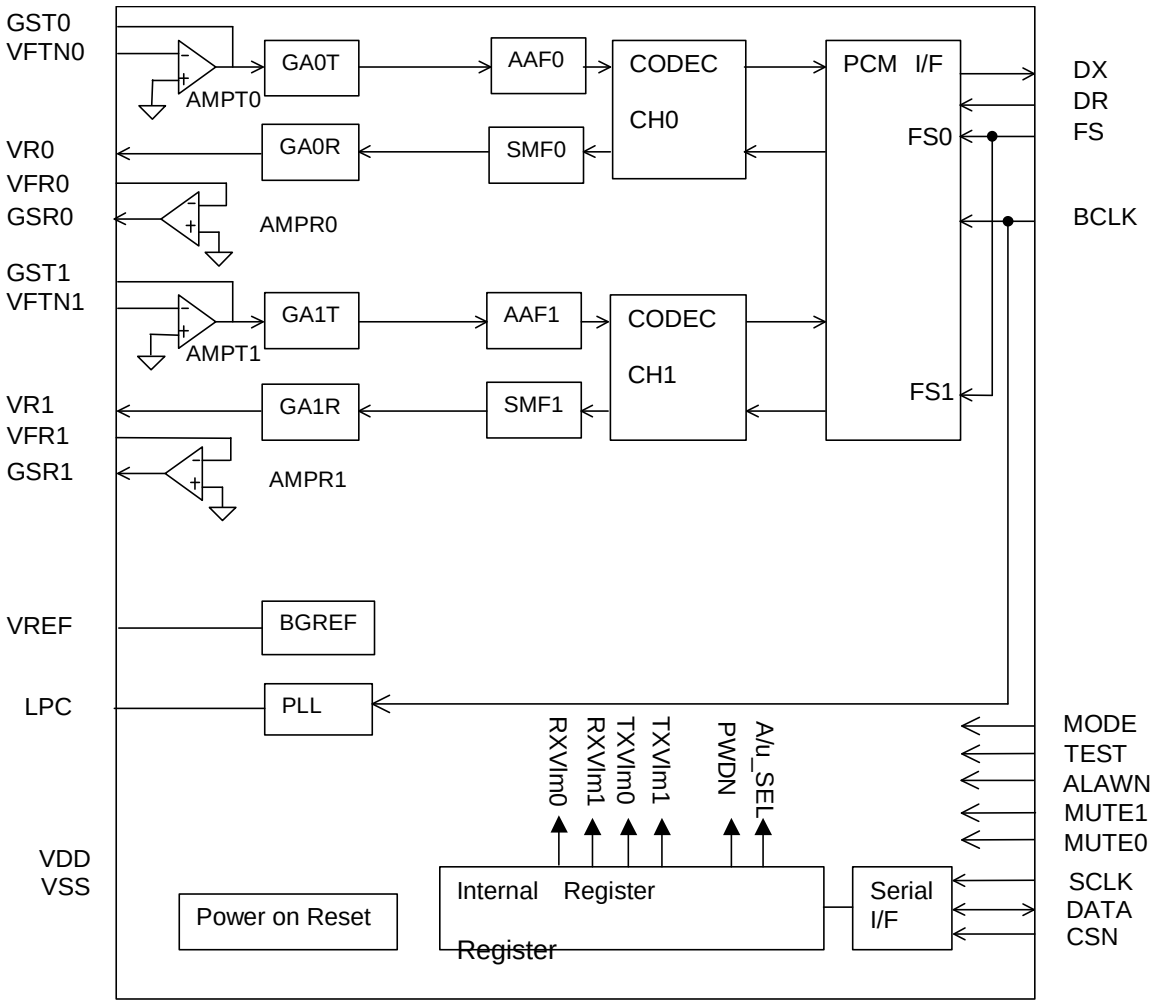
- Dual PCM CODEC and Filtering systems for PBX switch
- Independent functions on each channel Controlled by the internal register or hard pin
  - Power Down Mode (Register setting)
  - Mute (Hard pin, register setting)
  - Gain Adjustment: +6 to -18dB (1dB step by register setting)
- Selectable PCM Data Interface Timing: Long Frame / Short Frame/GCI
- Selectable PCM Data Rate: 4.096MHz, 2.048MHz (Register setting)
- OP Amp for External Gain Adjustment
- A-law/u-law Select (Hard pin, Register setting)
- Serial Interface for the internal register access
- Power on Reset
- Single Power Supply Voltage
  - +3.3V ± 0.3V
- Low Power Consumption
  - 42mW typ

PACKAGE

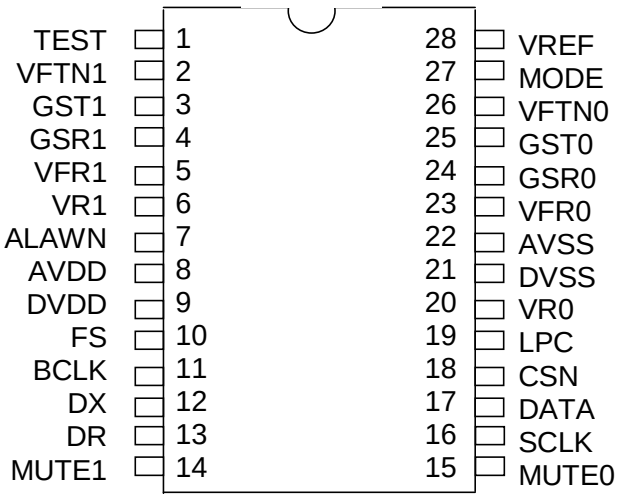
- 28pinSSOP
  10.40 x 7.9 mm (0.65mm pin pitch)

CONTENTS

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN CONDITION

Pin #	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Outout status (Power down mode)	Remarks
1	TEST	I	(*2)				Tied to AVSS
2	VFTN1	I	Analog				
3	GST1	O	Analog	50pF	10kΩ(*1)	Hi-Z	
4	GSR1	O	Analog	50pF	10kΩ(*1)	Hi-Z	
5	VFR1	I	Analog				
6	VR1	O	Analog	50pF	10kΩ	Hi-Z	
7	ALAWN	I	CMOS				
8	AVDD	–					
9	DVDD	–					
10	FS	I	CMOS				
11	BCLK	I	CMOS				
12	DX	O	CMOS	15pF		Hi-Z	
13	DR	I	CMOS				
14	MUTE1	I	CMOS				
15	MUTE0	I	CMOS				
16	SCLK	I	CMOS				
17	DATA	I/O	CMOS	15pF		Hi-Z (Input)	
18	CSN	I	CMOS				
19	LPC	O	Analog				0.22uF
20	VR0	O	Analog	50pF	10kΩ	Hi-Z	
21	DVSS	–					
22	AVSS	–					
23	VFR0	I	Analog				
24	GSR0	O	Analog	50pF	10kΩ(*1)	Hi-Z	
25	GST0	O	Analog	50pF	10kΩ(*1)	Hi-Z	
26	VFTN0	I	Analog				
27	MODE	I	(*2)				Tied to AVSS or AVDD
28	VREF	O	Analog				More than 1.0uF

*1) DC load(MIN.) includes a feedback resistance of input/output op-amp.
*2) Please tie to AVSS or AVDD, in order not to have a noise impact to the adjacent analog pins.

PIN FUNCTION

Pin#	Name	I/O	Function
1	TEST	I	**TEST MODE setting (Please tie to AVSS)** 0: Normal mode 1: Test mode
2	VFTN1	I	**Negative analog input of the transmit OPamp(AMPT1) for channel 1.** Transmit gain is defined by the ratio of R2/R1. R1 is the external input resister connected to this pin. R2 is the external feedback resister connected between this pin and GST1.
3	GST1	O	**Output of the transmit OPamp(AMPT1) for channel 1.**
4	GSR1	O	**Output of the receive OPamp(AMPR1) for channel 1.**
5	VFR1	I	**Negative analog input of the receive OPamp(AMTR1) for channel 1.** Receive gain is defined by the ratio of R4/R3. R3 is the external input resister connected to this pin. R4 is the external feedback resister connected between this pin and VR1.
6	VR1	O	**Analog Output equivalent to the received PCM data for channel 1.**
7	ALAWN	I	**A-law/u-law Select** 0: A-law 1: u-law
8	AVDD	-	**Positive supply voltage for analog circuit.** +3.3V supply.
9	DVDD	-	**Positive supply voltage for digital circuit.** +3.3V supply.
10	FS	I	**Frame sync input.** FS must be 8kHz clock which is synchronized with BCLK.
11	BCLK	I	**Bit clock of PCM data interface.** This clock is input for the internal PLL which gerenates the internal system clocks. This clock defines the input/output data rate of DX and DR. The frequency of BCLK should be 2.048MHz or 4.096MHz set via CPU register..
12	DX	O	**Serial output of PCM data.** The channel 1 data is output following the channel 0 data. The PCM data rate is synchronized with BCLK. This output remains in the high impedance state except for the period of transmitting PCM data.
13	DR	I	**Serial input of PCM data.** The channel 1 data is received following the channel 0 data. The PCM data rate is synchronized with BCLK.
14	MUTE1	I	**CH1 mute setting** 0: mute 1: normal operation
15	MUTE0	I	**CH0 mute setting** 0: mute 1: normal operation
16	SCLK	I	**Clock input of serial interface.**
17	DATA	I/O	**Data input of serial interface.**
18	CSN	I	**Read and write enable of serial interface.**
19	LPC	O	**Pin for PLL loop filter.** External capacitance(Min 0.22uF) should be connected between this pin and AVSS.

Pin#	Name	I/O	Function
20	VR0	O	**Analog Output equivalent to the received PCM data for channel 0.**
21	DVSS	-	**Ground for digital circuit.**
22	AVSS	-	**Ground for analog circuit.**
23	VFR0	I	**Negative analog input of the receive OPamp(AMTR0) for channel 0.** Receive gain is defined by the ratio of R4/R3. R3 is the external input resister connected to this pin. R4 is the external feedback resister connected between this pin and VR0.
24	GSR0	O	**Output of the receive OPamp(AMPR0) for channel 0.**
25	GST0	O	**Output of the transmit OPamp(AMPT0) for channel 0.**
26	VFTN0	I	**Positive analog input of the transmit Opamp(AMPT0) for channel 0.**
27	MODE	I	**MODE select** 0 : Register off mode 1 : normal mode
28	VREF	O	**Analog ground output.** External capacitance(1.0 uF) should be connected between this pin and AVSS.

CIRCUIT DESCRIPTION

Block	Function
AMPT0,1	Op-amp for input gain adjustment. The gain is adjusted with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor.
AMPR0,1	Op-amp for output gain adjustment. This op-amp is used as an inverting amplifier. The gain is adjusted with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor.
AAF0,1	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voice band. AAF is a 2nd order RC low-pass filter.
A/D	Converts analog signal to 8bit PCM data according to the companding schemes of ITU recommendation G.711; A-law or u-law. The band limiting filter is also integrated. The selection of companding schemes is set by ALAWN register or hard pin as follows: "H": u-Law "L": A-Law
D/A	Expands 8bit PCM data according to A-law or u-law. The selection of companding schemes is set by ALAWN register or hard pin as follows: "H": u-Law "L": A-Law
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of D/A output.
BGREF	Provides the stable analog ground voltage using an on-chip band-gap reference circuit which is temperature compensated. The output voltage is 1.5V for +3.3V operation.
GA0T/R GA1T/R GATN	Gain selects of analog I/O signals. It is posibble to select gain from +6dB to -18dB (1dB/step). Gain is defined by the internal register.
SERIAL I/F	Interface to the internal register by using SCLK, DATA, and CSN pins.
PLL	PLL generates system clock of AK2303LV. Reference clock is BCLK. More than 0.22uF capacitance should be connected between LPC and VSS as a PLL Loop filter.
PCM I/F	PCM data rate is available for 4.096, 2.048MHz which synchronizes with BCLK. Three kinds of data format (Long Frame, Short Frame,GCI) are available. Data format is selected by the register “PCM IF”. PCM IF = “L” LongFrame or ShortFrame (LF/SF are selected automatically) PCM IF = “H” GCI PCM data stream, which includes B1 and B2 data, is output through DX pin and input through DR pin. B2 PCM data stream always follows B1 PCM data stream. B1/B2 and Ch0/Ch1 assignment is changed by the SEL2B

FUNCTIONAL DESCRIPTION

PCM Data Interface

AK2303LV supports the following 3 PCM data formats

Long Frame Sync(LF)
Short Frame Sync(SF)
GCI

PCM data of both channels are multiplexed and interfaced through the common pins(DR,DX).The first 8bit is defined as B1 channel and the seconds 8bit is defined as B2 channel in the PCM data stream.
The order of PCM data is MSB first in each channel.

Selection of the interface mode

The GCI and ordinary PCM interface(LF,SF) are selectable through the CPU register as following table.
Either LF or SF is automatically selected by means of detecting the length of 8KHz frame signal in AK2303LV when PCM I/F is set to "0".

Register for PCM Interface mode select(Address:100 Bit:5)

PCMIF	PCM Interface	Comments
0	LF or SF	LF/SF are selected automatically
1	GCI	

∗ Default value after power-on reset =LF/SF mode(PCMIF=0).

LONG FRAME(LF) / SHORT FRAME (SF)

Automatic LF/SF selection

AK2303LV monitors the duration of the FS "H" level and selects either LF or SF interface format automatically.

Period of FS="H"	Interface format
more than 2 clocks of BCLK	LF
1 clock of BCLK	SF

Timing of the interface

16 bits PCM data (B1 and B2) is accommodated in 1 frame (125us) defined by 8kHz frame sync signal.
Although there are 32 time slots at maximum in 8kHz frame (when BCLK=4.096MHz), PCM data for AK2303LV occupy one time slot for channel 0 and channel 1, as is indicated in following.

Frame Sync signal (FS)

8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface.

Bit Clock (BCLK)

BCLK defines the PCM data rate. BCLK can be varied 4.096, 2.048MHz. All internal clock of the LSI is generated based on this BCLK signal.

Register for BCLK frequency select(Address:101 Bit:7,6)

CLKSEL[1:0]	BCLK frequency	comments
00	Reserved	
01	Reserved	
10	2.048MHz	Default value
11	4.096MHz	

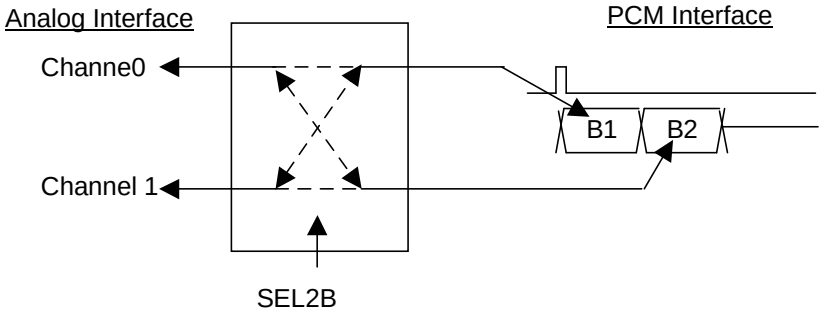
Position of the Ch0,Ch1 PCM data in the DX/DR data flow

B1 and B2 channel of the PCM data channel are assigned to Analog Ch0 and Ch1 as is defined by SEL2B register. Time-slot on PCM High-way (Time-slot#0~31(MAX)) can be also assigned for B1 and B2 channel data set as is defined by TS[4:0] register.

Channel selection

CH0,1selection(Address:100 Bit:6)

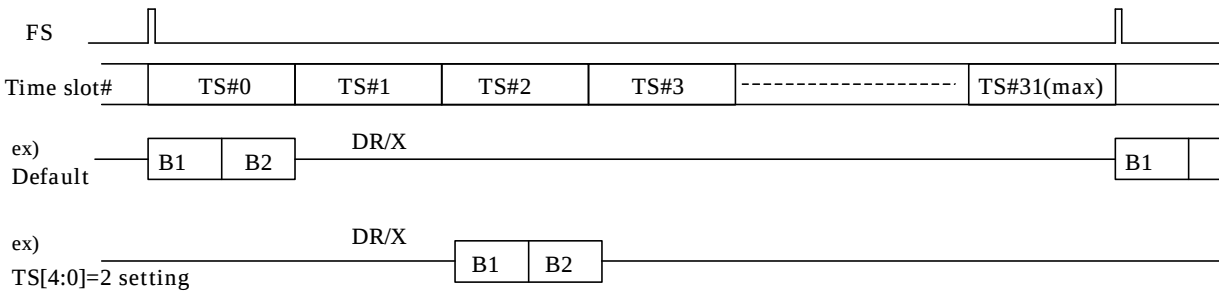
SEL2B	CH0	CH1	Remarks
0	B1	B2	Default on Reset
1	B2	B1	



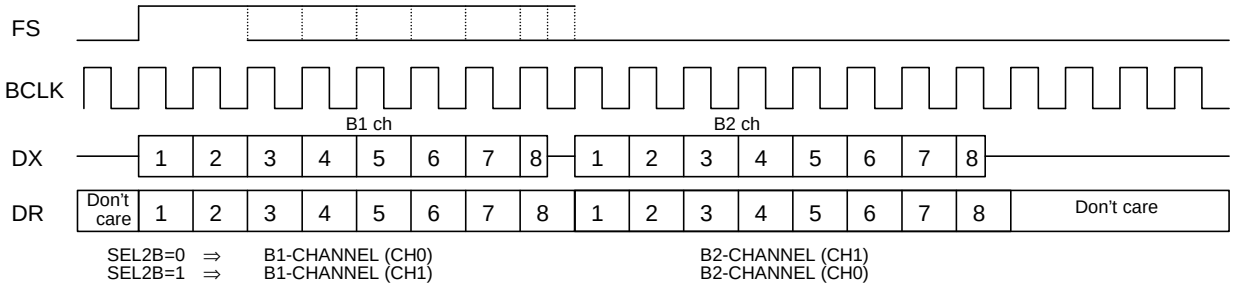
Time slot Assignment

B1, B2 Time-slot selection (Address:101 Bit:4~0)

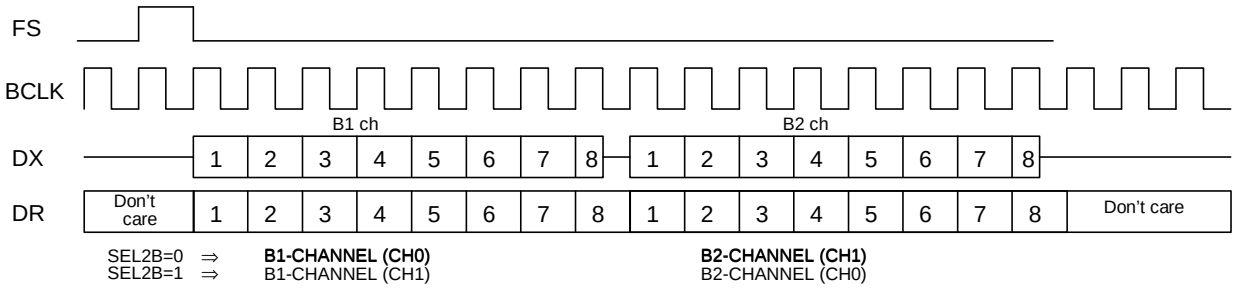
TS[4:0]	Time slot	B1	B2	Remarks
00000	0	The first half of 8bit in Time-slot#0	The latter half of 8bit in Time-slot#0	Default On Reset
00001 to 11110	XX	The first half of 8bit in Time-slot#XX	The latter half of 8bit in Time-slot#XX	
11111	31	The first half of 8bit in Time-slot#31	The latter half of 8bit in Time-slot#31	



Long Frame



Short Frame



! Important Notice

Please set time-slot selection as proper value. Maximum time slot is determined from clock speed.

At the power up sequence, please set the mute by MUTE0/1 before power up.
Then release them after the CODEC initialization and TS assignment to avoid the PCM output data collision with other CODEC's PCM output.

Please don't stop feeding FS and BCLK except in Full power down mode.

Internal PLL does free running when BCLK is not provided.

GCI (General Circuit Interface)

GCI data format and clocking which is used for ISDN application is shown as following.
4.096, 2.048MHz can be used for BCLK. Thus, data rate will be 2.048 or 1.024MHz.

Timing of the interface

8 bits PCM data is accommodated in 1 frame(125us) defined by 8kHz frame sync signal.
Although there are 16 time slots at maximum in 8kHz frame(when BCK=4.096MHz), PCM data on GCI occupy one time slot for channel 0 and channel 1, as is indicated in following.

Frame Sync signal (FS)

8kHz reference signal. This signal indicates the timing and the frame position of 8kHz GCI. High level duration of the FS is 1 clock period of BCLK.

Bit Clock (BCLK)

BCLK defines the GCI data rate. All the internal clock of the LSI is generated based on this BCLK signal. The data rate of GCI is half of BCLK. BCLK can be used either 4.096MHz or 2.048MHz.

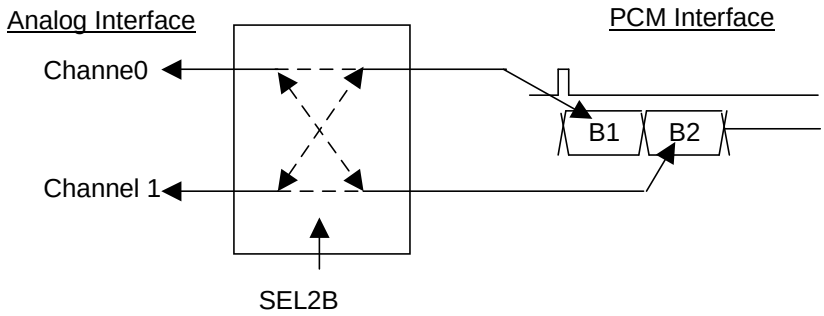
Position of the Ch0,Ch1 GCI data in the DX/DR data flow

B1 and B2 channel of the GCI data channel are assigned to Analog Ch0 and Ch1 as is defined by SEL2B register as same way as PCM interface. Time-slot also can be assigned by same way as PCM format.

Channel selection

CH0,1selection(Address:100 Bit:6)

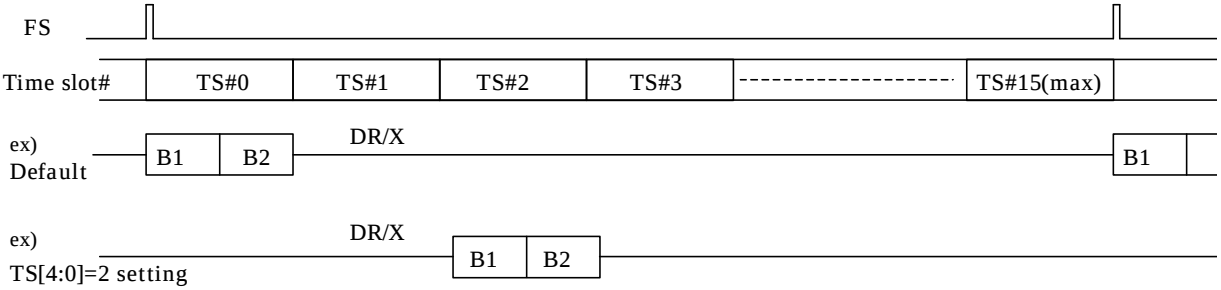
SEL2B	CH0	CH1	Remarks
0	B1	B2	Default On Reset
1	B2	B1	



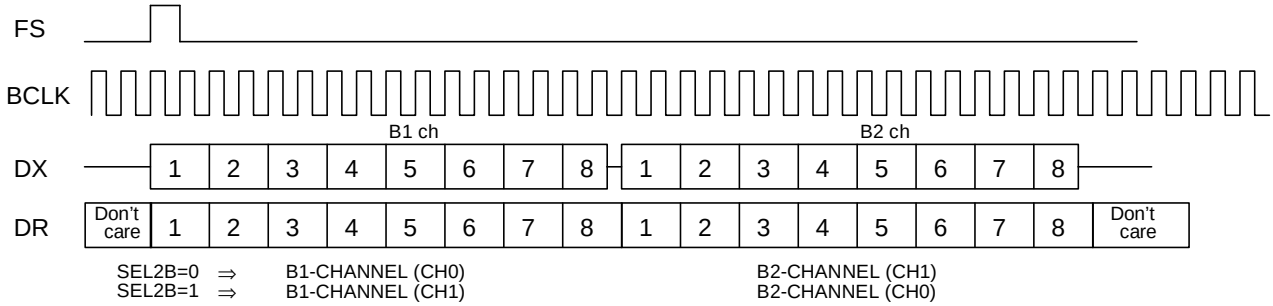
Time slot Assignment

B1, B2 Time-slot selection (Address:101 Bit:4~0)

TS[4:0]	Time slot	B1	B2	Remarks
00000	0	The first half of 8bit in Time-slot#0	The latter half of 8bit in Time-slot#0	Default On Reset
00001 to 01110	XX	The first half of 8bit in Time-slot#XX	The latter half of 8bit in Time-slot#XX	
01111	15	The first half of 8bit in Time-slot#15	The latter half of 8bit in Time-slot#15	



GCI



! Important Notice

Please set time-slot selection as proper value. Maximum time slot is determined from clock speed.

At the power up sequence, please set the mute by MUTE0/1 before power up.
Then release them after the CODEC initialization and TS assignment to avoid the PCM output data collision with other CODEC's PCM output.

Please don't stop feeding FS and BCLK except in Full power down mode.

Internal PLL does free running when BCLK is not provided.

MUTE

The output on each channel can be muted independently throu gh the CPU register as shown in the table.

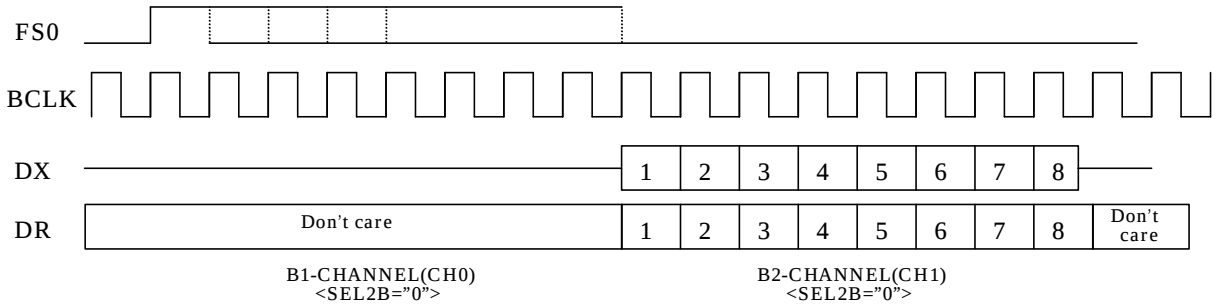
Mute register(Address:100 Bit:5,4)

MTCH0,1	Operation	DX pin	VRX pin
0	Normal	PCM data output	CODEC analog output
1	Mute	High-Impedance(*1)	AGND*

(*1)
MTCH0 and MTCH1 are the mute control bit for CH0 and CH1, respectively. B1 and B2 channel muted by MTCH0/1 is defined by SEL2B bit shown in the PCM Interface section.

<EXAMPLE>

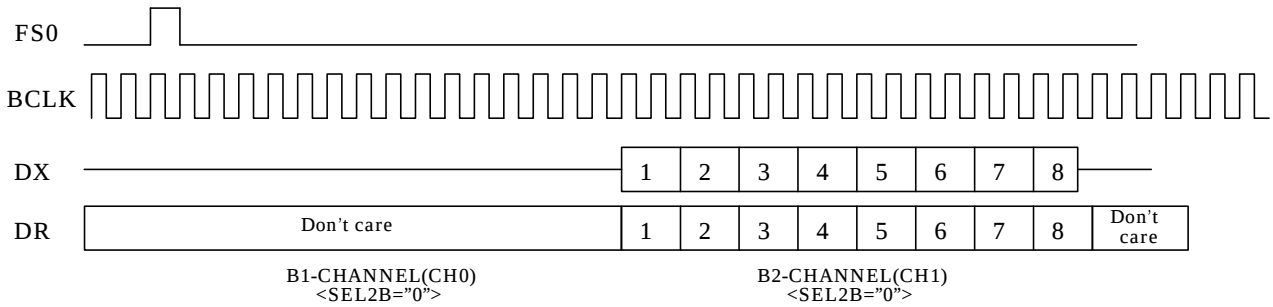
LF Mode CH0 mute (MTCH=1, MTCH1=0, SEL2B=0)



VRX0 : CODEC CH0 analog output is always at AGND level.

VRX1 : CODEC CH1 analog output is the signal converted from the PCM data of CH1 input through DR pin.

GCI mode CH0 mute (MTCH0=1, MTCH1=0, SEL2B=0)



VRX0 : CODEC CH0 analog output is always at AGND level.

VRX1 : CODEC CH1 analog output is the signal converted from the PCM data of CH1 input through DR pin.

GAIN ADJUSTMENT

Analog input/output gain can be adjusted at the range from +6dB to –18dB by 1.0dB step through CPU register.

VR Register(Address:011 –000 Bit:4 –0)

GanT4 GanR4	GanT3 GanR3	GAnT2 GAnR2	GAnT1 GAnR1	GAnT0 GAnR0	Gain [dB]	Remarks
0	0	0	0	0	+6	
0	0	0	0	1	+5	
0	0	0	1	0	+4	
0	0	0	1	1	+3	
0	0	1	0	0	+2	
0	0	1	0	1	+1	
0	0	1	1	0	0	Default
0	0	1	1	1	-1	
0	1	0	0	0	-2	
0	1	0	0	1	-3	
0	1	0	1	0	-4	
0	1	0	1	1	-5	
0	1	1	0	0	-6	
0	1	1	0	1	-7	
0	1	1	1	0	-8	
0	1	1	1	1	-9	
1	0	0	0	0	-10	
1	0	0	0	1	-11	
1	0	0	1	0	-12	
1	0	0	1	1	-13	
1	0	1	0	0	-14	
1	0	1	0	1	-15	
1	0	1	1	0	-16	
1	0	1	1	1	-17	
1	1	---	---	---	-18	

RESET

Power on Reset

AK2303LV automatically generates the internal reset pulse which resets all the circui t that is necessary to start the initialization after the power on reset. The CPU registers are set to the default value.

After the internal reset pulse is generated, CODEC Ch0/Ch1 starts the initialization procedure by being fed FS signal, and it takes 180ms(typ.), 350ms(max) to complete the initialization after the detection of power on.

Power up slope to enable the Power-on Reset

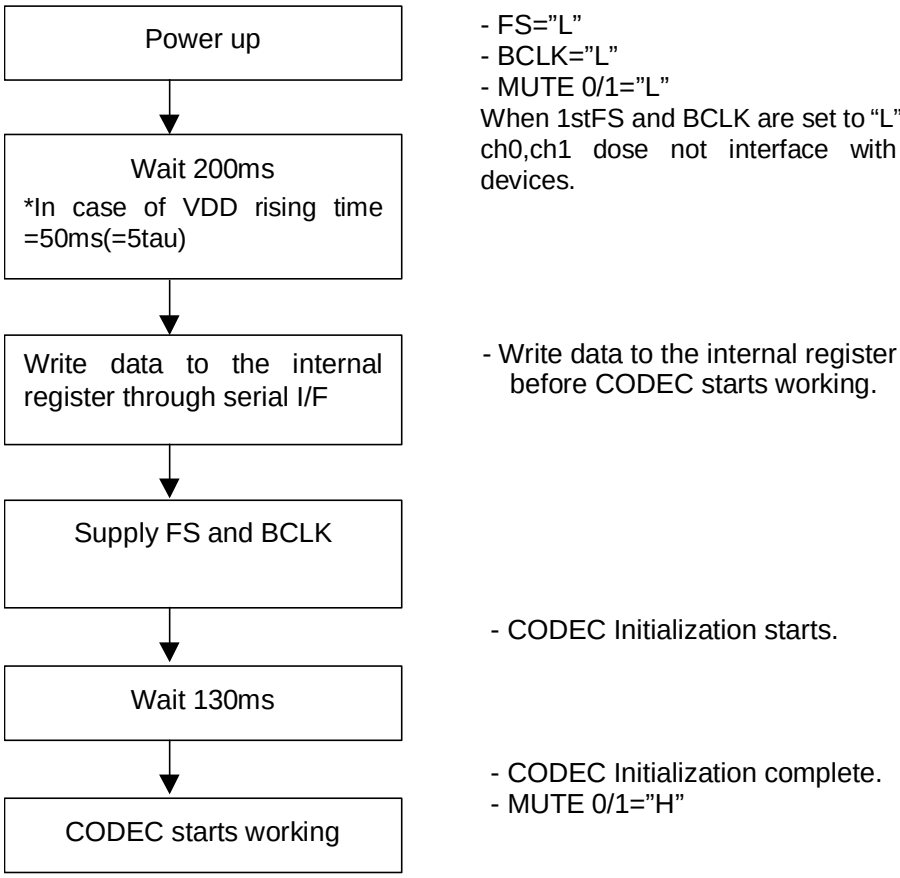
When power-up slope is no longer than 50ms(=5tau:tau is time constant), Power On Reset works normally.

When the time is longer than 50ms, Power On Reset is not activated and no internal registers are initialized. In this case all registers must be written through CPU interface.

NOTE) For stable operation after power up, we recommend to write all register value through CPU interface after power up.

Recommended start up procedure

The following start up procedure is recommended when AK2303LV is going to power up.



POWER DOWN

Power consumption is reduced in the power down mode.
In the power down mode, the current fed to analog circuits and the clock for digital circuits, are stopped, and the related circuits hold its current status.

There are two power down modes.
- **Power down for all circuits**
- **Power down by block**

* In the power down mode, the output pins of corresponding blocks turn to Hi-Z. (See page 5)

POWER DOWN MODE SETTING
2 power down modes -

Mode	Circuits	Registers	Operation for "0"/"1"	Note
All circuit	All	PD	"0" : Normal "1" : Power down	- CPU Registers are not reset.(hold its value) **- Serial I/F is available.** - No need to supply FS, BCLK.
Block	CODEC CH0	PDCH0	"0" : Normal "1" : Power down	- Keep supplying FS and BCLK. - AMPTn, AMPRn(n=0,1) Input/Output is active, even when CODEC CHn(n=0,1) is in power down mode, **Please refer table of the next page in detail.**
	CODEC CH1	PDCH1		

WAKE UP FROM POWER DOWN MODE
After power down mode for CODEC CH0/CH1 is cleared, the CODEC circuit starts to be initialized.
It takes 130mS(typ).

WAKE UP FROM FULL POWER DOWN MODE
When full circuit power down mode for CODEC is cleared, AK2303LV starts the same wake up sequence as one at power on. It takes 250ms(typ).

POWER DOWN BLOCK		ALL BLOCK	CODEC CH0	CODEC CH1	CODEC CH0&1
REGISTER		PD	PDCH0	PDCH1	PDCH0 PDCH1
Channel 0	AMPT0	OFF			
	GA0T	OFF	OFF		OFF
	AAF0	OFF	OFF		OFF
	CODEC CH0	OFF	OFF		OFF
	SMF0	OFF	OFF		OFF
	GA0R	OFF			
	AMPR0	OFF			
Channel 1	AMPT1	OFF			
	GA1T	OFF		OFF	OFF
	AAF1	OFF		OFF	OFF
	CODEC CH1	OFF		OFF	OFF
	SMF1	OFF		OFF	OFF
	GA1R	OFF			
	AMPR1	OFF			
PCM I/F		OFF			OFF
PLL		OFF			
BGREF		OFF			
SERIAL I/F					

SERIAL INTERFACE

The internal registers can be read/written with SCLK, DATA, and CSN pins.

1word consists of 16bits. The first 4bits are the instruction code which specifies read/write.
The following 3bits specify the address. The rest of 8bits are for setting registers.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I3	I2	I1	I0	A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
Instruction code (4bit)				Address (3bit)			*	Data for internal registers (8bit)							

*)Dummy bit for adjusting the I/O timing when reading register.

INSTRUCTION CODEC

I3	I2	I1	I0	Read/Write
1	1	1	0	Read
1	1	1	1	Write
Other codes				No action

SCLK and WRITE/READ

(1) Input data are loaded into the internal shift register at the rising edge of SCLK.
(2) The rising edge of SCLK is counted after the falling edge of CSN.
(3) When CSN is "L" and more than 16 SCLK pulses:
[WRITE] Data are loaded into the internal register at the rising edge of the SCLK 16th pulse.
[READ] DATA pin is switched to an input pin at the falling edge of the SCLK 16th pulse.

CSN and WRITE / READ CANCELLATION

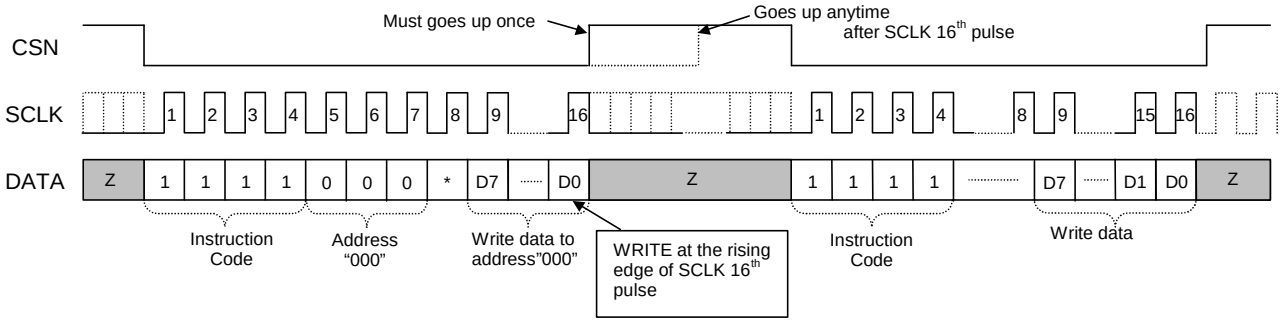
(1) WRITE is cancelled when CSN goes up before the rising edge of the SCLK 16th pulse.
(2) READ is cancelled when CSN goes up before the falling edge of the SCLK 16th pulse.

SERIAL WRITE / READ (SERIAL ACCESS)

(1) CSN must go up to "H" before the next access in successive access.
(2) When the next access is going to be done , if CSN remains to be "L", successive access can not be done.

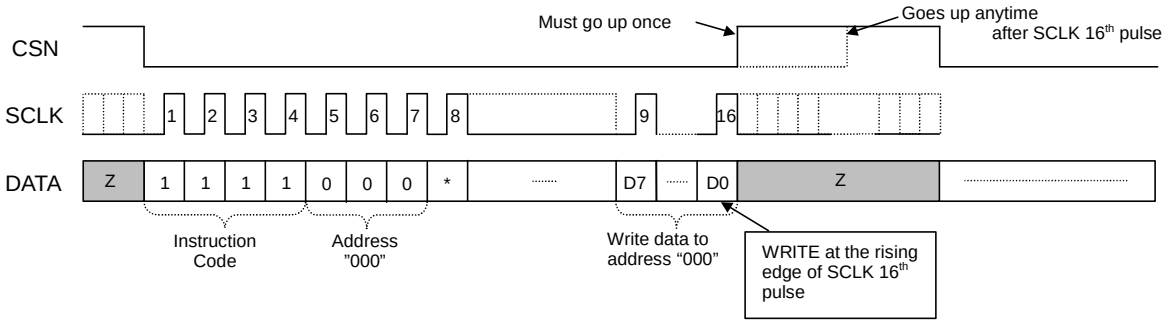
WRITE

Continuous SCLK

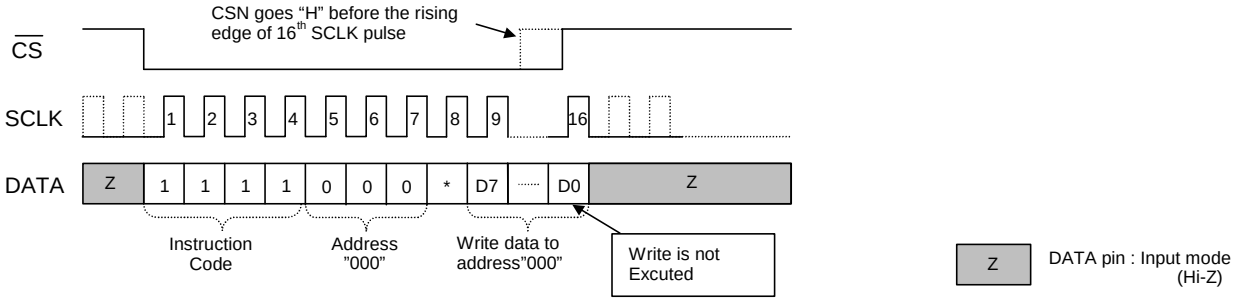


Burst SCLK

SCLK can be stop at "H" level or "L" level at anytime during the write cycle. After resuming the SCLK, write cycle is retrieved
normally.

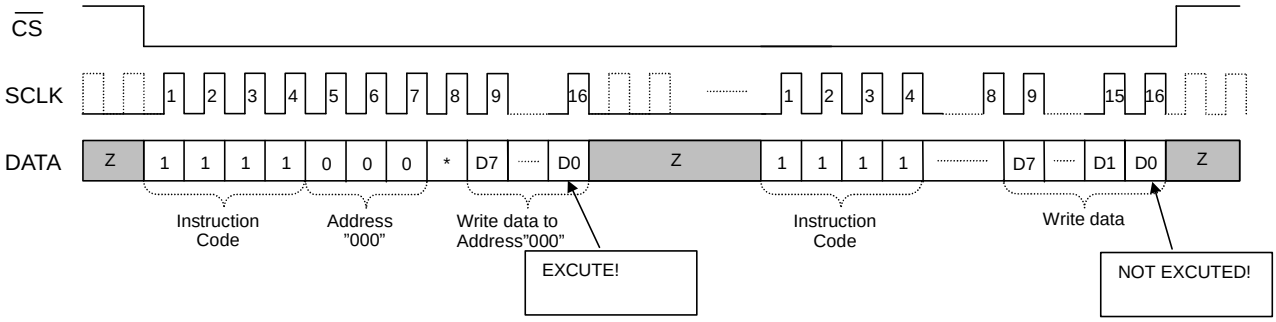


CANCELLATION



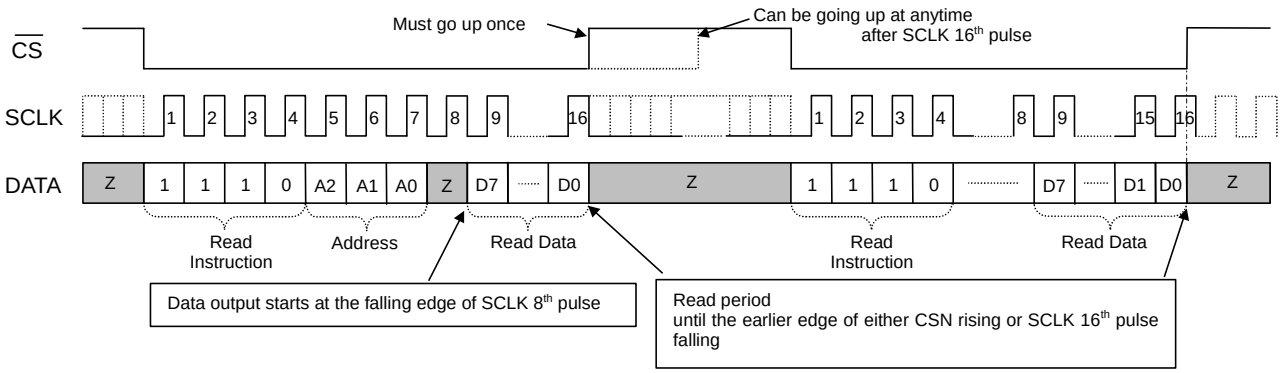
SERIAL ACCESS

Serial access with CSN staying "L" during the serise of write cycle.

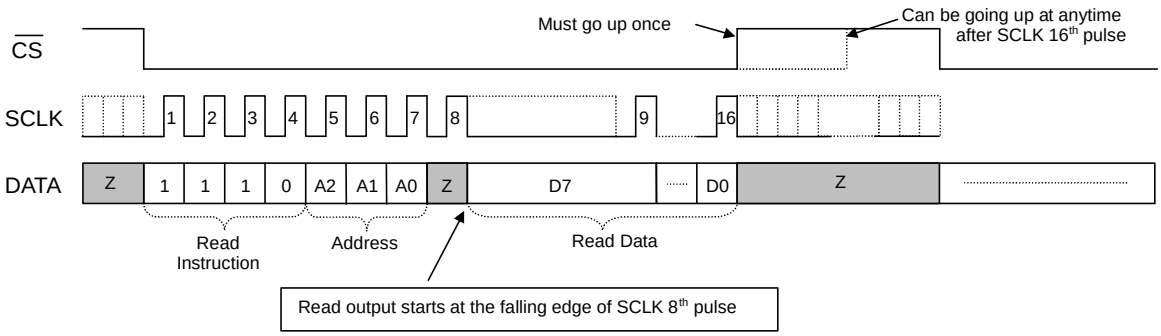


READ

CONTINOUS SCLK

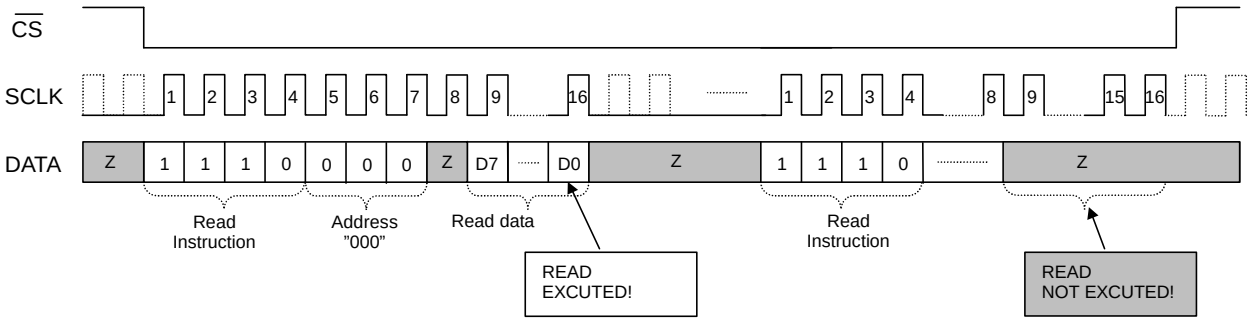


Burst SCLK

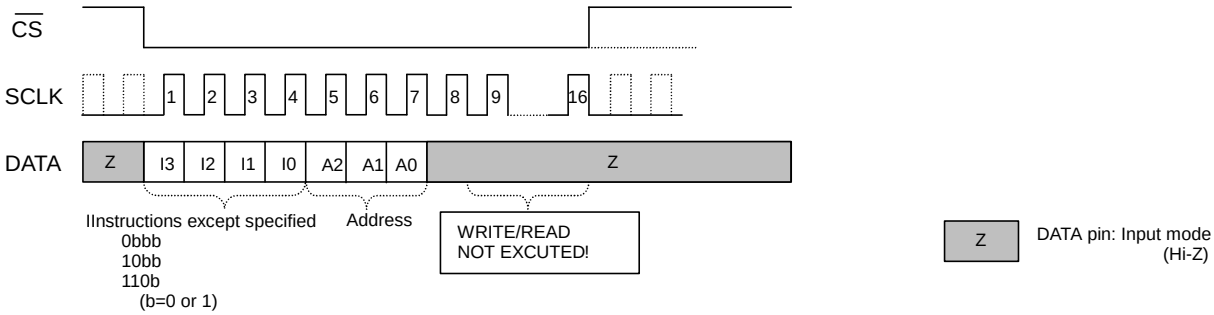


SERIAL ACCESS

Serial access with CSN staying “L” during the serise of read cycle.



DISCORD OF INSTRUCTION CODE



MODE SETTING

AK2303LV has a normal mode and a register off mode set by MODE pin. (pin#27)
In nomal mode, all registers are able to be accessed through the serial interface and the various functions listed in the table of the next page can be controled via the interface.
In register off mode, all registers except volume are forced to defult value.
The register off mode eliminates the fatal abnormal condition of system caused by the crush of the internal register value whitch may occurr due to the lightning, the strong electromagnetic field and quick power supply change.

MODE pin status	MODE
MODE="H" (AVDD)	Normal mode: 1.All registers can be accessed. 2. It iis highly recommended that all the register are to be written periodically and after the abnormal circumstances happens.
MODE="L" (AVSS)	Register off mode: 1.Register data of address "100" and "101" are forced to defult value. The register of adress "000" to "001" are remain to be accessed. 2.ALAWN, MUTE1 and MUTE0 setting are valid only from pin setting.

Attention: Please connect MODE pin to AVSS or AVDD.

REGISTER MAP

Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	*	0	0	-	GA0R4	GA0R3	GA0R2	GA0R1	GA0R0
0	0	1	*	0	0	-	GA1R4	GA1R3	GA1R2	GA1R1	GA1R0
0	1	0	*	0	0	-	GA0T4	GA0T3	GA0T2	GA0T1	GA0T0
0	1	1	*	0	0	-	GA1T4	GA1T3	GA1T2	GA1T1	GA1T0
1	0	0	*	ALAWN	SEL2B	PCMIF	MTCH1	MTCH0	PD	PDCH1	PDCH0
1	0	1	*	CLKSEL1	CLKSEL0	-	TS4	TS3	TS2	TS1	TS0
1	1	0	*	Reserved							
1	1	1	*	Reserved							

*) Dummy Bit
Note) All registers except “0” and “Reserved” can read/write.
Note) “0” bit data can not be written, however “0” data will be output when it is read.
Note) When mode pin is “L”, register address “100” and “101” is fixed to default value.

INITIALIZATION OF REGISTERS

The registers are initialized at POWER ON RESET only.
Power on reset may not be excuted due to the difference of power up time constant. Thus it is highly recommended that all the register (address(000 – 101)) are to be written at the time of the power up and after the abnormal circumstances happens such as micro interrupt of the power line or mal operation due to lightning.

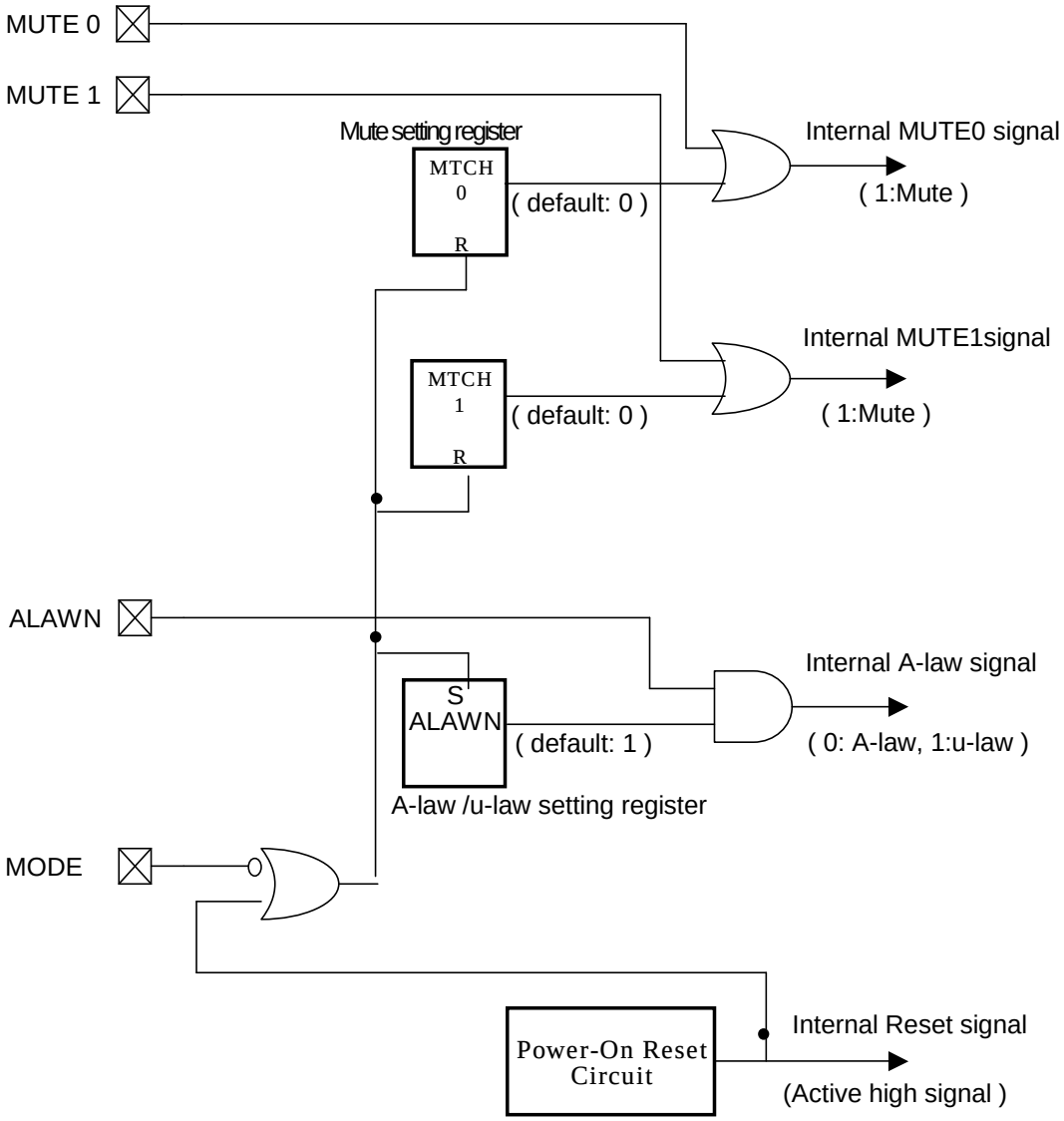
REGISTER FUNCTION

Address	Bit	Name	Default	Function	Refer
000	0	GA0R0	0	**Receive gain adjustment on ch0**	
	1	GA0R1	1	+6 to –18dB by 1.0dB step	
	2	GA0R2	1		
	3	GA0R3	0	00000: +6dB 11xxx: -18dB	
	4	GA0R4	0		
	5	-			
	6	-			
	7	-			
001	0	GA1R0	0	**Receive gain adjustment on ch1**	
	1	GA1R1	1	+6 to –18dB by 1.0dB step	
	2	GA1R2	1		
	3	GA1R3	0	00000: +6dB 11xxx: -18dB	
	4	GA1R4	0		
	5	-			
	6	-			
	7	-			

Address	Bit	Name	Default	Function	Refer
010	0	GA0T0	0	**Transmit gain adjustment on ch0** +6 to –18dB by 1.0dB step 00000: +6dB 11xxx: -18dB	
	1	GA0T1	1		
	2	GA0T2	1		
	3	GA0T3	0		
	4	GA0T4	0		
	5	-			
	6	-			
	7	-			
011	0	GA1T0	0	**Transmit gain adjustment on ch1** +6 to –18dB by 1.0dB step 00000: +6dB 11xxx: -18dB	
	1	GA1T1	1		
	2	GA1T2	1		
	3	GA1T3	0		
	4	GA1T4	0		
	5	-			
	6	-			
	7	-			
100	0	PDCH0	0	**CODEC CH0,1 Power down control** 0: Power ON 1: Power OFF	
	1	PDCH1	0		
	2	PD	0	**Full Power down** 0: Power ON 1: Power OFF	
	3	MTDX0	0	**Mute control: VR0.VR1,DX pin** 0: Normal output 1: Mute	
	4	MTDX1	0		
	5	PCMIF	0	**PCM Interface select** 0: LF/SF 1: GCI	
	6	SEL2B	0	**PCM data channel select** 0: CH0→B1 1: CH1→B1	
	7	ALAWN	1	**A/u-law select** 0: A-law 1: μ-law	
101	0	TS0	0	**Time slot setting** 4.096MHz : 0 to 31 2.048MHz : 0 to 15 1.024MHz : 0 to 7	
	1	TS1	0		
	2	TS2	0		
	3	TS4	0		
	4	TS5	0		
	5	-	0		
	6	CLKSEL0	0	**BCLK frequency setting *** CLKSEL[1:0]= 00: (Reserved) 01: (Reserved) 10: 2.048MHz 11: 4.096MHz	
	7	CLKSEL1	1		
110	0		0	Reserved	
	1		0		
	2		0		
	3		0		
	4		0		
	5		0		
	6		0		
	7		0		

* Please set the same frequency as BCLK input.

Address	Bit	Name	Default	Function	Refer
111	0		0	Reserved	
	1		0		
	2		0		
	3		0		
	4		0		
	5		0		
	6		0		
	7		0		


MUTE 0
MUTE 1
Mute setting register
MTCH
0
R
(default: 0)
Internal MUTE0 signal
(1:Mute)
MTCH
1
R
(default: 0)
Internal MUTE1signal
(1:Mute)
ALAWN
S
ALAWN
(default: 1)
Internal A-law signal
(0: A-law, 1:u-law)
A-law /u-law setting register
MODE
Power-On Reset
Circuit
Internal Reset signal
(Active high signal)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltages Analog/Digital Power Supply	AVDD DVDD	-0.3	6.5	V
VSS Voltage	AVSS DVSS	-0.1	0.1	V
Digital Input Voltage	VTD	-0.3	VDD+0.3	V
Analog Input Voltage	VTA	-0.3	VDD+0.3	V
Input current (except power supply pins)	IIN	-10	10	mA
Storage Temperature	Tstg	-55	125	°C

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies Analog/Digital power supply	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	Ta	-40		85	°C
Frame Sync Frequency	FS		8		kHz

Note) All voltages reference to ground : VSS=0V

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD=+3V±0.3V, Ta = –40 ~ +85 °C, FS=8kHz.

DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption BCLK=2048kHz	PDD1	PDCH0,1 =0,0 All output unloaded		42		mW
	PDDd	PD = 1 Power down		2.5		
Output High Voltage (CMOS level)	VOH	IOH=-1.6mA	0.8VDD			V
Output Low Voltage (CMOS level)	VOL	IOL=1.6mA			0.4	V
Input High Voltage1 (CMOS level)	VIH1		0.7VDD			V
Input Low Voltage1 (CMOS level)	VIL1				0.3VDD	V
Input Leakage Current	Ii		-10		+10	uA
Input Capacitance	Ci				5	pF
Output Leakage Current	Io	Tri-state mode	-10		+10	uA

CODEC

Absolute Gain (VDD=3.3V ±0.3V)

Parameter	Conditions		Min	Typ	Max	Units
Analog Input Level	Input: 0dBm0@1020Hz			0.531		Vrms
Absolute Transmit Gain		(Typ)	(-0.15)	-	(+0.15)	dB
			-0.25	-	+0.25	dB
Analog Output Level	Input: 0dBm0@1020Hz			0.531		Vrms
Absolute Receive Gain		(Typ)	(-0.15)	-	(+0.15)	dB
			-0.25	-	+0.25	dB
Maximum Overload Level	+3.14dBm0			0.762		Vrms

* Power supply and the temperature are in typical condition. Not tested.

Gain Tracking

Parameter	Conditions		Min	Typ	Max	Units
Transmit Gain Tracking Error	Reference Level: -10dBm0 1020Hz Tone	-55dBm0 ~-50dBm0	-1.2	-	1.2	dB
		-50dBm0 ~-40dBm0	-0.4	-	0.4	
		-40dBm0 ~ 3dBm0	-0.2	-	0.2	
Receive Gain Tracking Error	Reference Level: -10dBm0 1020Hz Tone	-55dBm0 ~-50dBm0	-1.2	-	1.2	dB
		-50dBm0 ~-40dBm0	-0.4	-	0.4	
		-40dBm0 ~ 3dBm0	-0.2	-	0.2	

Frequency Response

Parameter	Conditions		Min	Typ	Max	Units
Transmit Frequency Response	Relative to: 0dBm0@1020Hz	0.05kHz	-	-	-30	dB
		0.06kHz	-	-	-26	
		0.2kHz	-1.8	-	0	
		0.3 ~3.0kHz	-0.15	-	0.15	
		3.4kHz	-0.8	-	0	
		4.0kHz	-	-	-14	
Receive Frequency Response	Relative to: 0dBm0@1020Hz	0 ~3.0kHz	-0.15	-	0.15	dB
		3.4kHz	-0.8	-	0	
		4.0kHz	-	-	-14	

Distortion

Parameter	Conditions		Min	Typ	Max	Units
Transmit Signal to Distortion	1020Hz Tone	-40dBm0 ~-45dBm0	25	-	-	dB
		-30dBm0 ~-40dBm0	30	-	-	
		0dBm0 ~-30dBm0	36	-	-	
Receive Signal to Distortion	1020Hz Tone	-40dBm0 ~-45dBm0	25	-	-	dB
		-30dBm0 ~-40dBm0	30	-	-	
		0dBm0 ~-30dBm0	36	-	-	
Single Frequency Distortion Transmit			-	-	-46	dB
Single Frequency Distortion Receive			-	-	-46	dB
Intermodulation Distortion	-6dBm@860Hz,1380Hz		-	-	-42	dB

Note) C-message Weighted for u-Law, Psophometric Weighted for A-Law

Envelope delay Distortion

Parameter	Conditions	Min	Typ	Max	Units
Transmit Delay, Absolute	f =1600Hz	-	-	360	us
Transmit Delay, Relative	f =500Hz ~600Hz	-	-	220	
	f =600Hz ~1000Hz	-	-	145	
	f =1000Hz ~2600Hz	-	-	75	us
Relative to f=1600Hz	f =2600Hz ~2800Hz	-	-	105	
	f =2800Hz ~3000Hz	-	-	155	
Receive Delay, Absolute	f =1600Hz			240	us
Receive Delay, Relative	f =500Hz ~1000Hz	-40	-	-	
	f =1000Hz ~1600Hz	-30	-	-	
	f =1600Hz ~2600Hz	-	-	90	us
Relative to f=1600Hz	f =2600Hz ~2800Hz	-	-	125	
	f =2800Hz ~3000Hz	-	-	175	

Noise

Parameter	Conditions		Min	Typ	Max	Units
Idle Channel Noise [1)]	u-law, C-message		-	0	10	dBrnC0
A!D	A-law, Psophometric		-	90	-80	dBm0p
Idle Channel Noise [2)]	u-law, C-message		-	0	10	dBrnC0
D!A	A-law, Psophometric		-	90	-80	dBm0p
Noise, Single Frequency	VFXIN = 0 Vrms, DR = DX f=0 ~100kHz		-	-	-53	dBm0
PSRR, Transmit	AVDD=DVDD=5V±100mVop f=0 ~50kHz		40	-	-	dB
PSRR, Receive	AVDD=DVDD=5V±100mVop f=0 ~50kHz		40	-	-	dB
Spurious Out-of-Band Signal	0dBm0,	4.6 ~7.6kHz	-	-	-30	
at VRX Output [3)]	0.3 ~3.4kHz	7.6 ~8.4kHz	-	-	-40	dB
	PCM CODE	8.4 ~100kHz	-	-	-32	

Note 1) Analog Input = Analog Ground
Note 2) Digital Input(DR) = +0 Code
Note 3) Not tested in production Test. Parameters guaranteed by design.

Interchannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive	0dBm0@VFXIN, Idle PCM code	-	-	-75	dB
Receive to Transmit	0dBm0 code level, VFXIN = 0 Vrms	-	-	-75	dB
Transmit to Transmit	0dBm0@VFXIN, Idle PCM code	-	-	-75	dB
Receive to Receive	0dBm0 code level, VFXIN = 0 Vrms	-	-	-75	dB

Intrachannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive	0dBm0@VFXIN, Idle PCM code	-	-	-75	dB
Receive to Transmit	0dBm0 code level, VFXIN = 0 Vrms	-	-	-75	dB

Analog Interface Transmit Amplifier

Parameter	Conditions	Min	Typ	Max	Units
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	50	pF
Output voltage Swing	GSTn(n=0,1)		2.25		Vp-p

Analog Interface Receive Output (VDD: 3.3V±0.3V)

Parameter	Conditions	Min	Typ	Max	Units
Output voltage(AGND level)	+0 PCM code input	-	1.5	-	V
Load Resistance		10			kΩ
Load Capacitance				50	pF
Output voltage Swing	VRn(n=0,1)	-	2.25	-	Vp-p

Analog Interface Receive Output Amplifier

Parameter	Conditions	Min	Typ	Max	Units
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	50	pF
Output Voltage Swing	GSRn(n=0,1)	-	2.25	-	Vp-p

VOLUME (GA0T,GA0R,GA1T,GA1R)

Parameter	Pin	Conditions	Min	typ	max	Unit
Step margin		Relative to: 0dB	-1.0		+1.0*)	dB

*)Monotonus increase/decrease is guranteed

PCM INTERFACE (Long Frame, Short Frame, GCI)

Unless otherwise noted, the specification applies for TA = -40 to +85°C, VDD = 5V±5%/3V±0.3V,VSS = 0V and FS0= 8kHz. All timing parameters are measured at VOH = 0.8VDD and VOL =0.4V.

Parameter	Symbol	Min	Typ	Max	Units	Ref Fig
FS Frequency	$1/t_{PF}$	-	8	-	kHz	Fig1 Fig2 Fig3
BCLK Frequency	$1/t_{PB}$	2048		4096	kHz	
BCLK Pulse Width High	t_{WBH}	80			ns	
BCLK Pulse Width Low	t_{WBL}	80			ns	
Rising Time: (BCLK,FS0,FS1,DX0,DX1,DR0,DR1)	t_R			40	ns	
Falling Time: (BCLK,FS0,FS1,DX0,DX1,DR0,DR1)	t_F			40	ns	
Hold Time: BCLK Low to FS High	t_{HBF}	40			ns	
Setup Time: FS High to BCLK Low	t_{SFB}	70			ns	
Setup Time: DR to BCLK Low	t_{SDB}	40			ns	
Hold Time: BCLK Low to DR	t_{HBD}	40			ns	
Delay Time: BCLK High to DX valid Note1)	t_{DBD}			60	ns	
Long Frame						
Hold Time: 2nd period of BCLK Low to FS Low	t_{HBFL}	40			ns	Fig1
Delay Time: FS or BCLK High, whichever is later,to DX valid Note1)	t_{DZFL}			60	ns	
Delay Time: BCLK Low to DX High-Z Note1)	t_{DZCL}	10		60	ns	
FS Pulse Width Low	t_{WFSL}	1			BCLK	
Short Frame						
Hold Time: BCLK Low to FS Low	t_{HBFS}	40			ns	Fig2
Setup Time: FS Low to BCLK Low	t_{SFBS}	40			ns	
Delay Time: BCLK Low to DX High-Z Note1)	t_{DZCS}	10		60	ns	
GCI						
BCLK Frequency	$1/t_{PBG}$	2048		4096	kHz	Fig3
Delay Time: Second BCLK Low to DX High-Z	t_{DZCG}	10		60	ns	
Setup Time: DR to Second BCLK High	t_{SDBG}	40			ns	
Hold Time: Second BCLK High to DR	t_{HBDG}	40			ns	

Note1) Measured with 150pF Load capacitance and driving two LSTTLs

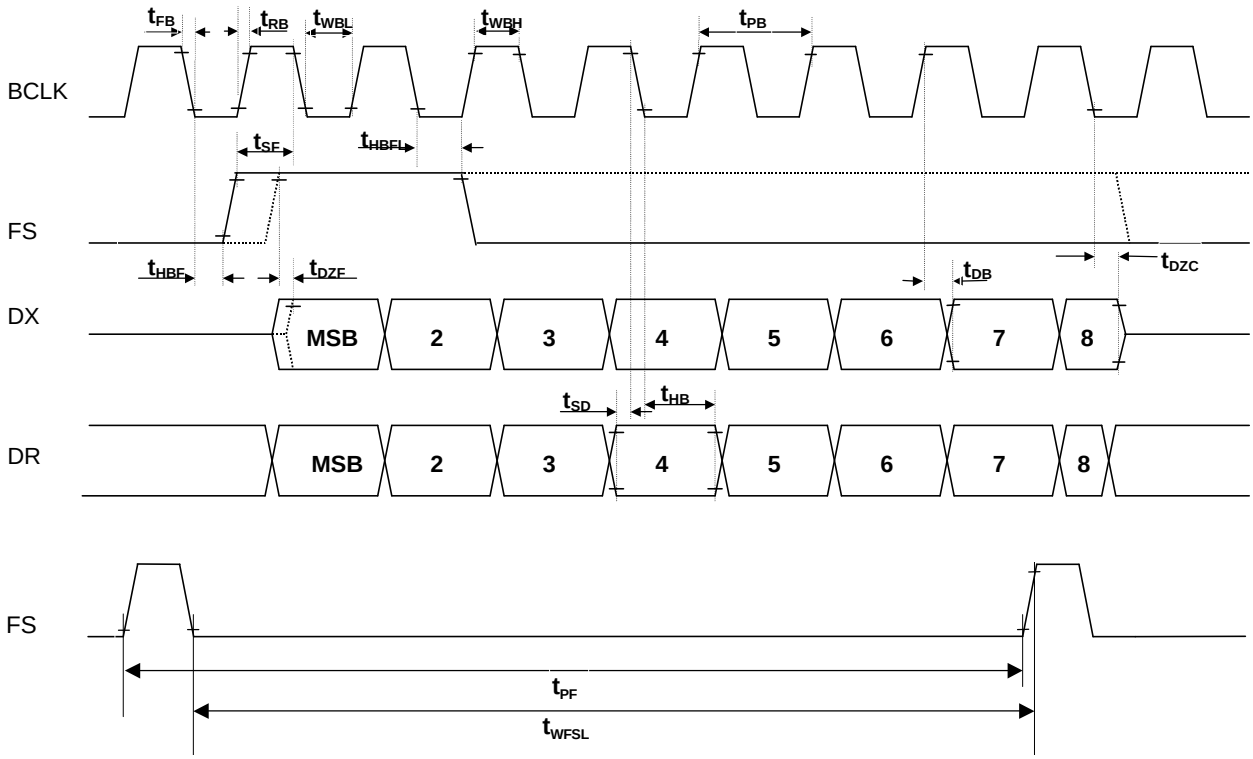


Fig1 PCM Interface Timing < Long Frame >

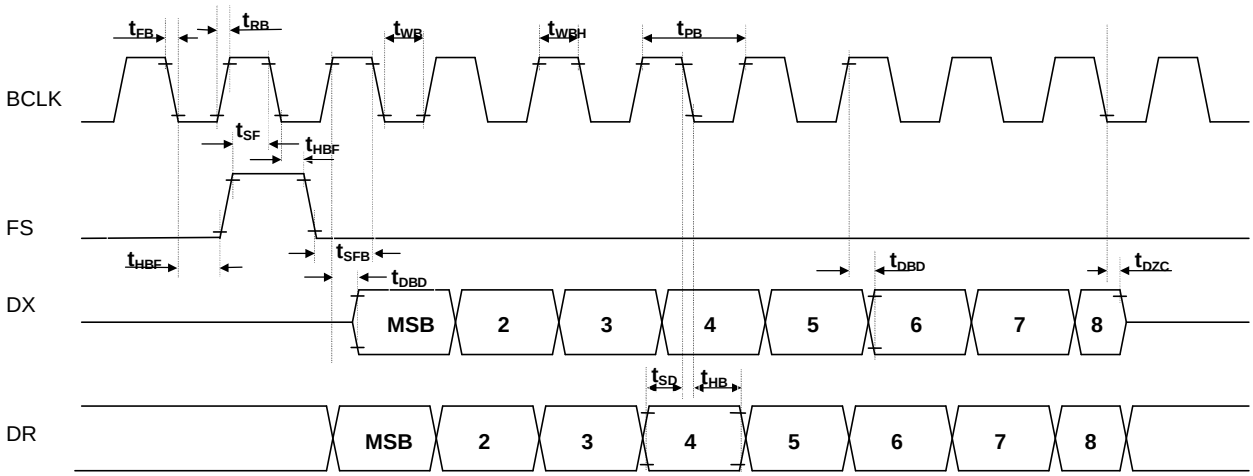


Fig2 PCM Interface Timing < Short Frame >

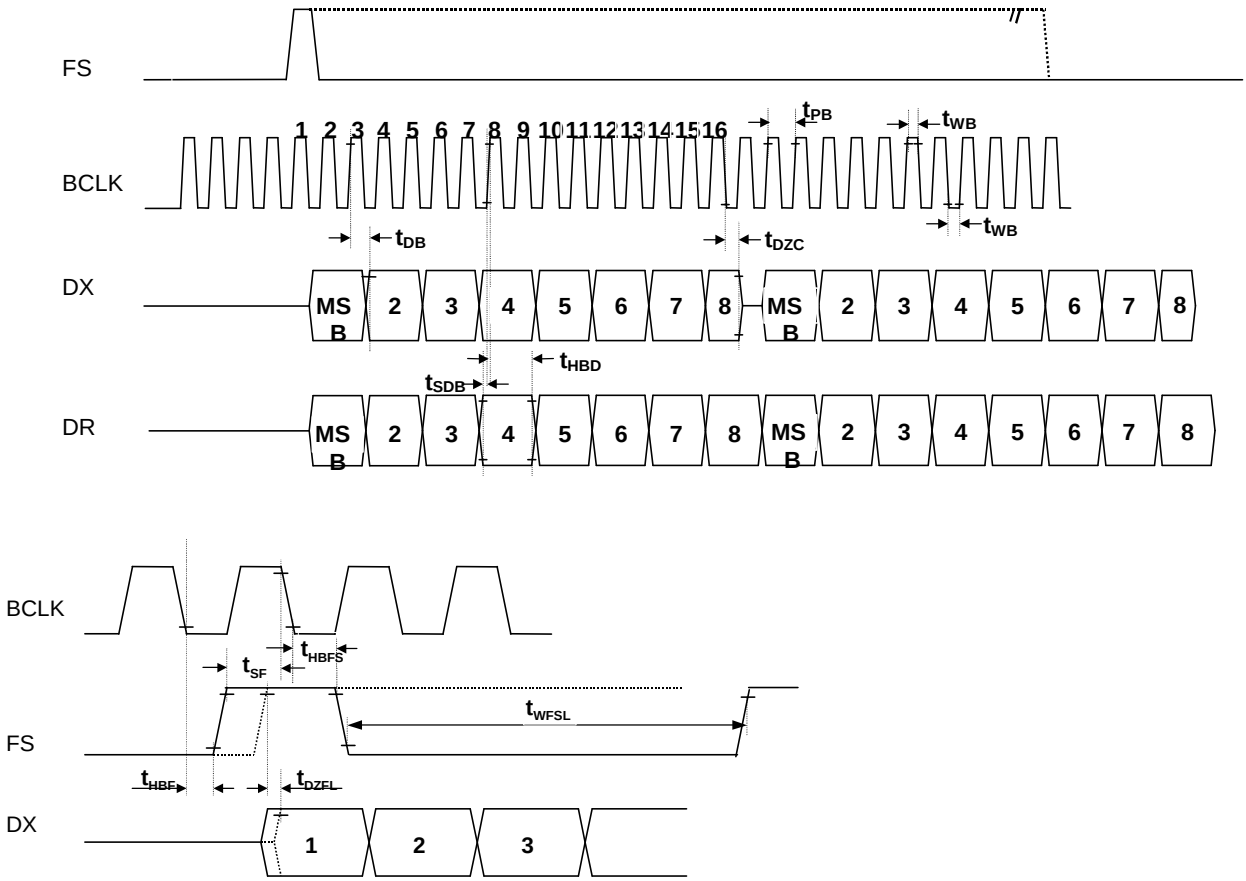


Fig3 PCM Interface Timing < GCI >

SERIAL INTERFACE

Parameter	Symbol	Min	Typ	Max	Units	Ref fig
SCLK Frequency	$1/t_{PSCLK}$			4	MHz	Fig4
SCLK Pulse Width High	t_{WSH}	40			ns	
SCLK Pulse Width Low	t_{WSL}	40			ns	
CS(bar) Pulse Width Low	t_{WCL}	16			SCLK	
Hold Time: SCLK High to CS(bar) Low	t_{HCS}	80			ns	
Setup Time: CS Low to SCLK High	t_{SCS}	40			ns	
Rising Time: CS(bar),SCLK	t_R			100	ns	
Falling Time: CS(bar),SCLK	t_F			100	ns	
W R I T E						
Setup Time: DATA to SCLK High	t_{SDC}	40			ns	Fig4
Hold Time: SCLK High to DATA	t_{HDC}	40			ns	
Hold Time: SCLK Low to CS(bar) High	t_{HCS2}	0			ns	
R E A D						
Delay Time: SCLK Low to DATA pin drive	t_{DDD}	0			ns	Fig5
Delay Time: SCLK Low to DATA valid	t_{DVD}			60	ns	
Delay Time: SCLK Low to DATA High-Z	t_{DZSD}	0		60	ns	Fig6
Delay Time: CS High to DATA High-Z	t_{DZCD}	0		60	ns	
CS(bar) Pulse Width High	t_{WCH}	40			ns	

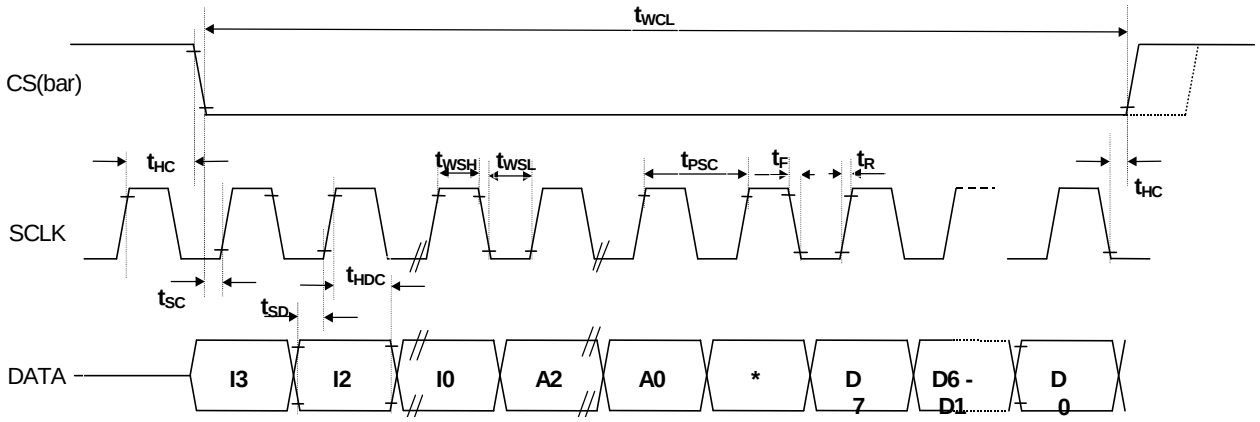


Fig4 Serial Interface Timing <WRITE>

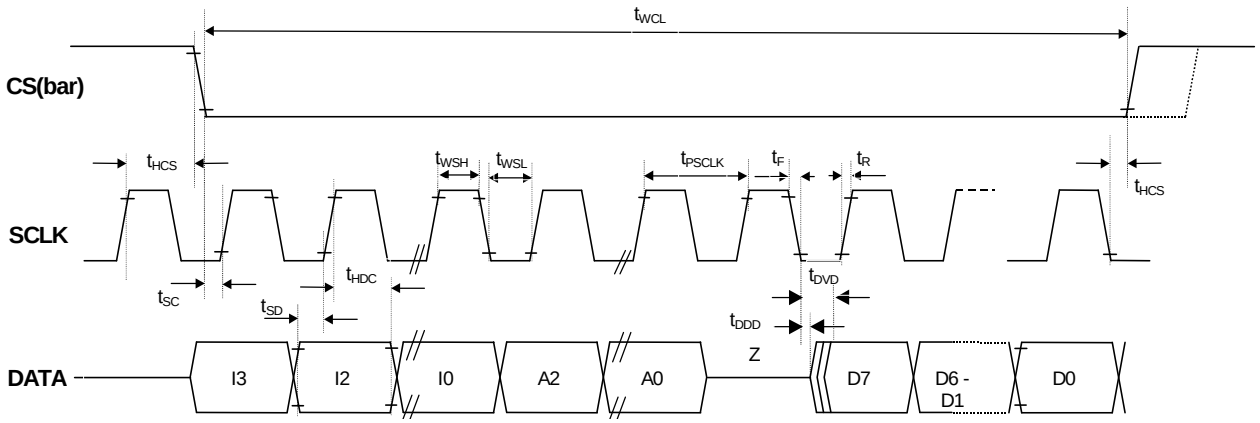


Fig5 Serial Interface Timing <READ>

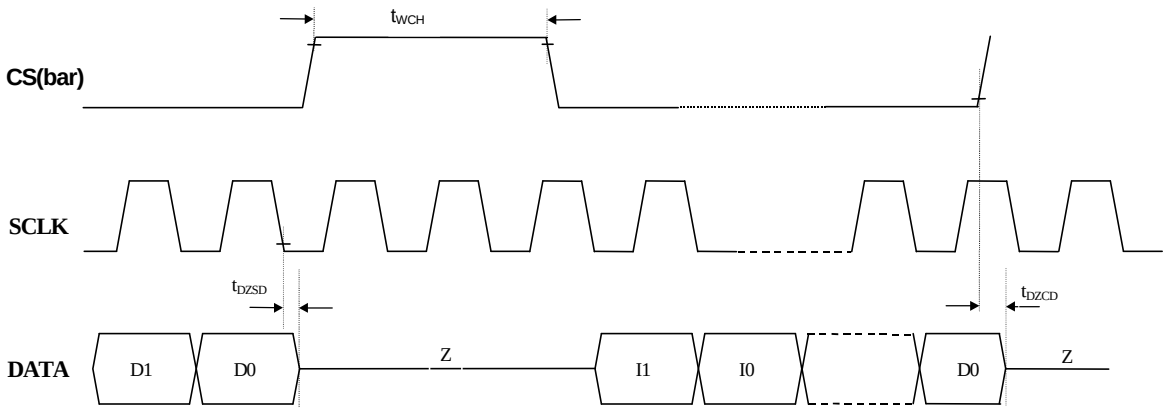
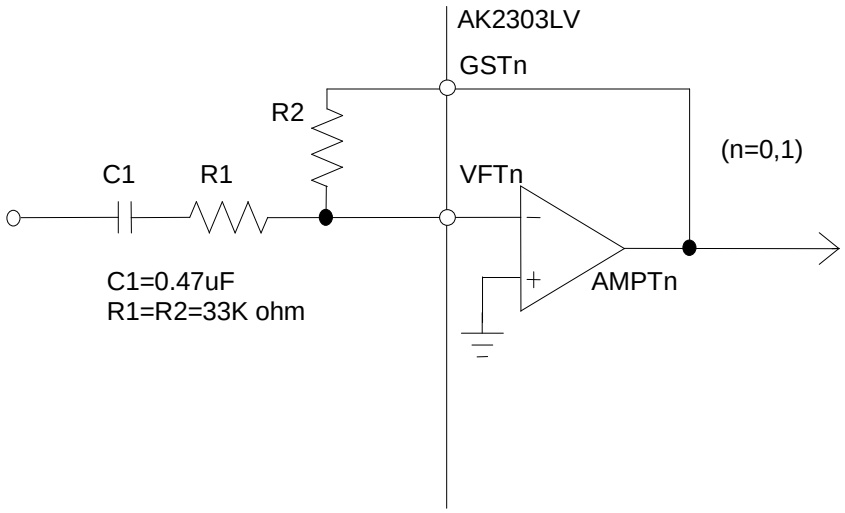


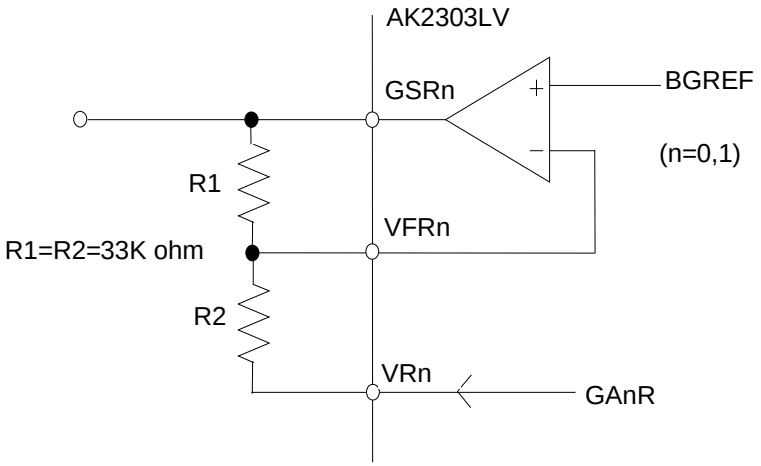
Fig6 Serial Interface Timing <READ>

APPLICATION CIRCUIT EXAMPLE

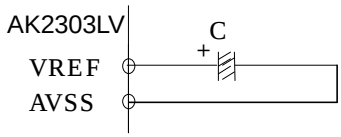
Analog input circuit(AMPT0,1)
AK2303LV has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment. Op-amp can be used as an inverting amplifier. Feedback resistor must be 10kΩ or larger.



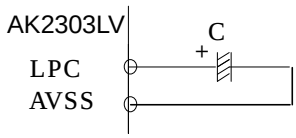
Analog output circuit(AMPR0,1)
AK2303LV has an op-amp at analog output stage of each channel to consist in an inverting amplifier for a gain adjustment of 0dBm0 level. Feedback resistor must be 10kΩ or larger.



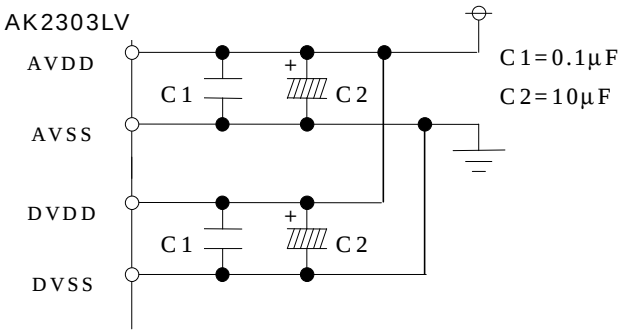
Analog ground stabilization capacitor
An external capacitor of more than 1.0uF should be connected between VREF and VSS to stabilize analog ground (VREF).



PLL Loop filter capcitor
An external capacitor of more than 0.22uF should be connected between LPC and VSS.



Power Supply
To attenuate the power supply noise, connect capacitors between VDD and VSS, as shown below.



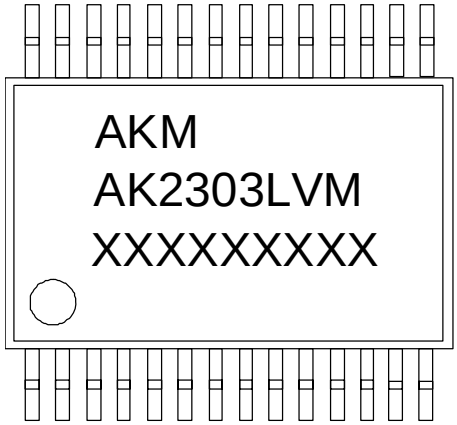
PACKAGE INFORMATION

- 28pin SSOP

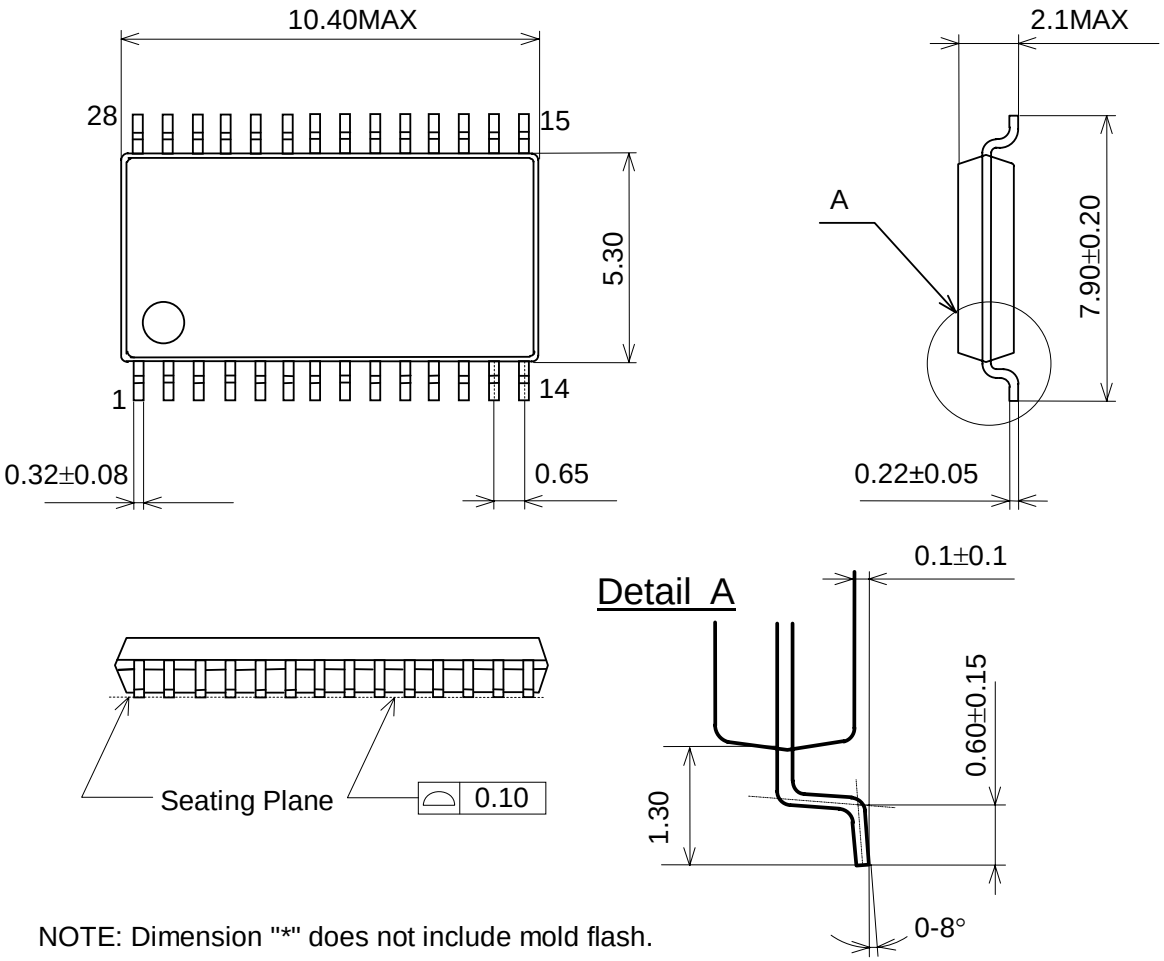
Marking

XXXXXXXXX: Date Code Identifier (9 digits)

AK2303LV



28pin SSOP (Unit: mm)



NOTE: Dimension "*" does not include mold flash.

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
11/10/17	01	Specification Change	1, 39, 40	Package Change: (28pin VSOP) → (28pin SSOP) Marking diagram was changed. Package drawing was changed.
12/01/25	02	Error Correction	39	PACKAGE INFORMATION Marking diagram was changed

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