= Preliminary =

AK2401A

Direct Conversion Transceiver

1. General Description

The AK2401A is a direct conversion transceiver that provides high performance narrow-band radio communication. The receiver block of the AK2401A integrates a LNA, I/Q demodulator, PGA and 24-bit delta-sigma ADC, and realizes both performances of high sensitivity and high tolerance to adjacent channel interference, intermodulation and blocking. Digital filter that is able to support channel selection for multiple radio systems, enabling simple system designing for a radio platform. The AK2401A also integrates a delta-sigma Fractional-N synthesizer that composes a high performance PLL with an external VCO. The transmission block has a DAC and a driver amplifier. The AK2401A is housed in a small QFN package (7mm x 7mm), realizing to downsize wire-less applications.

2. Features

- ☐ Operating Frequency: 29MHz ~ 1200MHz
- ☐ Power Supply: 2.7 ~ 3.3V (CPVDD, DACVDD: 2.7 ~ 5.5V, DVDD : 1.7 ~ 1.9V or 2.7 ~ 3.3V)
- ☐ Operational Temperature: -40 ~ +85ºC
- ☐ LNA: Gain 15dB, NF 1.2dB, IIP3 +7dBm
- ☐ High Linearity Direct Conversion I/Q Demodulator
- ☐ 24-bit ΔΣ A/D Converter: up to 150kHz Output Sampling Frequency (TCXO=19.2MHz)
- ☐ Band Changeable Digital Filter (Bandwidth can be set arbitrarily)
- ☐ Automatic Gain Control (AGC) function for LNA and PGA
- ☐ Real-time DC Offset Canceller (RDOC) Function
- ☐ RSSI Function: Data read by SPI communication
- ☐ 18-bit ΔΣ Fractional-N PLL Synthesizer
- ☐ Digital Frequency Modulation (FM/FSK) by Frequency Offset Function
- ☐ Fast Lock Function reduces Lock-up Time
- ☐ 12-bit D/A Converter: 200kHz Max. Sampling Frequency, S/N 72dB
- ☐ Transmission Driver Amplifier: −6 ~ +6 dBm Output
- ☐ Local Signal Dividing Circuit
- ☐ TCXO Frequency: 18.432MHz / 19.2MHz are recommended
- ☐ Frequency: 52-pin QFN (7×7×0.85mm 0.4 mm pitch)

3. Application

- Narrow Band Radio Communication: 6.25kHz/7.5kHz/12.5kHz/15kHz/20kHz/25kHz/ 50kHz/100kHz/150kHz / etc.
- Modulation Method: FM/2FSK/4FSK/QPSK/π/4 DQPSK /16QAM/64QAM
  (Modulation / demodulation needs to be done externally. Modem function is not installed.)
- Analog/Digital Dual Mode Transceiver
- Digital Radio System for Industrial Use
- Public safety and Community/Emergency Radio System
- Convenience Transceiver
- Marine/Mobile Communication System
- Low power / Telemeter Transmitter
- Amateur Radio System

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5. Block Diagram and Functions

5.1. Block Diagram

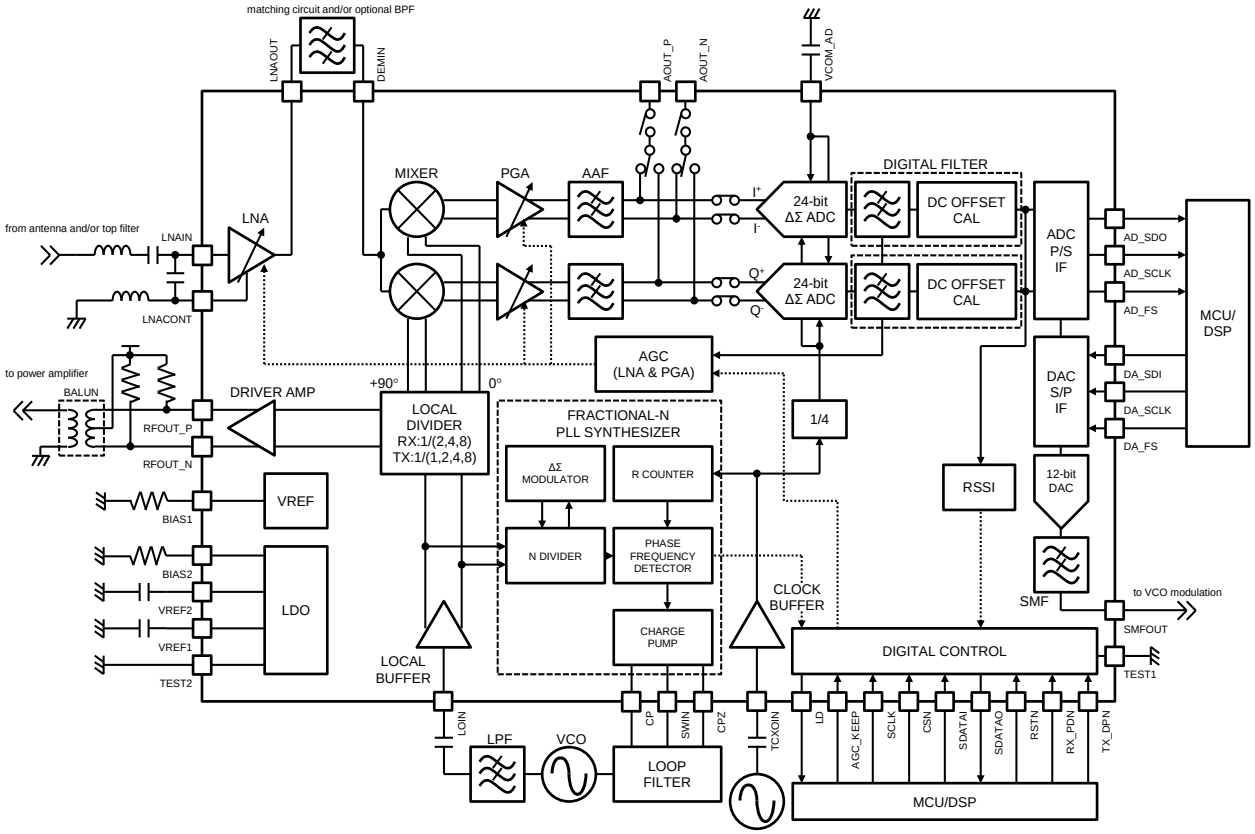


Figure 1. AK2401A Block Diagram

5.2. Functions

The AK2401A consists of the Analog Receiving Circuit 1 (LNA), the Analog Receiving Circuit 2 (MIXER, PGA and AAF), the Digital Receiving Circuit (ADC, DIGITAL FILTER, RSSI, AGC and ADC P/S IF), the Local Oscillation Circuit (PLL SYNTHESIZER, LOCAL BUFFER, LOCAL DIVIDER and CLOCK BUFFER), the Transmitting Data Generation Circuit (DAC S/P IF, DAC and SMOOTHING FILTER), the Transmitting Pre-amplifier Circuit (DRIVER AMP), the Reference Voltage Generation Circuit (VREF), the Internal Low Voltage Generation Circuit (LDO) and the Digital Control Circuit (DIGITAL CONTROL).

- Analog Receiving Circuit 1 (LNA: Low Noise Linear Amplifier)
  Amplify received RF signal in low noise. An automatic gain controlling (AGC) function that automatically switches operation mode according to the input signal level is implemented to prevent degradation of distortion characteristics in strong input environment. An external matching circuit is needed at input/output of the LNA. An external filter can be added between the LNA and the MIXER blocks depending on the Image suppression characteristic demands.

- Analog Receiving Circuit 2 (MIXER, PGA, AAF)
  The direct conversion type MIXER down coverts RF signal that is amplified by LNA. The MIXER is operated by two local signals with 90 degrees phase difference, and it generates Ich/Qch baseband signal. A matching circuit is necessary at the MIXER input. The PGA (programmable gain amplifier) is composed by a first-order low-pass filter that is able to change the gain by register settings. It amplifies the dynamic range by keeping the input level of the ADC after this block. The PGA has an AGC function that changes PGA gain automatically according to input signal level. The AAF is composed by a third-order low-pass filter (F_c=100kHz). It is an anti-aliasing filter that prevents aliasing at the ADC after this block. An analog filter is composed by the PGA and the AAF reducing blocking signals on ADC input.

- Digital Receiving Circuit (ADC, DIGITAL FILTER, RSSI, AGC, ADC P/S IF)
  The 24-bit delta-sigma A/D converter converts an analog baseband signal that is generated at the analog receiving circuit to a digital baseband signal. The digital filter is composed by a decimation filter and a channel filter for removing adjacent channel interference and blocking. The channel filter is selected from 10 types standard channel filters that have different frequency characteristics and FIR filter that can be set the coefficient arbitrary. The narrowest pass band of the standard channel filters is 2 kHz and the widest is 60 kHz. The output sampling frequency differs depending on the type of selected channel filter, and it will be 150 kHz at maximum when using a 19.2 MHz reference clock. A DC OFFSET CAL block is composed of a real-time DC offset canceller (RDOC) and a DC offset calibrator. It cancels DC offset that is superimposed to a baseband signal. The RSSI outputs a signal-strength level of the DC OFFSET CAL output. It can be confirmed by register read on SPI. The parallel interface for ADC outputs digital baseband signals.

- Local Generation Circuit (PLL SYNTHESIZER, LOCAL BUFFER, LOCAL DIVIDER, CLOCK BUFFER)
  The FRACTIONAL-N PLL is composed by a PLL SYNTHESIZER, external LOOP FILTER and VCO. It generates a local frequency signal by multiplying the reference clock from the TCXOIN pin by “N”, and converts to a local frequency by dividing the signal by “N” (N=2, 4, 8) at LOVAL DIVIDER. At the same time, two local signals that have 90 degree phase difference are generated.

- Transmitting Data Generation Circuit (DAC S/P IF, DAC, SMF)
  The 12-bit DA converter converts a digital baseband signal that is input to a serial/parallel interface for DAC to an analog baseband signal. The SMF (SMOOTHING FILTER) is a low-pass filter (fc=20kHz) that smoothing the DAC output. These circuits are used for generating an audio signal of transmission and connected to voltage control pin of an external VCO. In other case, it is able to be used as a general purpose 12-bit DAC.

- Transmitting Pre-amplifier Circuit (DRIVER AMP)
  This circuit amplifies a signal that is divided by “N” by the LOCAL DIVIDER and outputs. It is assumed to use as a transmitting signal output when modulating the signal directly by an external VCO.

- Reference Voltage Generation Circuit (VREF)
  Generate reference voltage for each block.

- Internal Low Voltage Generation Circuit (LDO)
  Generate a 1.9V power from external 3V power (SYNVDD). This internal power supply is supplied to the digital receiving circuit, the digital control circuit and a part of local oscillation circuit.

- Digital Control Circuit (DIGITAL CONTROL)
  - Register Write/Read by 4-wire Serial Interface (CSN, SCLK, SDATAI, SDATAO pins)
  - Hardware Reset Signal Input (RSTN pin)
  - AGC Function Control Signal Input (AGC_KEEP pin)
  - PLL Status Output (LD pin)
  - Power Management by Pins (RX_PDN, TX_PDN pins)

6. Pin Configurations and Functions

6.1. Pin Configurations

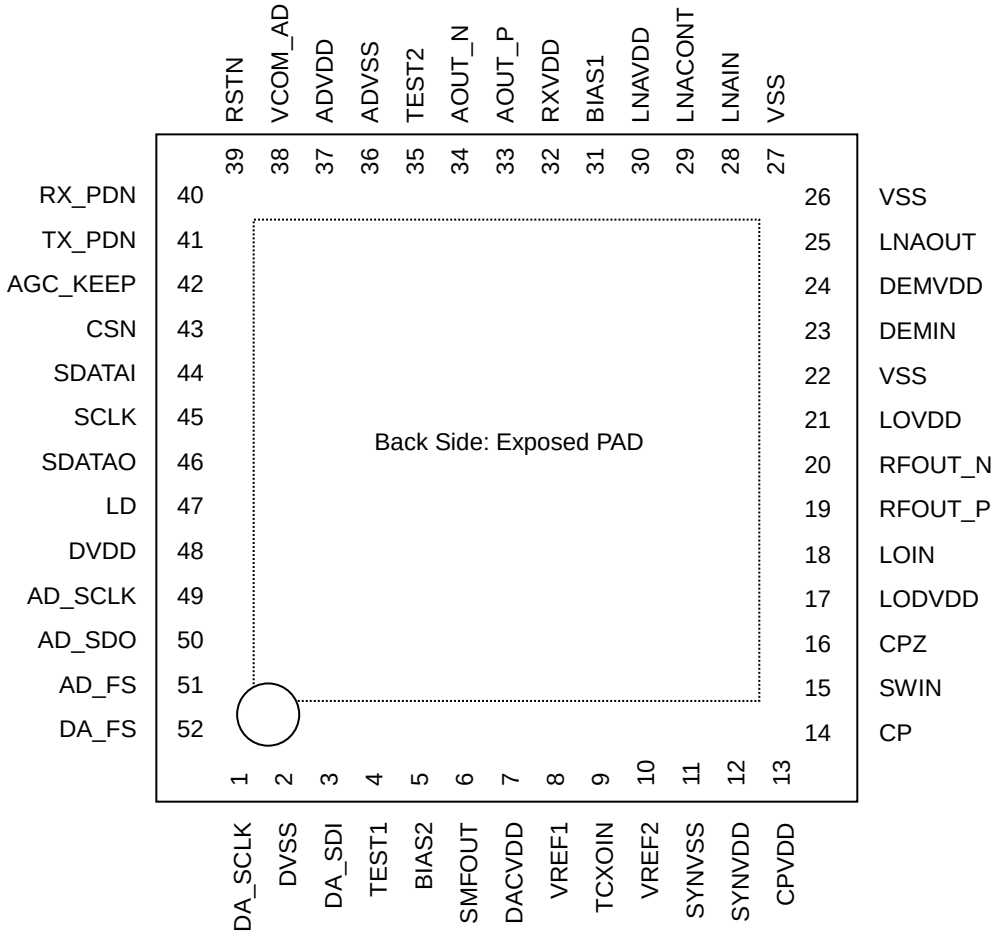


Figure 2. Pin Configurations (52-pin QFN0707, Top View)

6.2. Pin Functions

AI: Analog Input Pin, AO: Analog Output Pin, DI: Digital Input Pin, DO: Digital Output Pin,
P: Power Supply Pin, G: Ground Pin
All digital input pins must not be allowed to float.

No.	Pin Name	Type	PD Status	Function
1	DA_SCLK	DI	Hi-Z	Serial Data Clock Input for D/A Converter
2	DVSS	G	-	Digital Ground for Interface Circuit.
3	DA_SDI	DI	Hi-Z	D/A Converter Serial Data Input
4	TEST1	DI	100kΩ Pull down	Test Pin. Connect to VSS.
5	BIAS2	AI	-	Resistance Pin for setting charge pump output current
6	SMFOUT	AO	Hi-Z	Smoothing Filter Output
7	DACVDD	P	-	Analog Power Supply for D/A Converter
8	VREF1	AO	-	LDO Reference Connect a capacitor to stabilize LDO reference voltage
9	TCXOIN	AI	27kΩ Pull down	Reference Clock Input
10	VREF2	AO	-	Reference Voltage Pin Connect a capacitor to stabilize reference voltage.
11	SYNVSS	G	-	Analog Ground for Synthesizer
12	SYNVDD	P	-	Analog Power Supply for Synthesizer
13	CPVDD	P	-	Analog Power Supply for Charge Pump
14	CP	AO	Hi-Z	Charge Pump Output
15	SWIN	AI	* 1	Connect a resistor for Fast Lock
16	CPZ	AI	* 1	Connect a capacitor for Loop Filter
17	LODVDD	P	-	Analog Power Supply for Local Divider and Local Buffer
18	LOIN	AI	50Ω Pull down	Local Input
19	RFOUT_P	AO	Hi-Z * 2	Driver Amplifier Positive Output
20	RFOUT_N	AO	Hi-Z * 2	Driver Amplifier Negative Output
21	LOVDD	P	-	Analog Power Supply for Local Amplifier and Driver Amplifier
22	VSS	G	* 3	Ground
23	DEMIN	AI	H-Z	MIXER Input
24	DEMVDD	P	-	Analog Power Supply for MIXER
25	LNAOUT	AO	Hi-Z * 2	LNA Output
26	VSS	G	* 3	Ground
27	VSS	G	* 3	Ground
28	LNAIN	AI	100kΩ Pull down	LNA Input
29	LNACONT	AI	Hi-Z	LNA Matching Adjustment Pin
30	LNAVDD	P	-	Analog Power Supply for LNA
31	BIAS1	AI	Hi-Z	Connect a resistor for current adjustment
32	RXVDD	P	-	Analog Power Supply for PGA, AAF and VREF
33	AOUT_P	AO	Hi-Z	RX Positive Analog Output
34	AOUT_N	AO	Hi-Z	RX Negative Analog Output
35	TEST2	DI	100kΩ Pull down	Test Pin. Connect to VSS.
36	ADVSS	G	-	Ground for A/D converter
37	ADVDD	P	-	Analog Power Supply for A/D converter
38	VCOM_AD	AO	VSS	Connect a capacitor to stabilize reference voltage for A/D converter

39	RSTN	DI	Hi-Z	Hardware Reset Pin
40	RX_PDN	DI	Hi-Z	Power Down Pin for Receiving Block
41	TX_PDN	DI	Hi-Z	Power Down Pin for Transmitting Block
42	AGC_KEEP	DI	Hi-Z	AGC ON/OFF Control Pin
43	CSN	DI	Hi-Z	Register Serial Data Chip Select Pin
44	SDATAI	DI	Hi-Z	Register Serial Data Input
45	SCLK	DI	Hi-Z	Register Serial Data Clock Input
46	SDATAO	DO	Low	Register Serial Data Output
47	LD	DO	Low	Lock Detection Output Pin
48	DVDD	P	-	Digital Power Supply for Interface Circuit
49	AD_SCLK	DO	Low	Clock Output for A/D converter Serial Data
50	AD_SDO	DO	Low	Serial Data Output for A/D Converter
51	AD_FS	DO	Low	Frame Synchronized Output for A/D Converter Serial Data
52	DA_FS	DI	Hi-Z	Frame Synchronized Input for D/A Converter Serial Data
-	TAB	G	-	Exposed pad on the bottom surface of the package should be connected to VSS.

Notes:
* 1. When PD_SYNTH_N bit = “0”, the switch of loop filter selector is OFF.
* 2. Power supply must be supplied via an inductor since this pin is open drain/corrector pin.
* 3. Internally connected to the TAB.

7. Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage	LNAVDD pin, DEMVDD pin, ADVDD pin , SYNVDD pin, LODVDD pin, LOVDD pin, RXVDD pin	VDD1	-0.3	+6.5	V
	DACVDD pin	DACVDD	-0.3	+6.5	V
	CPVDD pin	CPVDD	-0.3	+6.5	V
	DVDD pin	DVDD	-0.3	+6.5	V
Ground Level * 4		VSS	0	0	V
Applied Analog Input Voltage		V_{AIN}	-0.3	VDD1+0.3 DACVDD+0.3 CPVDD+0.3	V
Applied Digital Input Voltage		V_{DIN}	-0.3	DVDD+0.3	V
Applied Input Current (except Power Supply pins)		I_{IN}	-10	+10	mA
Maximum LNAIN Input Level * 5		V_{LNAIN}		2.4	Vpp
Maximum DEMIN Input Level	DEMIN Input < 100MHz	DEMPOW1		+15	dBm
	DEMIN Input ≥ 100MHz	DEMPOW2		+10	dBm
Maximum LOIN Input Level		LOPOW		+14	dBm
Storage Temperature Range		T_{stg}	-55	125	ºC

Note:
* 4. VSS, SYNVSS, DVSS and ADVSS pins. All voltages are with respect to ground (VSS).
* 5. AC level that does not include DC bias in LNAIN pin.
* Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature Range	Ta	-40		85	ºC
Power Supply Voltage	VDD1	2.7	3.0	3.3	V
	DACVDD	2.7	5.0	5.5	V
	CPVDD	2.7	5.0	5.5	V
	DVDD* 6	2.7	3.0	3.3	V
		1.7	1.8	1.9	

Note:
* 6. DVDD is power supply for interface circuits.
If DVDD=2.7~3.3V, <Address0x4A> DO_MODE bit=”0”;
If DVDD=1.7~1.9V, <Address0x4A> DO_MODE bit=”1”.

9. Digital Characteristics

9.1. DC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage	* 7	V_{IH}	0.8DVDD			V
Low Level Input Voltage	* 7	V_{IL}			0.2DVDD	V
High Level Input Current	V_{IH}=DVDD, * 7	I_{IH1}			+10	µA
	V_{IH}=DVDD, * 8	I_{IH2}	+9	+33	+66	µA
Low Level Input Current	V_{IL}=0V, * 7	I_{IL1}	-10			µA
	V_{IL}=0V, * 8	I_{IL2}	-10			µA
High Level Output Voltage	I_{OH}=+0.2mA * 9	V_{OH}	DVDD-0.4		DVDD	V
Low Level Output Voltage	I_{OL}=-0.4mA * 9	V_{OL}	0.0		0.4	V

Regarding the input current, the direction in which the current flows into the IC is defined as + and the direction in which the current flows out from the IC is defined as -.

Notes:
* 7. RSTN, CSN, SDATAI, SCLK, DA_SCLK, DA_SDI, DA_FS, AGC_KEEP, RX_PDN and TX_PDN pins
* 8. TEST1 and TEST2 pins
* 9. SDATAO, LD, AD_SCLK, AD_SDO and AD_FS pins

10. Analog Characteristics

Specifications that are guaranteed by design are not tested.

10.1. Receiving Characteristics

VDD1= 2.7 ~ 3.3V, DACVDD=2.7 ~ 5.5V, CPVDD=2.7 ~ 5.5V,
DVDD= 1.7 ~ 1.9V or 2.7 ~ 3.3V, Ta= -40 ~ 85ºC,
LNA Input=MIXER RF Input=450MHz, LOIN Input=900MHz, <Address0x12>DIVSEL[1:0] bits="01" (Divide by 2), Normal Gain Mode; Unless otherwise specified

10.1.1. LNA

Parameter		Min.	Typ.	Max.	Unit	Description
Operating Frequency Range		29		1200	MHz	
Gain	Normal Power Mode	12	15	18	dB	Normal Gain Mode
	Low Power Mode	12	15	18	dB	
	Normal Power Mode	3	6	9	dB	Low Gain Mode LNA Input=-10dBm
	Low Power Mode	3	6	9	dB	
Noise Figure	Normal Power Mode		1.2	1.8	dB	Guaranteed by Design
	Low Power Mode		1.2	1.8	dB	
IIP3	Normal Power Mode	2	7		dBm	450.025MHz & 450.047MHz Input Observed 450.003MHz
	Low Power Mode	-7	-2		dBm	

10.1.2. MIXER+PGA+AAF+ADC

I channel and Q channel are specified independently.

Maximum PGA Gain:
I Channel: <Address0x15>PGAGAIN_I[5:0] bits="000000"(+28dB)
Q Channel: <Address0x16>PGAGAIN_Q[5:0] bits="000000"(+28dB)
Middle PGA Gain:
I Channel: <Address0x15>PGAGAIN_I[5:0] bits= "011100"(0dB)
Q Channel: <Address0x16>PGAGAIN_Q[5:0] bits= "011100"(0dB)
Minimum PGA Gain:
I Channel: <Address0x15>PGAGAIN_I[5:0] bits="110000"(-20dB)
Q Channel: <Address0x16>PGAGAIN_Q[5:0] bits="110000"(-20dB)

Parameter		Min.	Typ.	Max.	Unit	Description
Operating Frequency Range		29		1200	MHz	
Max. Gain	Normal Power Mode		42		dB	
	Low Power Mode		41		dB	
Min. Gain	Normal Power Mode		-6		dB	
	Low Power Mode		-7		dB	
Gain Control Range			48		dB	
Gain Control Step		0.7	1	1.3	dB	
Noise Figure	Normal Power Mode		16	20	dB	
	Low Power Mode		17	21	dB	Maximum PGA Gain * 10

IIP3	Normal Power Mode		15	19		dBm	Middle PGA Gain 25kHz & 47kHz offset Observed 3kHz
	Low Power Mode		7	11		dBm	
IIP2 (In-band)	Normal Power Mode		55	76		dBm	Middle PGA Gain 5.25kHz & 7.25kHz offset Observed 2kHz
	Low Power Mode		55	76		dBm	
IIP2 (Out-band)	Normal Power Mode		53	72		dBm	Maximum PGA Gain 1MHz & 1.002MHz offset Observed 2kHz
	Low Power Mode		53	72		dBm	
Input P1dB	Normal Power Mode		-28	-22		dBm	Maximum PGA Gain
	Low Power Mode		-28	-22		dBm	
Local Leak@DEMIN pin				-90		dBm	LOIN Input=0dBm
I/Q Gain Imbalance					0.5	dB	
I/Q Phase Imbalance					1	deg	LOIN Input=0dBm
Frequency Attenuation Characteristics (Normalized at 1kHz) Low Cutoff Mode * 11		10kHz	-1	0	+1	dB	Maximum PGA Gain
		100kHz	-18	-9	-3	dB	
		1MHz	-97	-86	-75	dB	
		10kHz	-1	0	+1	dB	Middle PGA Gain
		100kHz	-9	-2	-1	dB	
		1MHz	-72	-62	-52	dB	
		10kHz	-1	0	+1	dB	Minimum PGA Gain
		100kHz	-9	-2	+1	dB	
		1MHz	-68	-60	-50	dB	
Frequency Attenuation Characteristics (Normalized at 1kHz) High Cutoff Mode * 11		10kHz	-1	0	+1	dB	Maximum PGA Gain
		100kHz	-14	-5	0	dB	
		1MHz	-91	-81	-69	dB	
		10kHz	-1	0	+1	dB	Middle PGA Gain
		100kHz	-9	-1.6	+1	dB	
		1MHz	-69	-60	-50	dB	
		10kHz	-1	0	+1	dB	Minimum PGA Gain
		100kHz	-9	-2	+1	dB	
		1MHz	-68	-59	-50	dB	

Notes:
* 10. Calculated from an integration value of 300Hz~4kHz output noise.
* 11. Frequency Attenuation Characteristics means MIXER+PGA+AAF. It does not include ADC characteristics.

10.1.3. LOCAL BUFFER+LOCAL DIVIDER (RX)

Parameter		Min.	Typ.	Max.	Unit	Description
LOIN Input Sensitivity		-5	0	5	dBm	
Output Frequency Range	2 div	50		1200	MHz	3levels by <Address0x12> DIVSEL[1:0] bits
	4 div	29		600	MHz	
	8 div	29		300	MHz	

10.1.4. PLL SYNTHESIZER

BIAS2 pin=27kΩ

Parameter	Min.	Typ.	Max.	Unit	Description
N DIVIDER					
Operating Frequency Range	100		2400	MHz	High Frequency Mode
	100		1200	MHz	Low Frequency Mode
CLOCK BUFFER					
TCXOIN Input Sensitivity	0.4		2	Vpp	* 12
Operating Frequency Range	10	19.2 or 18.432	25	MHz	
PHASE FREQUENCY DETECTOR(PFD)					
Phase Detector Frequency(F_{PFD})			25	MHz	
CHARGE PUMP(CP)					
CP Current Adjust	22	27	33	kΩ	Connect to BIAS2 pin
Maximum CP Current		2400		μA	32 levels by <Address0x0A, 0x0B>
Minimum CP Current		75		μA	
I_{CP} TRI-STATE Leak Current		1		nA	$0.6 \le V_{CPO} \le$ (CPVDD - 0.7) (V_{CPO}:CP pin Voltage)
Sink/Source Current Mismatch * 13			10	%	V_{CPO} = CPVDD/2 Ta = 25ºC
I_{CP} vs V_{CPO} * 14			15	%	$0.5 \le V_{CPO} \le$ (CPVDD - 0.5) Ta = 25ºC
NOISE CHARACTERISTICS					
Normalized Phase Noise		-210		dBc/Hz	* 15

Notes:

* 12. In the case of using a TCXO other than 18.432MHz/19.2MHz, the cutoff frequency of the standard channel filter change. Also note that the output sampling rate of the ADC is related to the TCXO frequency.
* 13. Sink/Source Current Mismatch: $[(|I_{SINK}|-|I_{SOURCE}|)/\{(|I_{SINK}|+|I_{SOURCE}|)/2\}]\times100$ [%]
* 14. I_{CP} vs V_{CPO}: $[\{1/2*(|I_1|-|I_2|)\}/\{1/2*(|I_1|+|I_2|)\}]\times100$ [%]
* 15. It is calculated by the following formula with measuring in-band phase noise when PLL loop is locked.
  TCXOIN=19.2MHz, F_{PFD}=19.2MHz
  ($PN_{TOTAL} = PN_{SYNTH} - 10 \text{ Log } F_{PFD} - 20 \text{ Log } N$)
  PN_{TOTAL}: Normalized Phase Noise, PN_{SYNTH}: In-band Phase Noise

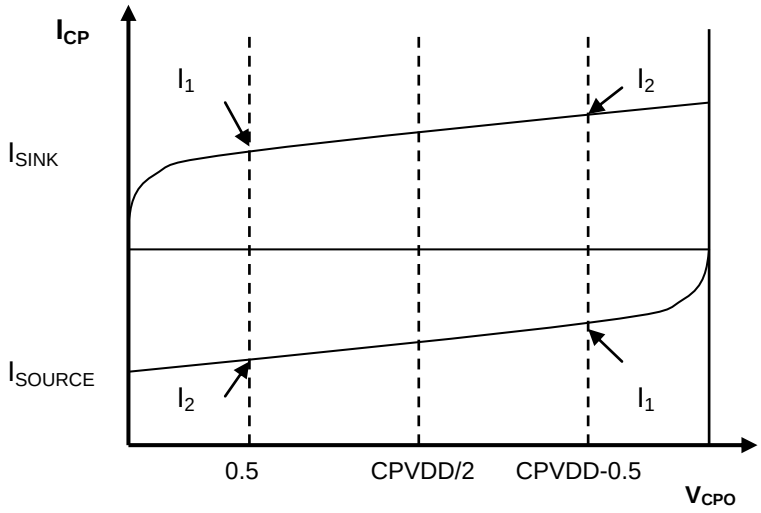


Figure 3. Charge Pump Characteristics - Voltage vs. Current

10.1.5. RSSI

Parameter		Min.	Typ.	Max.	Unit	Description
RSSI Output code <Address0x3A> RSSI[7:0] bits Read Back	LNA Input=-120dBm	0	14	28	Dec	Normal Gain Mode <Address0x1F> AGCOFF bit= “0” <Address0x2C> RSSI_LOW bit= “00”
	LNA Input=-50dBm	140	154	168	Dec	

10.2. Transmission Characteristics

VDD1=2.7 ~ 3.3V, DACVDD=2.7 ~ 5.5V, CPVDD=2.7 ~ 5.5V,
DVDD= 1.7 ~ 1.9V or 2.7 ~3.3V, Ta = -40 ~ 85ºC, LOIN Input = 0dBm; Unless otherwise specified

10.2.1. DAC+SMF

Parameter		Min.	Typ.	Max.	Unit	Description
Resolution			12		bit	
Sampling Frequency				200	kHz	
Load Resistance (R_L)		10	100		kΩ	
Load Capacitance (C_L)			50	100	pF	
Output Level	Low Level Mode	1.1	1.3	1.5	Vpp	High Level Mode:4.5 ~ 5.5V Low Level Mode:2.7 ~ 5.5V RL= 100kΩ,CL= 50pF Integrated Noise BW : 300Hz ~ 48kHz, fs= 96kHz,fout= 1kHz sine Observed SMFOUT pin
	High Level Mode	2.9	3.1	3.3	Vpp	
Reference Level	Low Level Mode	1.3	1.4	1.5	V	
	High Level Mode	2.3	2.4	2.5	V	
S/N	Low Level Mode		72		dB	
	High Level Mode		72		dB	
SINAD	Low Level Mode		65		dB	
	High Level Mode		65		dB	
SMF Frequency Characteristics	@1kHz		0		dB	
	@20kHz		-4		dB	
	@100kHz		-44		dB	

10.2.2. LOCAL BUFFER+LOCAL DIVIDER(TX)+DRIVER AMP

Parameter		Min.	Typ.	Max.	Unit	Description
LOIN Input Sensitivity		-5	0	5	dBm	
Output Frequency Range	no div	100		1200	MHz	4levels by <Address0x12> DIVSEL[1:0] bits
	2 div	100		1200	MHz	
	4 div	100		600	MHz	
	8 div	100		300	MHz	
Output Power@450MHz			+6		dBm	4 levels by <Address0x13> TXOLV[1:0] bits
			+3		dBm	
			0		dBm	
			-6		dBm	

10.3. Current Consumption

VDD1= 2.7 ~ 3.3V, DACVDD= 2.7 ~ 5.5V, CPVDD= 2.7 ~ 5.5V,
DVDD= 1.7 ~ 1.9V or 2.7 ~ 3.3V, Ta=-40 ~ 85ºC; Unless otherwise specified
Current Consumption includes the drive current of the digital output pin.

■ Current Consumption of Each Function

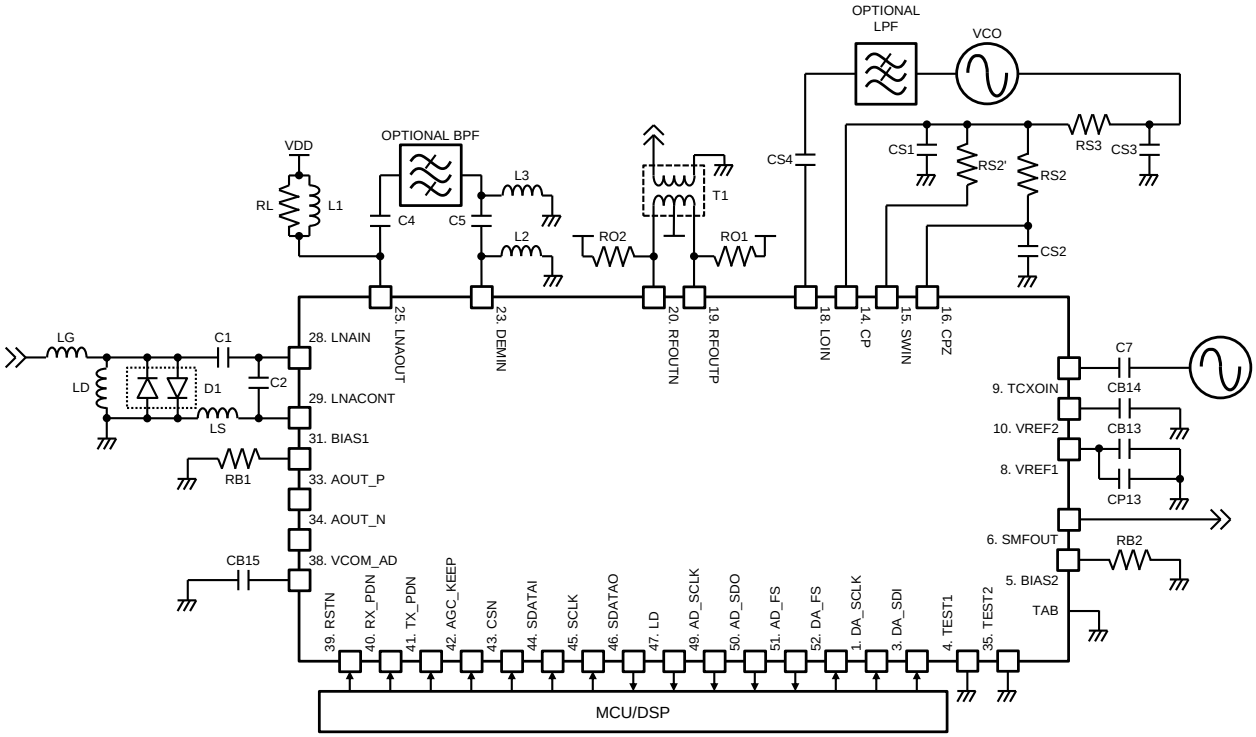
Parameter		Min.	Typ.	Max.	Unit	Description
BIAS CIRCUIT			1.7	2.2	mA	[10], [11]
PLL SYNTHESIZER	High Frequency Mode		15	20	mA	[5], [6]
	Low Frequency Mode		11	16	mA	
RX TOTAL (2 div)	Normal Power Mode		70	93	mA	[1], [2], [3], [5], [7], [8]
	Low Power Mode		52	70	mA	
TX TOTAL (2 div, 0dBm)			24	31	mA	[4], [7], [8], [9]

■ Current Consumption of Each Block (Guaranteed by Design)

Parameter		Min.	Typ.	Max.	Unit	Description
LNA	Normal Power Mode		14		mA	[1]
	Low Power Mode		4		mA	
MIXER+PGA+AAF	Normal Power Mode		35		mA	[2]
	Low Power Mode		27		mA	
ADC+DIGITAL			13		mA	[3]
CLOCK BUFFER			1		mA	[5]
LOCAL BUFFER			2.5		mA	[7]
LOCAL DIVIDER(RX)	2 div		4.5		mA	[8]
	4 div		5.5		mA	
	8 div		6.5		mA	
VREF			0.8		mA	[11]
DAC			5		mA	[4]
LOCAL DIVIDER(TX)	No div		2		mA	[7]
	2 div		3		mA	
	4 div		4		mA	
	8 div		5		mA	
DRIVER AMP	+6dBm		28		mA	[9]
	+3dBm		19		mA	
	0dBm		13.5		mA	
	-6dBm		7		mA	

11. Recommended External Circuits

11.1. Recommended External Circuits



11.2. List of Parts

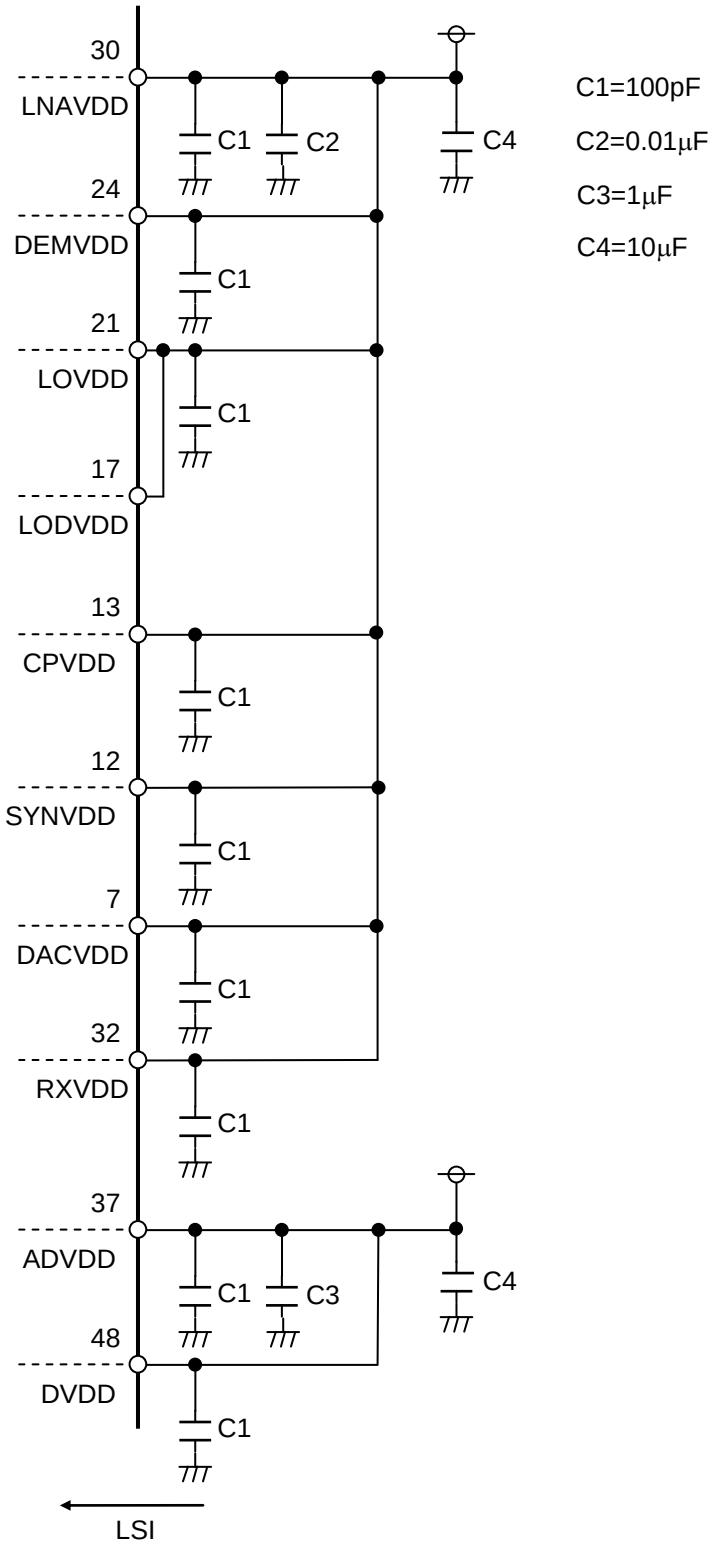
Table 1. Parts List for External Circuit Connection

Ref.	Value	Description	Ref.	Value	Description
LG	30nH	LNAIN=450MHz Normal Power Mode	T1	4:1	RFOUT=450MHz JTX-4-10T
LS	3.3nH		RO1	100Ω	
C2	3.6pF		RO2	100Ω	
C1	100pF		RS2	-	LOOP FILTER
LD	-		RS2’	-	
D1	-		RS3	-	
LG	47nH	LNAIN=450MHz Low Power Mode	CS1	-	
LS	3.3nH		CS2	-	
C2	1.3pF		CS3	-	
C1	100pF		CS4	1000pF	
LD	-		C7	100pF	
D1	-		CB13	10µF	
RL	200Ω	LNAOUT=450MHz	CP13	100pF	
L1	27nH		CB14	0.47µF	
C4	3.9pF		CB15	2.2µF	
L2	220nH	DEMIN=450MHz	RB1	47kΩ	±1% recommended
L3	22nH		RB2	27kΩ	±1% recommended
C5	20pF				

*Coil inductors are used.
*Matching circuit examples at frequencies other than 450 MHz are prepared as application notes. Contact us separately.
*DAN217UM is used for the diode LD.

11.3. Power Supply/Ground Pin

Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For a maximum effect, the capacitors should be located at the shortest distance between these pins.



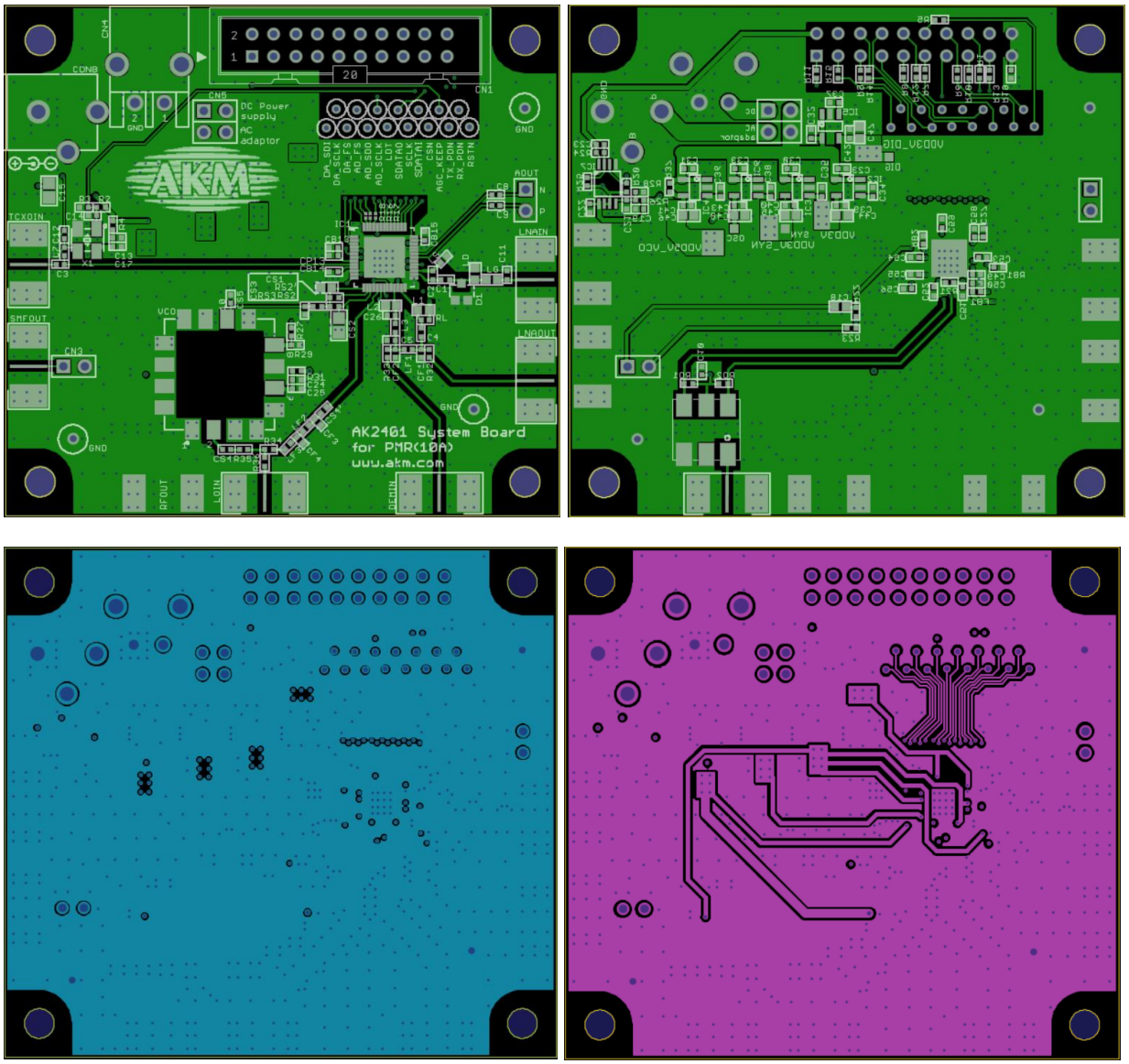
C1=100pF
C2=0.01μF
C3=1μF
C4=10μF

11.4. PCB Design

Below are board design guidelines confirmed by the conditions of our evaluation board and do not specify layout pattern of customer's board or guarantee the characteristics.

- Connect the exposed pad in the center of the back to the low impedance analog ground. If the exposed pad is not mounted, the operation may become unstable.
- The ADC is a 24-bit delta-sigma A/D converter. ADC operation clock is generated by dividing a reference clock that is input to the TCXOIN pin by four. For this reason, since (TCXO/4) MHz and its harmonic components leak to the input part of the LNA, selecting that frequency as the RF frequency causes suppression of receiver sensitivity. Therefore, if customer's RF frequency is equal to multiplied by (TCXO/4) MHz, evaluate its performance with customer's board. On our evaluation board we confirm that the suppression of receiver sensitivity will be relaxed by paying attention to the guidelines described below.
- Each VSS is not separated and connected to the same analog ground.
- Spurious characteristics are improved by short-circuiting the exposed pad and each VSS pin with the TOP layer of the PCB.
- Power supply pins need to be careful not to go around LNA because ADVDD/DVDD is the main spurious source. In addition to connecting a 100pF decoupling capacitor to each power supply pin, 0.01μF is added to LNAVDD and 1μF is added to ADVDD. Be careful with the isolation between the digital signal line of AD_SCLK and the power supply line of LNAVDD.
- Each power supply pin is wired in low impedance from LDO etc. without connecting ferrite beads in series. Improvement of spurious characteristics may be occurring by connecting 1Ω in series only for LNAVDD.
- Spurious characteristics degrade due to high frequency noise of AD_SCLK, AD_SDO, AD_FS pins. Put 100Ω damping resistance in series. Fill the digital signal line in the inner layer.
- Connect decoupling capacitors, especially small capacitance ceramic capacitors as closely as possible to AK2401A.
- Use a balun connected to RFOUT_P, RFOUT_N pins depending on the frequency band. Because it is an open collector pin, when using a balun without a center tap, it is necessary to supply the power supply voltage separately through an inductor.
- For VREF1, VREF2 pins capacitor connected to ground, stabilize the internal circuit, connect the specified value.
- All digital input pins must not be allowed to float.

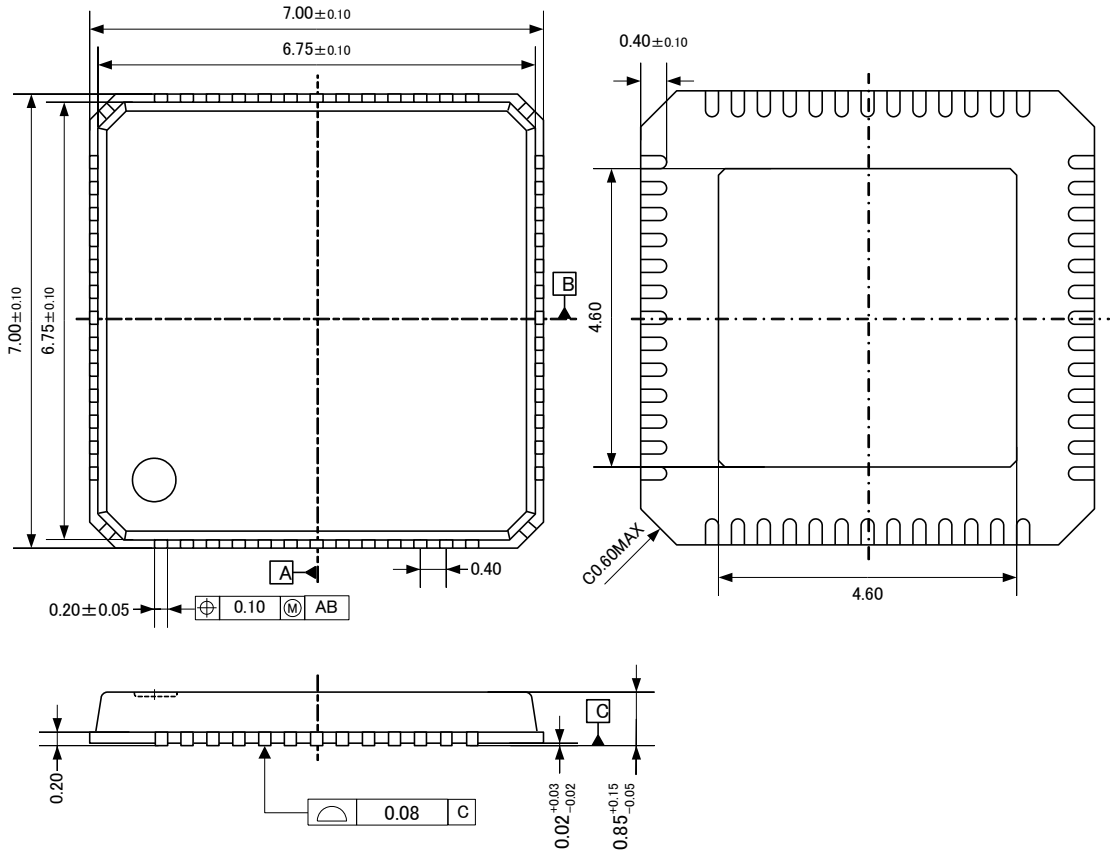
11.5. PCB Layout



12. Package

12.1. Outline Dimensions

52-pin QFN (Unit: mm)



*The exposed pad on the bottom surface of the package must be connected to VSS.

12.2. Marking

a: Product number : AK2401A
b: Date code : XXXXXXX
c: 1 pin marking: ●
d: Style : QFN
e: Number of pins : 52

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