AK4223

6:2 Audio Switch and 6:2 Video Switch

GENERAL DESCRIPTION

The AK4223 is an AV switch with 6:2 audio and 6:2 video switches. High performances with low power consumption are achieved by CMOS process. Integrated differential input circuits in audio and video blocks can separate the external ground noise. In audio block, a differential input circuit, audio LPF and 0dB/-6dB gain amplifier are integrated eliminating the needs for external LPF for audio outputs. In video block, an input clamp circuit, 6dB amplifier and video driver are integrated, and they also eliminate the need for external circuits. The AK4223 is offered in a space saving small 48-pin LQFP package, ideal for car navigation applications.

FEATURES

1. Audio Section
- **Selector with 6 inputs and 2 outputs**
- **Differential Input Circuit for Ground Noise Canceling**
- **LPF Circuit for Audio signals**
- **Output Gain Control: 0dB ~ - 6dB, -1dB Step**
- **S/(N+D): 90dB (@0dBV)**
- **Dynamic Range: 94dB**
- **Channel-Independent Mute Function**

2. Video Section
- **Selector with 6 inputs and 2 outputs**
- **Six Composite Signal Inputs**
- **On-Chip Sync-tip Clamp Circuit**
- **Video Drivers for Composite Signal Output (+6dB/+3dB/0dB/-3dB)**
- **Output Gain Control: -1dB ~ +1dB, 0.1dB Step**
- **LPF Circuit for Video signals (Bandwidth: 6MHz)**
- **S/N: 65dB**
- **Channel-Independent Mute Function**

3. Control Section
- **Serial µP I/F (I^2C)**

4. Power Supply: 7.5V ~ 9.5V

5. Ta = -40 ~ 85 °C

6. Package: 48pin LQFP

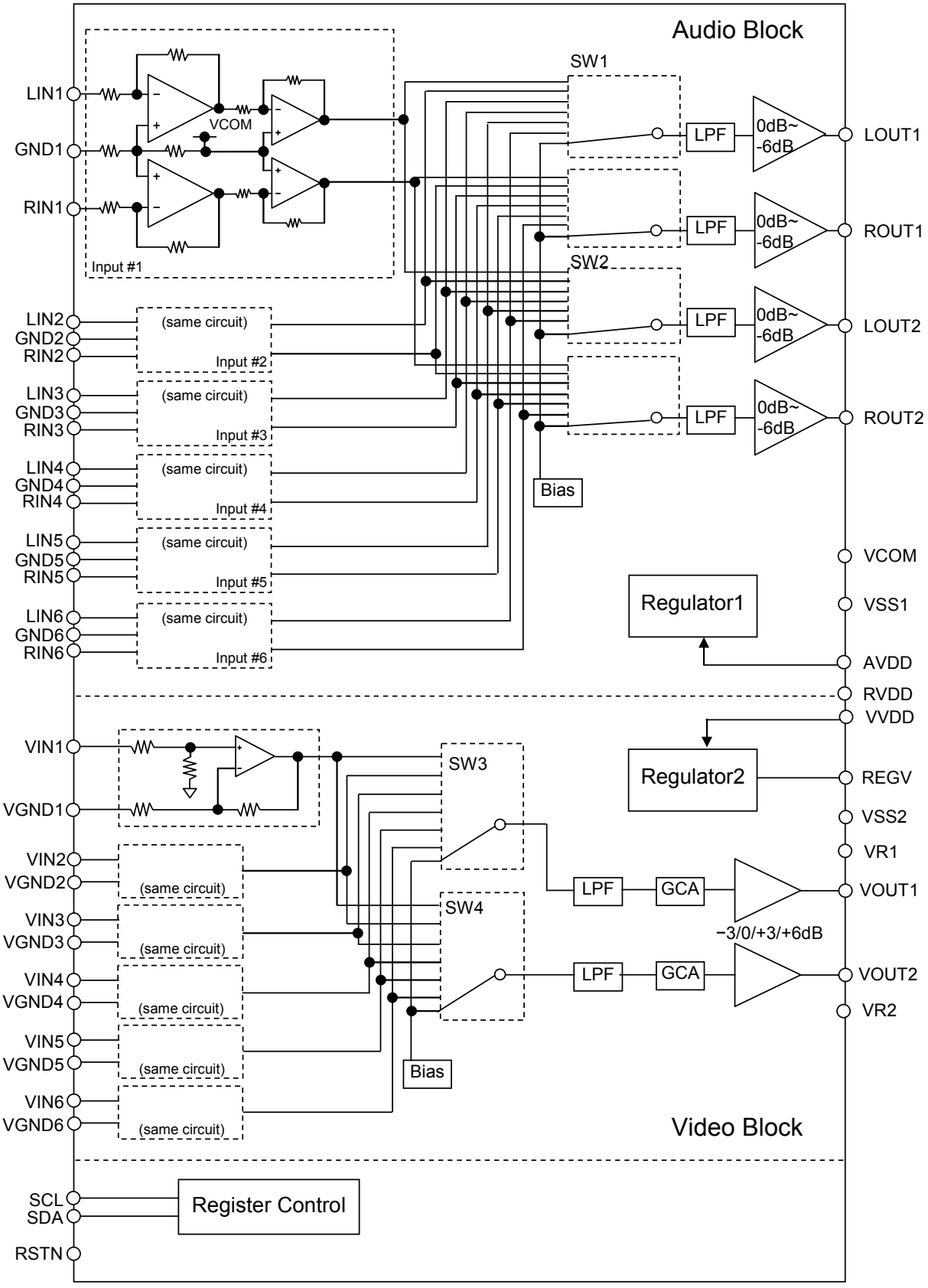
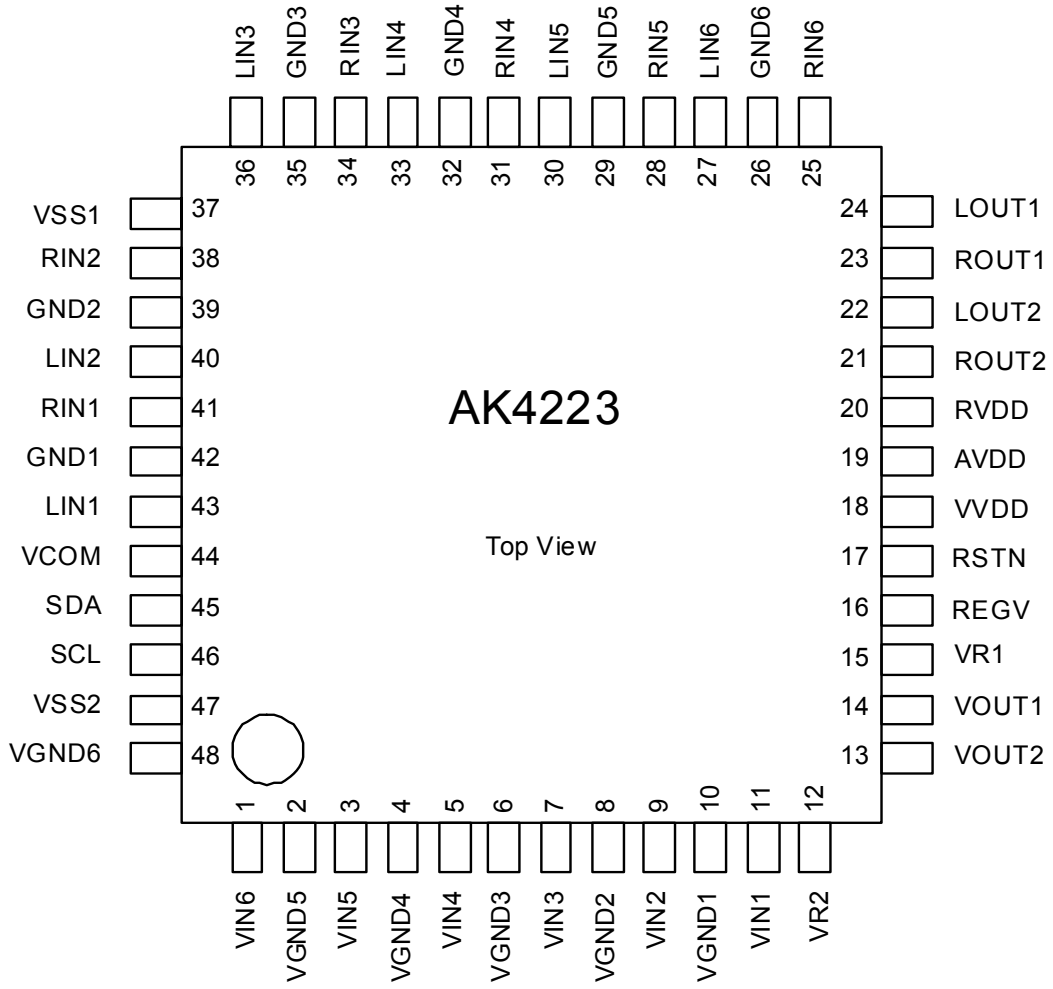


Figure 1. AK4223 Block Diagram

■ Ordering Guide

AK4223VQ	-40 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD4223	Evaluation Board for AK4223	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VIN6	I	Video Signal Input Pin 6.
2	VGND5	I	Video GND Input Pin 5.
3	VIN5	I	Video Signal Input Pin 5.
4	VGND4	I	Video GND Input Pin 4.
5	VIN4	I	Video Signal Input Pin 4.
6	VGND3	I	Video GND Input Pin 3.
7	VIN3	I	Video Signal Input Pin 3.
8	VGND2	I	Video GND Input Pin 2.
9	VIN2	I	Video Signal Input Pin 2.
10	VGND1	I	Video GND Input Pin 1.
11	VIN1	I	Video Signal Input Pin 1.
12	VR2	O	Video Signal Clamp Reference Pin 2. Normally connected to VSS2 with a 0.1µF capacitor.
13	VOUT2	O	Video Signal Output Pin 2.
14	VOUT1	O	Video Signal Output Pin 1.
15	VR1	O	Video Signal Clamp Reference Pin 1. Normally connected to VSS2 with a 0.1µF capacitor.
16	REGV	O	Regulator Output Pin for the power supply of Video Core Circuit. 5.0V (typ) For stability of the regulator, this pin must connect to VSS2 with a 10µF capacitor.
17	RSTN	I	Reset Mode Pin "L": Reset mode (All registers are initialized to their default values.) "H": Normal operation
18	VVDD	-	Power Supply Pin: 7.5V~9.5V
19	AVDD	-	Power Supply Pin: 7.5V~9.5V
20	RVDD	-	Power Supply Pin: 7.5V~9.5V
21	ROUT2	O	Audio Signal Output Pin ROUT 2.
22	LOUT2	O	Audio Signal Output Pin LOUT 2.
23	ROUT1	O	Audio Signal Output Pin ROUT 1.
24	LOUT1	O	Audio Signal Output Pin LOUT 1.
25	RIN6	I	Audio Signal Input Pin RIN 6.
26	GND6	I	Audio GND Input Pin GND 6.
27	LIN6	I	Audio Signal Input Pin LIN 6.
28	RIN5	I	Audio Signal Input Pin RIN 5.
29	GND5	I	Audio GND Input Pin GND 5.
30	LIN5	I	Audio Signal Input Pin LIN 5.
31	RIN4	I	Audio Signal Input Pin RIN 4.
32	GND4	I	Audio GND Input Pin GND 4.
33	LIN4	I	Audio Signal Input Pin LIN 4.
34	RIN3	I	Audio Signal Input Pin RIN 3.
35	GND3	I	Audio GND Input Pin GND 3.
36	LIN3	I	Audio Signal Input Pin LIN 3.
37	VSS1	-	Audio Ground Pin
38	RIN2	I	Audio Signal Input Pin RIN 2.
39	GND2	I	Audio GND Input Pin GND 2.
40	LIN2	I	Audio Signal Input Pin LIN 2.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
41	RIN1	I	Audio Signal Input Pin RIN 1.
42	GND1	I	Audio GND Input Pin GND 1.
43	LIN1	I	Audio Signal Input Pin LIN 1.
44	VCOM	O	Audio VCOM Voltage Pin. Normally connected to VSS1 with a 1μF electrolytic capacitor.
45	SDA	I/O	Control Data Pin.
46	SCL	I	Control Data Clock Pin.
47	VSS2	-	Video Ground Pin.
48	VGND6	I	Video GND Input Pin 6.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Audio Inputs	LIN1-6, RIN1-6, GND1-6	These pins must be open.
Video Input	VIN1-6, VGND1-6	These pins must be connected to VSS2.
Audio, Video Outputs	LOUT1-2, ROUT1-2, VOUT1-2	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2 =0V; Note 1)

Parameter	Symbol	min	max	Unit
Power Supply	AVDD VVDD RVDD	-0.3	+14.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Audio Input Voltage	VINA	-0.3	AVDD+0.3	V
Video Input Voltage	VINV	-0.3	5.5	V
Digital Input Voltage	VIND	-0.3	5.5	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. AVDD and RVDD must be the same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2 = 0V)

Parameter	Symbol	min	typ	max	Unit
Power Supply	AVDD VVDD RVDD	7.5	9.0	9.5	V

Note 3. AVDD and RVDD must be the same voltage.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta=25°C; AVDD= RVDD= VVDD= 9.0V; VSS1= VSS2 = 0V)

Power Supplies				
Parameter	**min**	**typ**	**max**	**Unit**
Power Supply (AVDD+RVDD+VVDD)				
Normal Operation (Note 4), (RSTN pin = "H")		33	50	mA
Power-Down Mode (Note 5), (RSTN pin = "L")		2.1	3.1	μA

Note 4. No input, No load.
Note 5. This is the value without analog inputs when all digital input pins are fixed to VSS1 or VSS2.

ANALOG CHARACTERISTICS (Audio)

(Ta=25°C; AVDD= RVDD= VVDD= 9.0V; VSS1=VSS2= 0V; Signal Frequency=1kHz, Measurement Frequency= 20Hz~20kHz, unless otherwise specified)

Parameter	Conditions	min	typ	max	Unit
S/(N+D) (Note 6)	Input=0dBV	82	90		dB
DR (0dBV reference) (Note 6)	Input=-60dBV, A-weighted	88	94		dB
S/N (0dBV reference) (Note 6)	A-weighted	88	94		dB
Input Impedance		70	100		kΩ
Input Voltage (Note 7)				2	Vrms
Gain	0dB	-0.4	0	+0.4	dB
	-6dB	-6.4	-6.0	-5.6	dB
AGCA step (Note 6)		-	1.0	-	dB
Interchannel Isolation (Note 8)		-	100		dB
LPF Frequency Response Input=1Vrms, 0dB at 1kHz	Response at 24kHz	-2	-0.5	-	dB
	Response at 96kHz	-	-24	-	dB
Interchannel Gain Mismatch			0.2	-	dB
Gain Drift			20	-	ppm/°C
Load Resistance (Note 9)	R1 (Figure 2) R1+R2 (Figure 2)	300 5			Ω kΩ
Load Capacitance	C1 (Figure 2) C2 (Figure 2)			1.5 30	nF pF
Power Supply Rejection	(Note 10)	-	74		dB
CMRR	f=1kHz, 1Vp-p input	35	45		dB

Note 6. This is a value when AGCA=0dB.
Note 7. The Input Voltage meets S/(N+D)>82dB.
Note 8. Between all channels of LIN1-6 and RIN1-6.
Note 9. The output resistance of audio output (LOUT1-2 and ROUT1-2) are less than l0Ω (typ).
Note 10. Applied to AVDD, RVDD and VVDD with a sine wave (1kHz, 50mVpp).

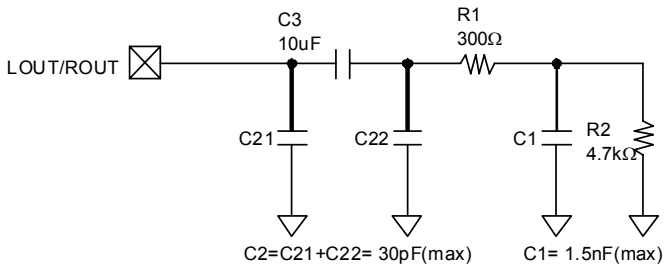


Figure 2. Load Resistance R1, R2 and Load Capacitance C1, C2

ANALOG CHARACTERISTICS (Video)

(Ta = 25°C; AVDD= RVDD= VVDD= 9.0V; VSS1= VSS2 = 0V; VGAIN= +6dB, VGCA=0dB; VR1/2 bit="0"; unless otherwise specified.)

Parameter	Conditions		min	typ	max	Unit
Sync tip clamp level (Note 11)	VGAIN=+3dB, +6dB				200	mV
	VGAIN=-3dB, 0dB				500	mV
Gain Input=0.3Vp-p, 100kHz	VGCA=+1dB	6dB	-	7	-	dB
		3dB	-	4	-	dB
		0dB	-	1	-	dB
		-3dB	-	-2	-	dB
	VGCA=0dB	6dB	5.6	6	6.4	dB
		3dB	2.6	3	3.4	dB
		0dB	-0.4	0	0.4	dB
		-3dB	-3.4	-3	-2.6	dB
	VGCA=-1dB	6dB	-	5	-	dB
		3dB	-	2	-	dB
		0dB	-	-1	-	dB
		-3dB	-	-4	-	dB
VGCA step			-	0.1	-	dB
Frequency Response Input=0.3Vpp, Sin Wave (0dB at 100kHz)	Response at 6MHz		-1.0		+1.0	dB
	Response at 27MHz		-	-35	-	dB
Group Delay Distortion	|GD3MHz – GD6MHz|			10	40	ns
Input Impedance				300		kΩ
Input Signal					1.5	Vpp
Inter channel Isolation	f=4.43MHz, 1Vpp input		-	52		dB
S/N	Reference Level = 0.7Vp-p, BW= 100kHz to 6MHz.		-	65		dB
Differential Gain	0.7Vpp 5steps modulated staircase. Chrominance & burst are 280mVpp, 4.43MHz.			+0.4	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. Chrominance & burst are 280mVpp, 4.43MHz.			+1	-	Degree
Load Resistance	VR1/2 bit = "0", R1+R2 (Figure 4)		140	150	160	Ω
	VR1/2 bit = "1", R1 (Figure 5)		100	-	-	kΩ
Load Capacitance	VR1/2 bit = "0", (Figure 4)					
		C1			1.5	nF
		C2			15	pF
	VR1/2 bit = "1", (Figure 5)					
		C1+C2			15	pF
CMRR	f=20kHz, 1Vp-p input		34	55		dB

Note 11. At the measurement point A in Figure 3. Idling DC output level is 200mV(max) when VGAIN=+6dB or +3db, and 500mV(max) when VGAIN=0dB or -3dB.

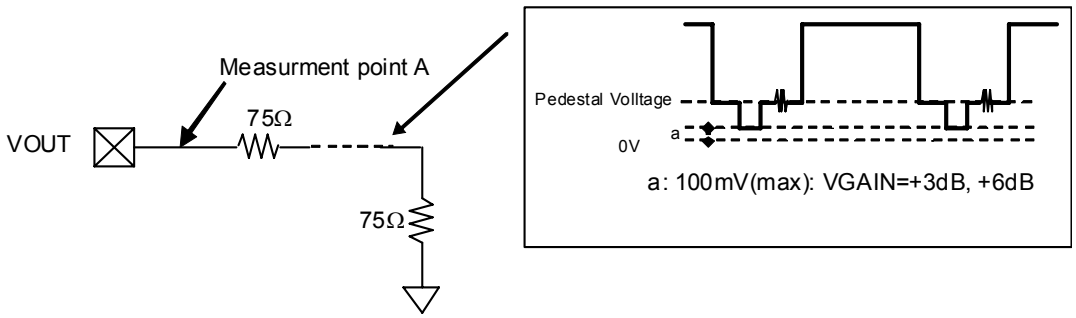


Figure 3. Measurement Point

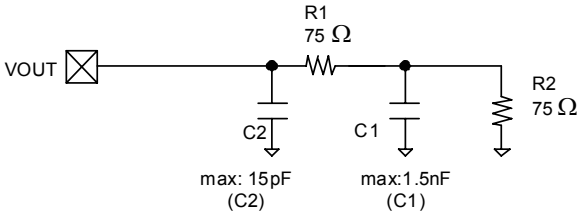


Figure 4. Load Resistance R1+R2 and Load Capacitance C1/C2 (VR1/2 bit = "0")

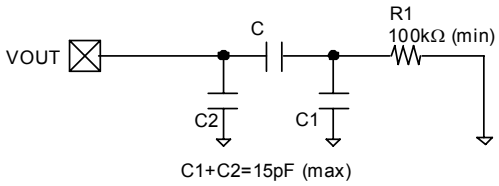


Figure 5. Load Resistance R1+R2 and Load Capacitance C1/C2 (VR1/2 bit = "1")

DC CHARACTERISTICS

(Ta=-40~85°C; AVDD= RVDD= VVDD= 7.5~9.5V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage (RSTN,SCL,SDA,CAD pins)	VIH	2.7	-	5.5	V
Low-Level Input Voltage (RSTN,SCL,SDA,CAD pins)	VIL	-	-	0.8	V
Low-Level Output Voltage (SDA pin: Iout=3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta= 25°C; AVDD =RVDD= VVDD= 9.0V)

Control Interface Timing (I^2C Bus)					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 13)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
RSTN Reject Pulse Width	tRPD			15	ns
RSTN Pulse Width (Note 14)	tPD	150			ns

Note 12. I^2C-bus is a trademark of NXP B.V.
Note 13. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 14. The AK4223 can be reset by setting the RSTN pin = "L" when powered up.

■ Timing Diagram

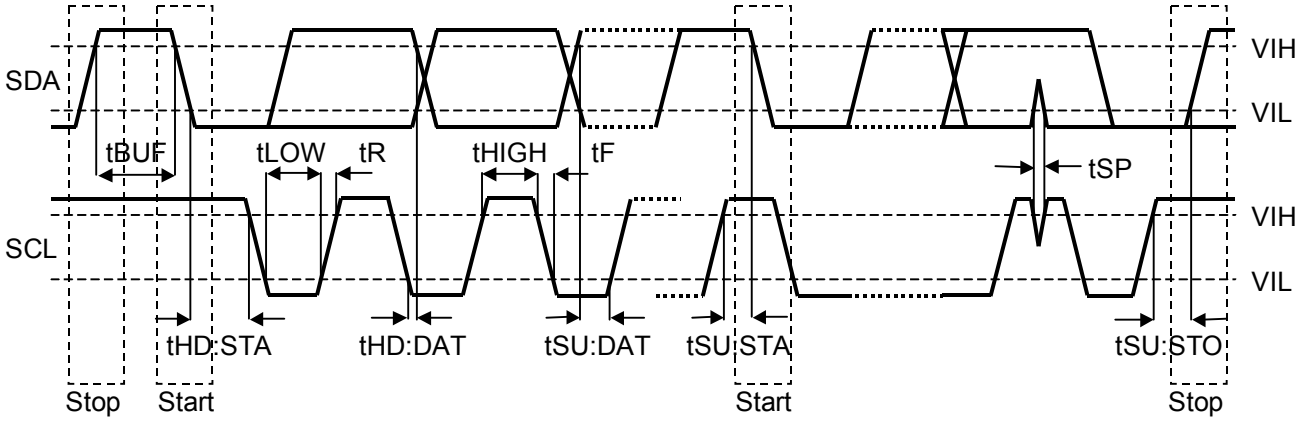


Figure 6. I²C Bus mode Timing

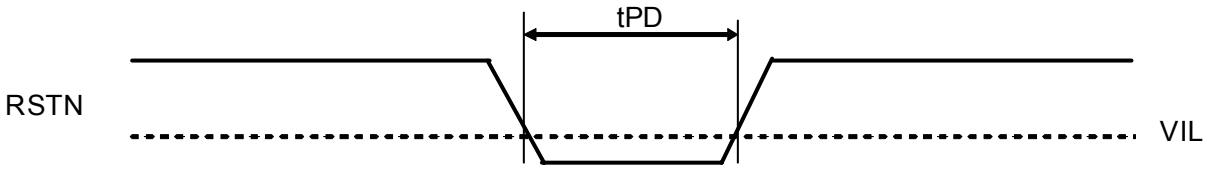


Figure 7. Reset Mode Timing

OPERATION OVERVIEW

■ Power Up/Down

The AK4223 can be reset by bringing the RSTN pin = "L" upon power-up. In reset mode, internal resisters are initialized and the audio and video circuits are in power-down state outputting Hi-Z signals. The RSTN pin must be "L" to execute this reset when power up the AK4223.

■ Audio and Video Signal Inputs

1. Audio Signal Input

The ground noise is cancelled by the differential input with the same ground for L and R channels. The output of LIN and RIN are the same phase. LIN1-6, RIN1-6 and GND1-6 pins must be AC coupled with a 0.47uF capacitor.

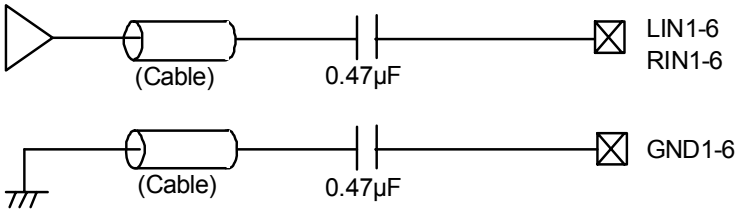


Figure 8. Audio Input Circuit (Differential)

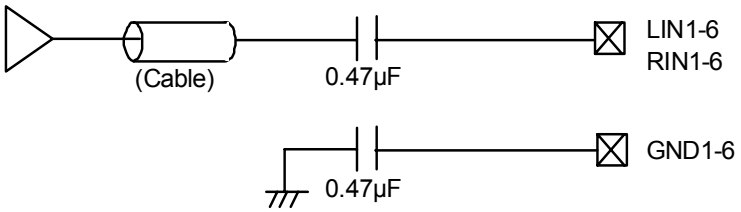


Figure 9. Audio Input Circuit (Single-ended)

2. Video Signal Input

Sync-tip output level is fixed by the internal clamp circuit. VIN1-6 pins must be input via a 0.1uF capacitor for AC coupling.

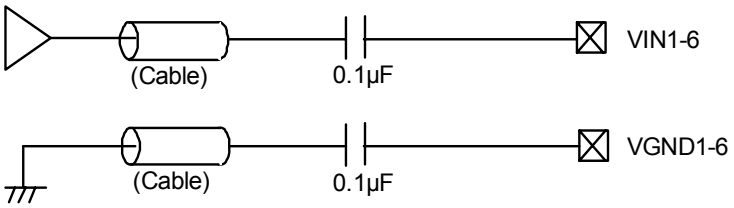


Figure 10. Video Input Circuit (Differential)

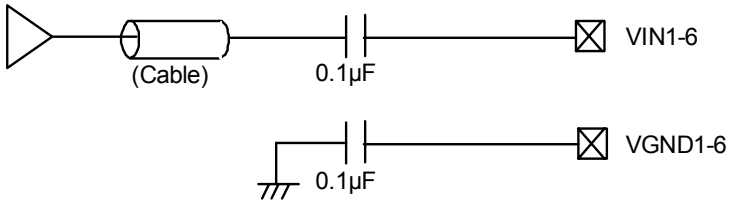


Figure 11. Video Input Circuit (Single-ended)

■ Input Selector

The AK4223 has 6:2 input selectors for audio input, and 6:2 input selectors for video input. The audio input selectors are set by ASEL12-10bits and ASEL22-20 bits, and the video input selectors are set by VSEL12-10bits and VSEL22-20 bits.

ASEL12 bit	ASEL11 bit	ASEL10 bit	Input Selector	
0	0	0	Off (Note 15)	(default)
0	0	1	LIN1 / RIN1	
0	1	0	LIN2 / RIN2	
0	1	1	LIN3 / RIN3	
1	0	0	LIN4 / RIN4	
1	0	1	LIN5 / RIN5	
1	1	0	LIN6 / RIN6	
1	1	1	(Reserved)	

Table 1. Audio Input Selector 1 (LOUT1/ROUT1)

ASEL22 bit	ASEL21 bit	ASEL20 bit	Input Selector	
0	0	0	Off (Note 15)	(default)
0	0	1	LIN1 / RIN1	
0	1	0	LIN2 / RIN2	
0	1	1	LIN3 / RIN3	
1	0	0	LIN4 / RIN4	
1	0	1	LIN5 / RIN5	
1	1	0	LIN6 / RIN6	
1	1	1	(Reserved)	

Table 2. Audio Input Selector 2 (LOUT2/ROUT2)

Note 15. The audio outputs become 3.9V(typ., Gain=0dB) when input selectors are OFF.

VSEL12 bit	VSEL11 bit	VSEL10 bit	Input Selector	
0	0	0	Off (Note 16)	(default)
0	0	1	VIN1	
0	1	0	VIN2	
0	1	1	VIN3	
1	0	0	VIN4	
1	0	1	VIN5	
1	1	0	VIN6	
1	1	1	(Reserved)	

Table 3. Video Input Selector 1 (VOUT1)

VSEL22 bit	VSEL21 bit	VSEL20 bit	Input Selector	
0	0	0	Off (Note 16)	(default)
0	0	1	VIN1	
0	1	0	VIN2	
0	1	1	VIN3	
1	0	0	VIN4	
1	0	1	VIN5	
1	1	0	VIN6	
1	1	1	(Reserved)	

Table 4. Video Input Selector 2 (VOUT2)

Note 16. The video outputs become sync tip level when input selectors are OFF.

■ Audio Output Level Setting

AGCA12-10 bits control the audio output level of the L/ROUT1 pin, and AGCA22-20 bits controls the audio output level of the L/ROUT2 pin. (Table 5, Table 6)

AGCA12 bit	AGCA11 bit	AGCA10 bit	L/ROUT1 GAIN [dB]	Output DC Level[V typ]	STEP
0	0	0	0 (default)	3.9	1dB
0	0	1	-1	3.7	
0	1	0	-2	3.5	
0	1	1	-3	3.4	
1	0	0	-4	3.2	
1	0	1	-5	3.1	
1	1	0	-6	3.0	
1	1	1	Reserved	-	

Table 5. L/ROUT1 Output Level Setting

AGCA22 bit	AGCA21 bit	AGCA20 bit	L/ROUT2 GAIN [dB]	Output DC Level[V typ]	STEP
0	0	0	0 (default)	3.9	1dB
0	0	1	-1	3.7	
0	1	0	-2	3.5	
0	1	1	-3	3.4	
1	0	0	-4	3.2	
1	0	1	-5	3.1	
1	1	0	-6	3.0	
1	1	1	Reserved	-	

Table 6. L/ROUT2 Output Level Setting

■ Audio Output Mute Select

The AK4223 has a channel independent mute function for audio outputs. AMUTE1/2 bits control L/ROUT1 and L/ROUT2 outputs mute. (Table 7, Table 8)

AMUTE1 bit	L/ROUT1 Output	
0	Normal Output	(default)
1	Mute	

Table 7. L/ROUT1 Output Mute Control

AMUTE2 bit	L/ROUT2 Output	
0	Normal Output	(default)
1	Mute	

Table 8. L/ROUT2 Output Mute Control

■ Video Output Level Setting

VGAIN11-10 bits control the video output level of the VOUT1 pin, and VGAIN21-20 bits control the video output level of the VOUT2 pin. (Table 9, Table 10)

VGAIN11 bit	VGAIN10 bit	VOUT1 output Level	VOUT1 Sync Tip Level (max)	
0	0	+6dB	200mV	(default)
0	1	0dB	500mV	
1	0	+3dB	200mV	
1	1	-3dB	500mV	

Table 9.VOUT1 Output Level Setting

VGAIN21 bit	VGAIN20 bit	VOUT2 output Level	VOUT2 Sync Tip Level (max)	
0	0	+6dB	200mV	(default)
0	1	0dB	500mV	
1	0	+3dB	200mV	
1	1	-3dB	500mV	

Table 10.VOUT2 Output Level Setting

VGCA14-10 bits finely tune the video output levels of VOUT1, and VGCA24-20 bits tune VOUT2. (Table 11, Table 12)

VGCA14-10 bit	VOUT1 GAIN [dB]	STEP
00000	–1.0	0.1dB
00001	–0.9	
00010	–0.8	
:	:	
01010	0 (default)	
:	:	
10010	+0.8	
10011	+0.9	
10100	+1.0	
others	Reserved	

Table 11. Video Output Level (VOUT1) Fine Tuning Setting

VGCA24-20 bit	VOUT2 GAIN [dB]	STEP
00000	–1.0	0.1dB
00001	–0.9	
00010	–0.8	
:	:	
01010	0 (default)	
:	:	
10010	+0.8	
10011	+0.9	
10100	+1.0	
others	Reserved	

Table 12. Video Output Level (VOUT2) Fine Tuning Setting

■ Video Output Driver

VR1 and VR2 bits control the video output driver of the VOUT1 and VOUT2 pins respectively. VR1 and VR2 bits should be set to "0" when driving 150Ω resistance.

VR1 bit	VOUT1	
0	150Ω Drive	(default)
1	min. 100kΩ Drive	

Table 13. VOUT1 Output Driver Setting

VR2 bit	VOUT2	
0	150Ω Drive	(default)
1	min. 100kΩ Drive	

Table 14. VOUT2 Output Driver Setting

■ Video Output Mute Setting

The AK4223 has a channel independent mute function of the video output. VMUTE1 and VMUTE2 bits mute (Sync tip clamp level) VOUT1 and VOUT2 outputs respectively. (Table 15, Table 16)

VMUTE1 bit	VOUT1 Output	
0	Normal Output	(default)
1	Mute	

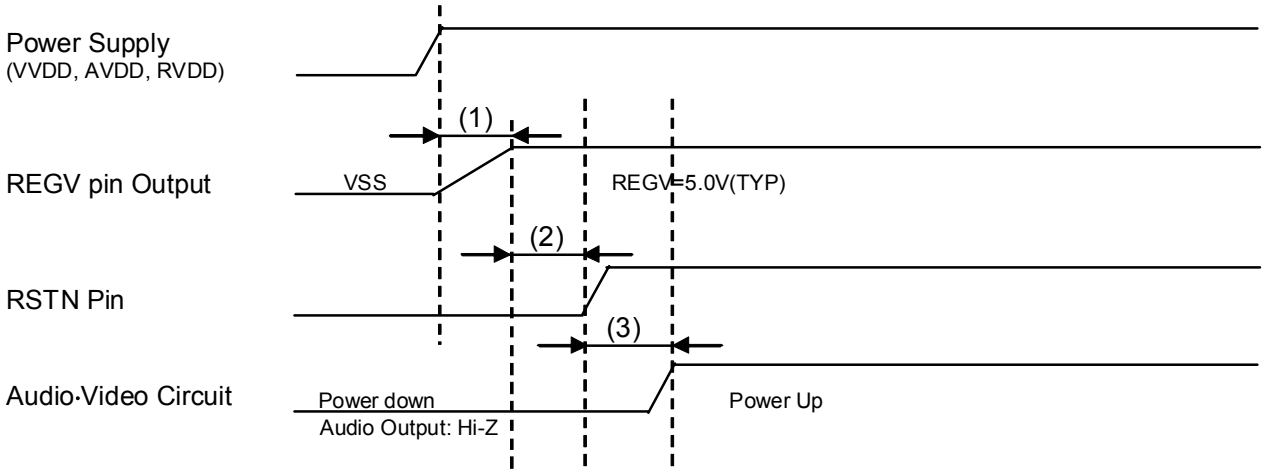
Table 15. VOUT1 Output Mute Control

VMUTE2 bit	VOUT2 Output	
0	Normal Output	(default)
1	Mute	

Table 16. VOUT2 Output Mute Control

■ System Reset

The RSTN pin must be set to "L" when power up the AK4223. The AK4223 powers up in reset state. The REGV pin starts outputting (typ. 5.0V) when power is supplied to the device. This reset is released by setting the RSTN pin to "H". Figure 12 shows the reset sequence.



Notes:
(1) Time that the REGV output reaches 95% of the maximum value. (typ. 800µs, max. 5ms)
(2) Reset Time (min. 150ns)
(3) Time to be in a normal operation after reset release. (Video Output: typ. 100ms, Audio Output: typ. 170ms)
*The required time to be in a normal operation of audio outputs is proportional to the capacity of an external capacitor at the VCOM pin. This typical value 170ms is for when the external capacitor is 1.0µF.

Figure 12 System Reset Diagram

■ Control Interface

The AK4223 supports the fast-mode I²C-bus system (max: 400kHz).

2-1. WRITE Operation

Figure 13 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 19). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010000". If the slave address matches that of the AK4223, the AK4223 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 20). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4223. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 15). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 16). The AK4223 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 19).

The AK4223 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4223 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 8-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 06H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 21) except for the START and STOP conditions.

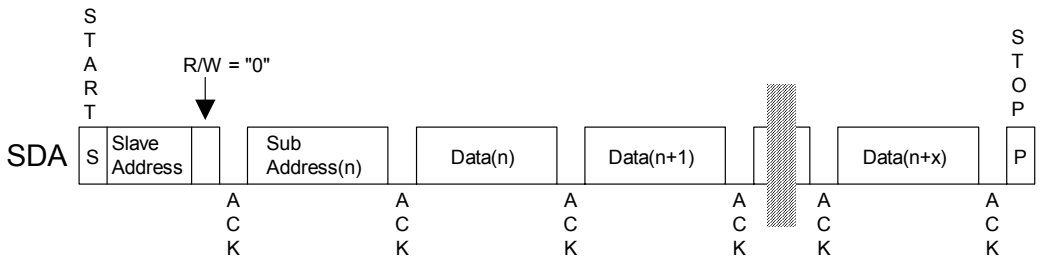


Figure 13. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	0	R/W

Figure 14. The First Byte

0	0	0	0	0	A2	A1	A0

Figure 15. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 16. Byte Structure after the second byte

2-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4223. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 06H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4223 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-2-1. CURRENT ADDRESS READ

The AK4223 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit set to "1", the AK4223 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4223 ceases transmission.

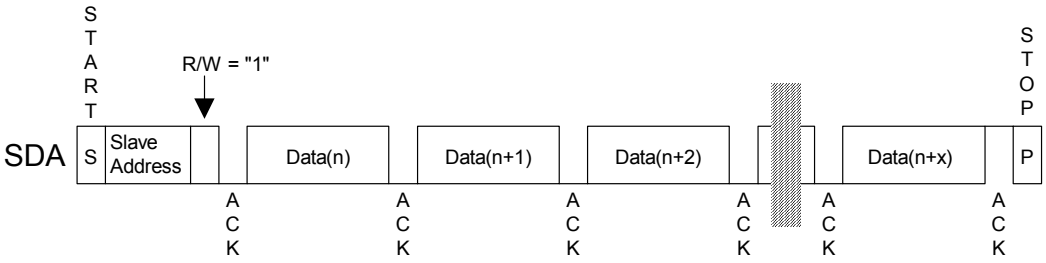


Figure 17. CURRENT ADDRESS READ

2-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4223 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4223 ceases transmission.

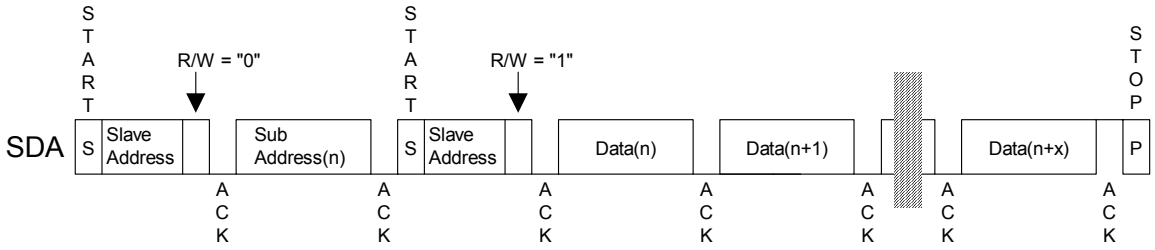


Figure 18. RANDOM ADDRESS READ

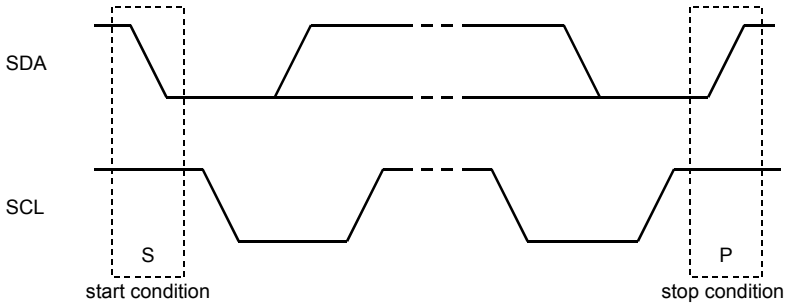


Figure 19. START and STOP Conditions

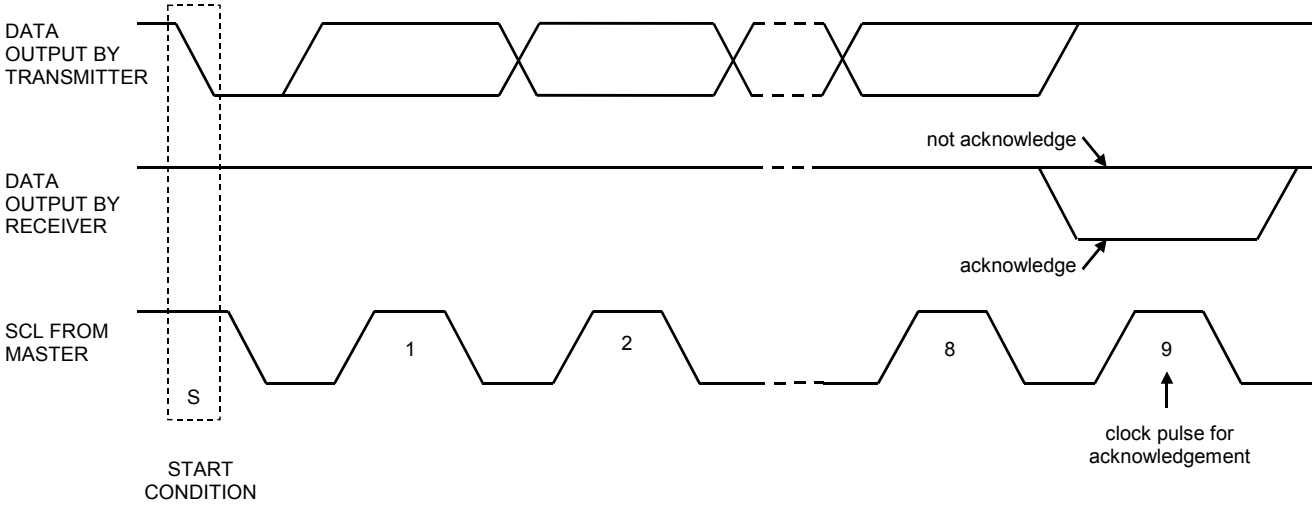


Figure 20. Acknowledge on the I^2C-Bus

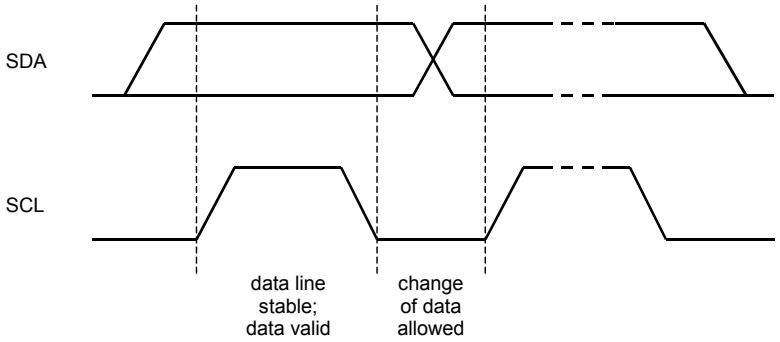


Figure 21. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	VMUTE2	VMUTE1	0	0	AMUTE2	AMUTE1
01H	Input Selector Control1	0	ASEL22	ASEL21	ASEL20	0	ASEL12	ASEL11	ASEL10
02H	Input Selector Control2	0	VSEL22	VSEL21	VSEL20	0	VSEL12	VSEL11	VSEL10
03H	Output Level Control1	0	AGCA22	AGCA21	AGCA20	0	AGCA12	AGCA11	AGCA10
04H	Output Level Control2	0	VR2	VR1	0	VGAIN21	VGAIN20	VGAIN11	VGAIN10
05H	Output Level Control3	0	0	0	VGCA14	VGCA13	VGCA12	VGCA11	VGCA10
06H	Output Level Control4	0	0	0	VGCA24	VGCA23	VGCA22	VGCA21	VGCA20

Note: Do not write any data to the register over 07H.

When the PDN pin changes to “L”, the registers are initialized to their default values.

The bits defined as 0 must contain a “0” value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	VMUTE2	VMUTE1	0	0	AMUTE2	AMUTE1
	Default	0	0	0	0	0	0	0	0

AMUTE2-1: Audio Output Mute Control (Table 7, Table 8)
0: Normal Operation (default)
1: Mute

VMUTE2-1: Video Output Mute Control (Table 15, Table 16)
0: Normal Operation (default)
1: Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Input Selector Control1	0	ASEL22	ASEL21	ASEL20	0	ASEL12	ASEL11	ASEL10
	Default	0	0	0	0	0	0	0	0

ASEL12-10: Audio Input Selector 1 Control (Table 1)
The LOUT1/ROUT2 pin outputs 3.9V (typ., Gain=0dB) at the default setting "000".

ASEL22-20: Audio Input Selector 2 Control (Table 2)
The LOUT2/ROUT2 pin outputs 3.9V (typ., Gain=0dB) at the default setting "000".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Input Selector Control2	0	VSEL22	VSEL21	VSEL20	0	VSEL12	VSEL11	VSEL10
	Default	0	0	0	0	0	0	0	0

VSEL12-10: Video Input Selector 1 Control (Table 3)
The video output is sync tip clamp level at the default setting "000".
VSEL22-20: Video Input Selector 2 Control (Table 4)
The video output is sync tip clamp level at the default setting "000".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Output Level Control1	0	AGCA22	AGCA21	AGCA20	0	AGCA12	AGCA11	AGCA10
	Default	0	0	0	0	0	0	0	0

AGCA11-10: Audio Output L/ROUT1 Level Control (Table 5)
000: 0dB (default)
001: -1dB
010: -2dB
…
110: -6dB
111: Reserved

AGCA21-20: Audio Output L/ROUT2 Level Control (Table 6)
000: 0dB (default)
001: -1dB
010: -2dB
…
110: -6dB
111: Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Output Level Control2	0	VR2	VR1	0	VGAIN21	VGAIN20	VGAIN11	VGAIN10
Default		0	0	0	0	0	0	0	0

VGAIN11-10: Video Output1 Level Control (Table 9)
00: +6dB (default)
01: 0dB
10: +3dB
11: -3dB

VGAIN21-20: Video Output2 Level Control (Table 10)
00: +6dB (default)
01: 0dB
10: +3dB
11: -3dB

VR1: Video Output1 Load Resistance
0: Drive 150Ω (default)
1: Drive 100kΩ (min)

VR2: Video Output2 Load Resistance
0: Drive 150Ω (default)
1: Drive 100kΩ (min)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Output Level Control3	0	0	0	VGCA14	VGCA13	VGCA12	VGCA11	VGCA10
Default		0	0	0	0	1	0	1	0

VGCA14-10: Video Output1 Level Control (Table 11)
The video output is +6dB (when VGAIN11-10 bits = "00"), 0dB (when VGAIN11-10 bits = "01"), +3dB (when VGAIN11-10 bits= "10") and -3dB (when VGAIN11-10 bits = "11") at the default setting "01010".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Output Level Control4	0	0	0	VGCA24	VGCA23	VGCA22	VGCA21	VGCA20
Default		0	0	0	0	1	0	1	0

VGCA24-20: Video Output2 Level Control (Table 12)
The video output is +6dB (when VGAIN21-20 bits = "00"), 0dB (when VGAIN21-20 bits = "01"), +3dB (when VGAIN21-20 bits= "10") and -3dB (when VGAIN21-20 bits = "11") at the default setting "01010".

SYSTEM DESIGN

Figure 22 shows a system connection diagram. An evaluation board [AKD4223] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

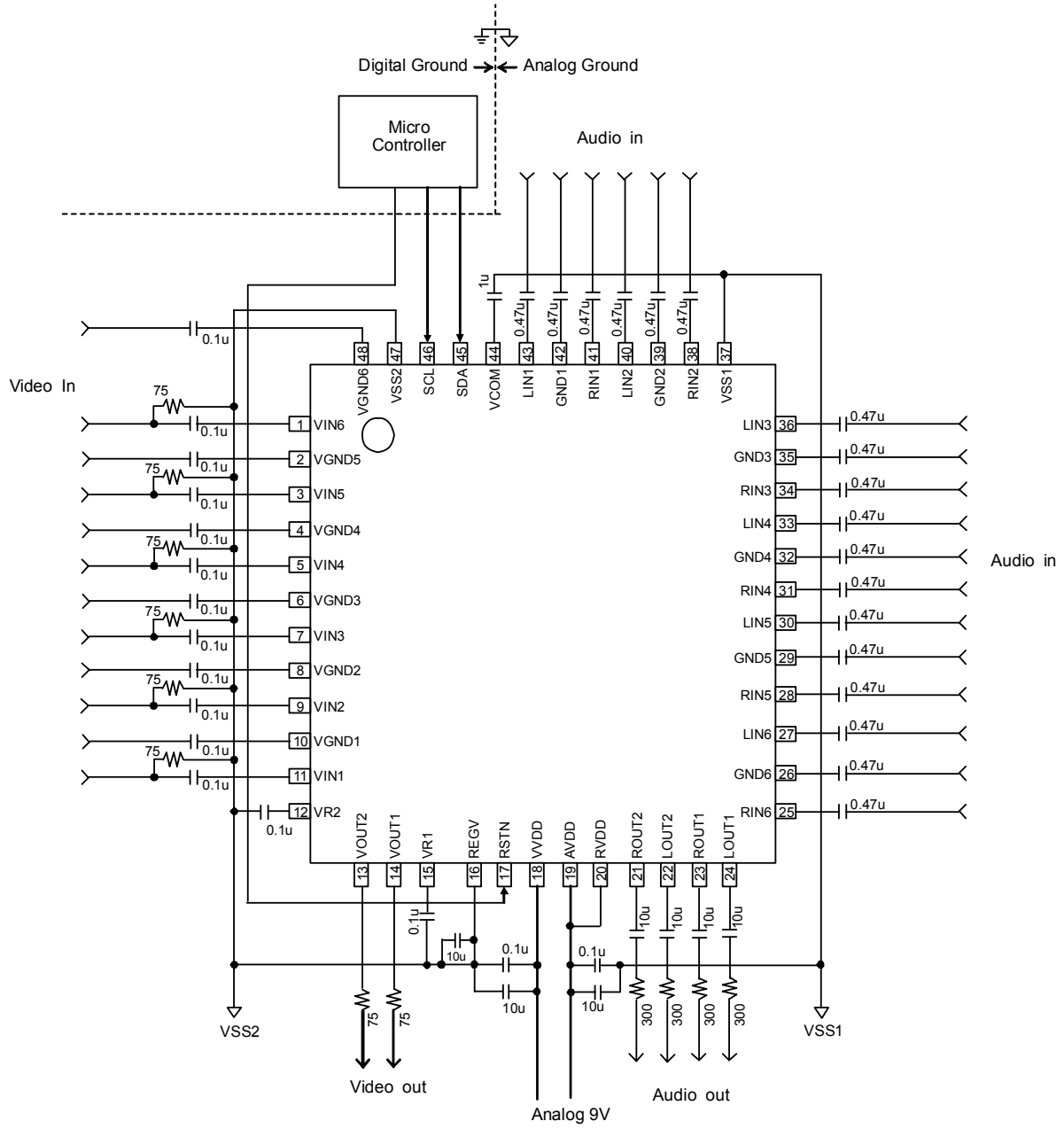


Figure 22. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4223 requires careful attention to power supply and grounding arrangements. AVDD, VVDD and RVDD are usually supplied from the analog power supply in the system. Alternatively if AVDD, VVDD and RVDD are supplied separately, AVDD and RVDD must be powered-up at the same time. The power up sequence between AVDD/RVDD and VVDD is not critical. VSS1 and VSS2 must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the power supply pin of AK4223 as possible.

2. Voltage Reference

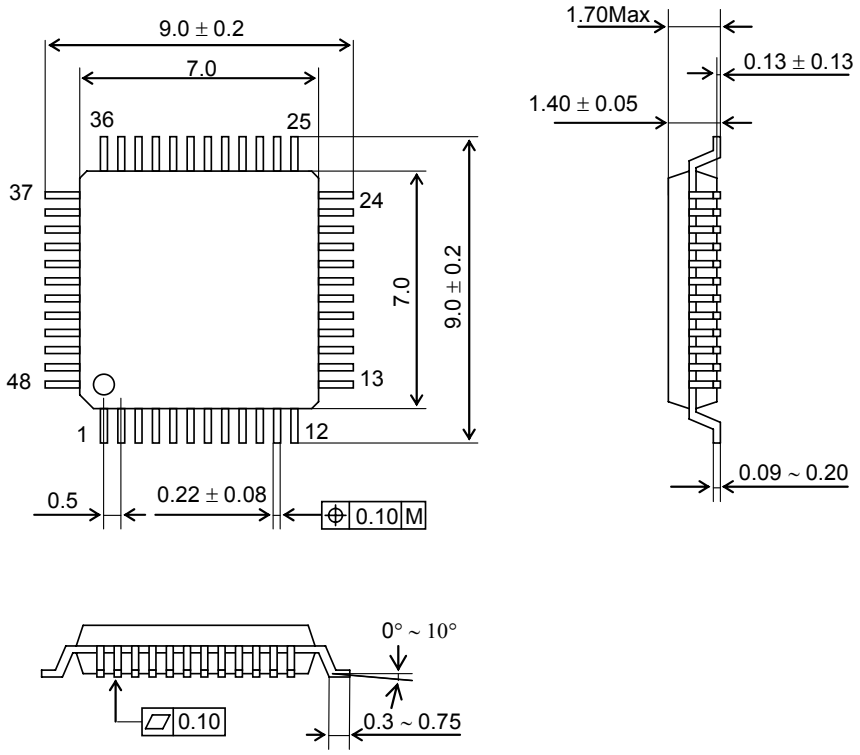
VCOM is a signal ground of this chip. An 1μF electrolytic capacitor attached between VCOM and VSS1 eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. To avoid coupling to the AK4223, all signals and especially clock signals should be kept away as far as possible from the VCOM pin.

3. Notes for Drawing a Board

Analog input and output pins should be as short as possible in order to avoid unwanted coupling into the AK4223. The unused pins should be open.

PACKAGE

48pin LQFP (Unit: mm)



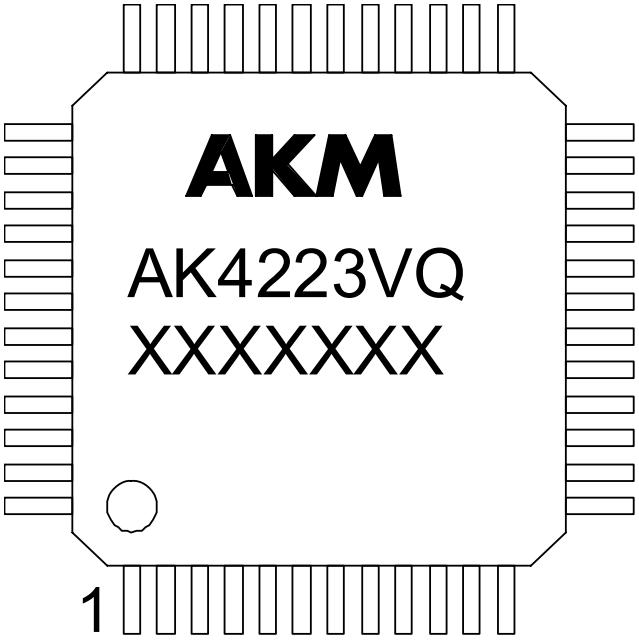
■ Package & Lead Frame Material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

RoHS Compliance

*All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in "lead-free" packages are fully compliant with RoHS.

MARKING



XXXXXXXX: Date code identifier

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
10/10/22	00	First Edition		
13/08/05	01	Figure Modification	2	FEATURES Figure 1 was changed.

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