AK4712

Stereo Cap-less LINE-Amp and HD Video-Amp

GENERAL DESCRIPTION

The AK4712 is a High Definition A/V cap-less line driver. The AK4712 integrates the audio line driver, SD/HD video filters and video drivers. Its A/V outputs are Ground-referenced and eliminate the need for large A/V DC-blocking capacitors with a built-in Charge-pump circuit. The AK4712 achieves excellent A/V performance by single 3.3V power supply. The AK4712 is ideal for a wide range of consumer HD applications, such as portable A/V players, set-top boxes, and Blu-ray/DVD player systems. The AK4712 is offered in a space saving 28pin QFN package.

FEATURES

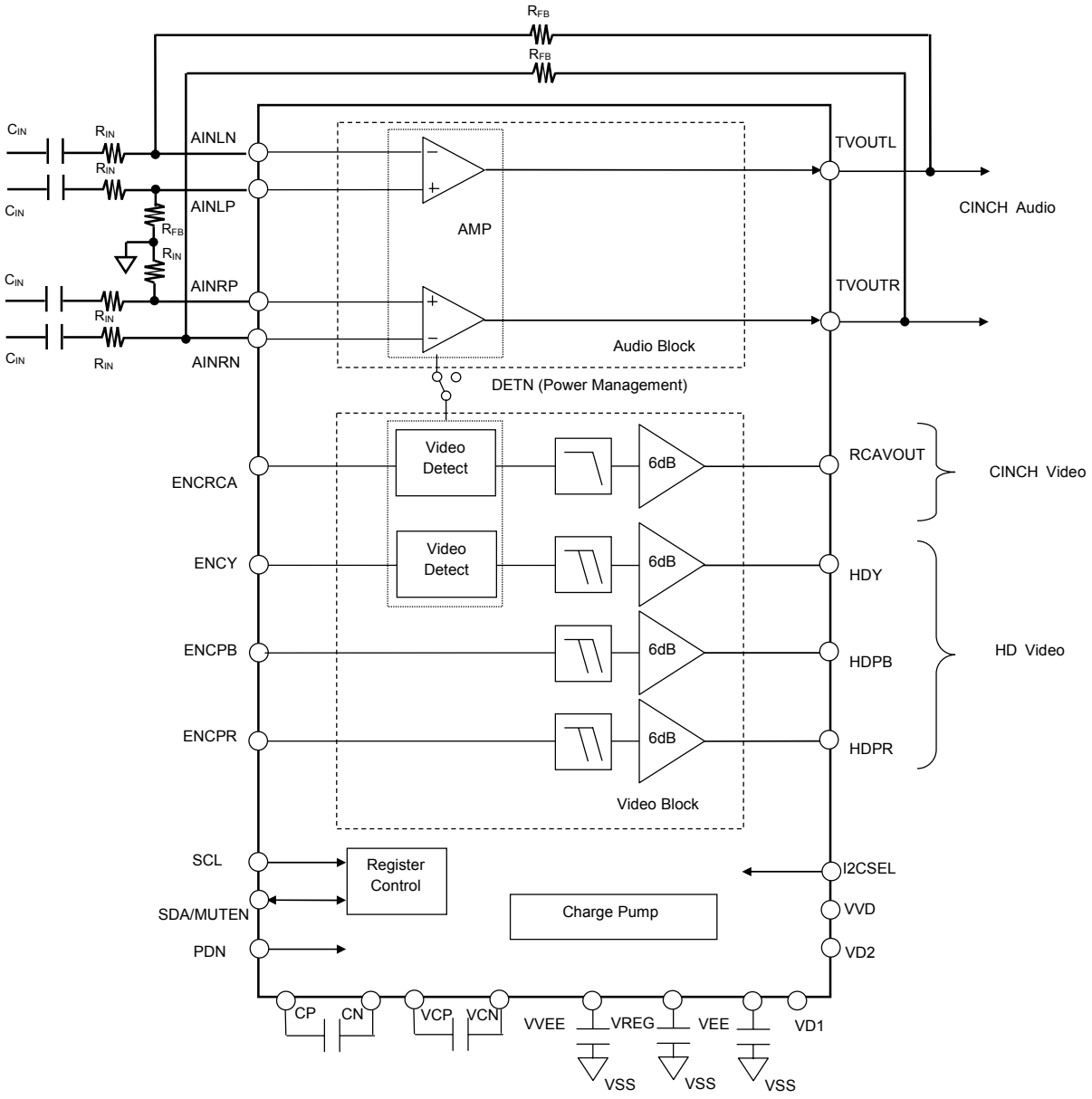
Audio section
- ☐ THD+N: –102dB (@2Vrms)
- ☐ Dynamic Range: 108dB (@2Vrms, A-weighted)
- ☐ Full Differential (or Single-ended) input for Decoder DAC
- ☐ Stereo Output for CINCH (2Vrms)
- ☐ Ground-Referenced Output Eliminates DC-Blocking Capacitor and Mute Circuit

Video section
- ☐ Integrated LPF
  - SD: –40dB@27MHz
  - HD: –36dB@74.25MHz ,–40dB@54MHz or 27MHz selectable
- ☐ 6dB Gain for Outputs
- ☐ 4ch 75ohm driver
  - 3ch for HD: Y/Pb/Pr
  - 1ch for CINCH: CVBS

Power supply
- ☐ 3.3V+/–5%
- ☐ Low Power Standby Mode

Package
- ☐ 28pin QFN (0.4mm pitch)

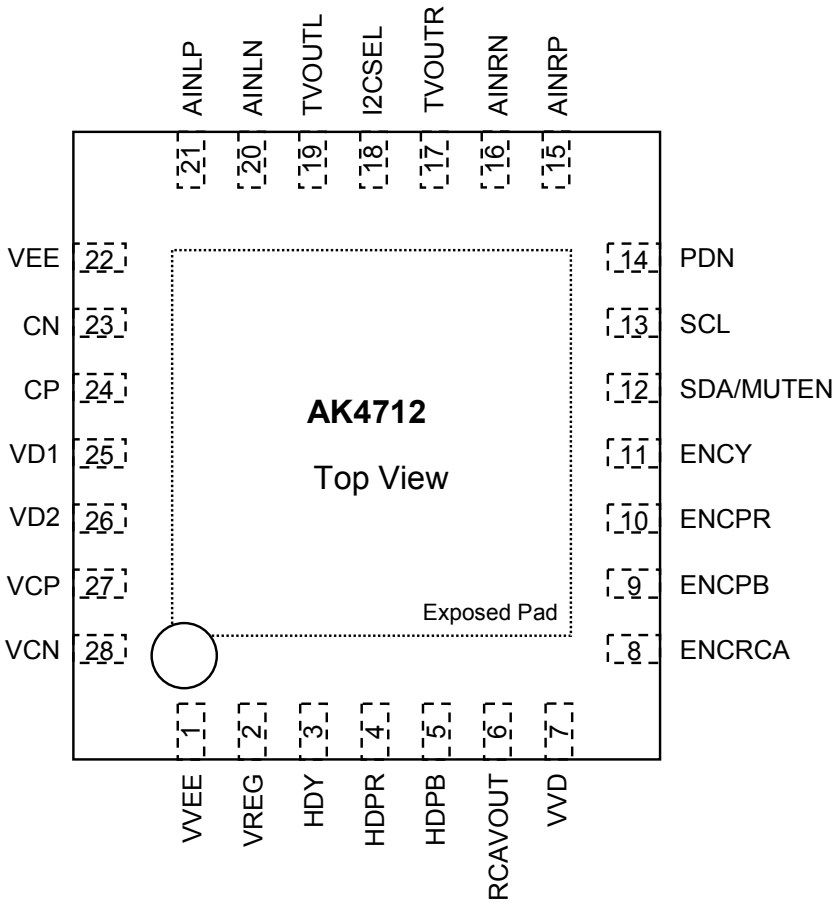
■ Block Diagram



■ Ordering Guide

AK4712EN	-10 ~ +70°C (when both SD and HD video are used) -10 ~ +85°C (when HD Video is not used) 28pin QFN (0.4mm pitch)
AKD4712	Evaluation board for AK4712

■ Pin Layout



Note 1. The exposed pad on the bottom surface of the package must be connected to VSS.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VVEE	O	Video Negative Voltage Output Pin Connect to ground via a 1.0 μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the ground pin. Non-polarized capacitors can also be used.
2	VREG	O	Internal regulator output Pin for Video Charge Pump. Connect to ground via a 1.0 μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the ground pin. Non-polarized capacitors can also be used.
3	HDY	O	Green/Y Output Pin
4	HDPR	O	Red/Pr Output Pin
5	HDPB	O	Blue/Pb Output Pin
6	RCAVOUT	O	Composite Output Pin for RCA
7	VVD	-	Video Power Supply Pin: 3.13V ~ 3.47V Normally connected to ground via a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor.
8	ENCRCA	I	Composite Input Pin for RCA
9	ENCPB	I	Blue/Pb Input Pin for Encoder
10	ENCPR	I	Red/Pr Input Pin for Encoder
11	ENCY	I	Green/Y Input Pin for Encoder
12	SDA/MUTEN	I	I2CSEL= "L": Audio Mute Pin I2CSEL= "H": Control Data Input Pin
13	SCL	I	Control Data Clock Input Pin When I2CSEL="L", SCL pin must be connected to PDN pin.
14	PDN	I	Power-Down Mode Pin When at "L", the AK4712 is in the power-down mode and is held in reset. The AK4712 should always be reset upon power-up.
15	AINRP	I	Rch Positive Analog Input Pin
16	AINRN	I	Rch Negative Analog Input Pin
17	TVOUTR	O	Rch Analog Output Pin
18	I2CSEL	I	I2C Control Enable Pin L: Disable H: Enable
19	TVOUTL	O	Lch Analog Output Pin
20	AINLN	I	Lch Negative Analog Input Pin
21	AINLP	I	Lch Positive Analog Input Pin

22	VEE	O	Audio Negative Voltage Output Pin Connect to ground via a 1.0 μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the ground pin. Non-polarized capacitors can also be used.
23	CN	I	Audio Negative Charge Pump Capacitor Terminal Pin Connect to the CP pin via a 1.0 μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the CP pin. Non-polarized capacitors can also be used.
24	CP	I	Audio Positive Charge Pump Capacitor Terminal Pin Refer to the CN pin.
25	VD1	-	Audio Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS via a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor.
26	VD2	-	Video Charge Pump Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS via a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic cap.
27	VCP	I	Video Negative Charge Pump Capacitor Terminal Pin Connect to the VCN pin via a 1.0 μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the VCP pin. Non-polarized capacitors can also be used.
28	VCN	I	Video Positive Charge Pump Capacitor Terminal Pin Refer to the VCP pin.
-	VSS (Exposed Pad)	-	Analog Ground The exposed pad on the bottom surface of the package must be connected to the ground.

Note: All digital input pins must not be allowed to float.

■Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AINLN, AINLP, AINRP, AINRN, ENCPB, ENCPR	Open
	ENCRCA, ENCY	VVD
	TVOUTL, TVOUTR, RCAVOUT, HDY, HDPB, HDPR	Open
Digital	SCL	Connect to PDN pin

ABSOLUTE MAXIMUM RATINGS

(VSS = 0V; Note 2)

Parameter	Symbol	min	max	Unit
Power Supply	VD1 VD2 VVD	–0.3 –0.3 –0.3	4.0 4.0 4.0	V V V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage(PDN, I2CSEL pins)	VIND1	–0.3	VVD+0.3	V
Digital Input Voltage (SCL, SDA/MUTEN pins)	VIND2	–0.3	4.0	V
Video Input Voltage	VINV	–0.3	VVD+0.3	V
Audio Input Voltage (Note 3)	VINA	VEE-0.3	VD1+0.3	V
Ambient Operating Temperature	Ta (Note 4) Ta (Note 5)	–10	70 85	°C
Storage Temperature	Tstg	–65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VEE: VEE pin voltage.

The internal negative power supply generating circuit provides negative power supply (VEE).

The PDN pin and MUTEN bit control operation mode as shown in Table 2.

Mode			VEE pin Voltage
0	Full Power-down		0V
1	Mute and Video power down (AMP power down)	No video input	0V
2	Mute and Video power up (AMP power down)	Video input	0V
3	Normal operation (AMP operation)	No video input	-VD2+0.2V
4	Normal operation (AMP operation)	Video input	-VD2+0.2V

Table 1. VEE pin voltage

Note 4. When both SD and HD video are used.

Note 5. When HD video is not used.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS = 0V; Note 2)

Parameter	Symbol	min	typ	max	Unit
Power Supply (Note 6)	VD1	3.13	3.3	3.47	V
	VD2	3.13	3.3	3.47	V
	VVD	3.13	3.3	3.47	V

Note 2. All voltages with respect to ground.
Note 6. VVD must be connected to the same voltage.

*AKM assumes no responsibility for the usage beyond recommended operating conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VD1=VD2=VVD= 3.3V)

Power Supplies		min	typ	max	Unit
Power Supply Current					
Normal Operation (PDN = "H")					
VD1+VD2+VVD	(With load, Note 7)		100	136	mA
VD1+VD2+VVD	(With load, Note 8)		28.0		mA
Standby Mode (PDN = "H")	(Note 9)				
VD1+VD2+VVD			1.2	1.7	mA
Power-Down Mode (PDN = "L")	(Note 10)				
VD1+VD2			0	10	μA
VVD			0	10	μA

Note 7. MUTEN bit = "1", SDAPW bit = HDAPW bit = "1", Audio Output:1kHz 2Vrms output with 4.5kΩ load at all audio output pins, 100% color bar output with 150Ω load at all video output pins..
Note 8. When HD video is not used.
Note 9. MUTEN bit = "0", SDAPW bit = HDAPW bit = "1", No video signal.
Note 10. All digital inputs are held at VD1 or VSS. No signal, no load.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD1=VD2=VVD= 3.13 ~ 3.47V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%VD1	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD1	V
Low-Level Output Voltage (SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta=25°C; VD1=VD2=VVD= 3.3V; Signal Frequency=1kHz; Measurement frequency=20Hz ~ 20kHz; R_L ≥4.5kΩ; 2Vrms output; R_{IN}=10 kΩ, R_{FB}=20 kΩ, unless otherwise specified)

Parameter	min	typ	max	Unit
Analog Input: (AINLP/AINLN/AINRN/AINRP pins)				
Analog Input Characteristics (Note 11)				
Input Resistance R_{IN}	1	10	47	kΩ
Feedback Resistance R_{FB}	4.7	20	100	kΩ
Stereo Output: (TVOUTL/TVOUTR pins) (Note 12)				
Analog Output Characteristics				
Output Voltage (Note 13)		2.0		Vrms
THD+N (at 2Vrms output, Note 14, Note 15)		–102	-80	dB
Dynamic Rang (–60dB Output, A-weighted, Note 14)	98	108		dB
S/N (A-weighted, Note 14, Note 17)	98	108		dB
Interchannel Isolation (Note 14)	90	100		dB
DC offset (Note 16)	-5	0	+5	mV
Load Resistance TVOUTL/R	4.5			kΩ
Load Capacitance TVOUTL/R			20	pF
Power Supply Rejection (PSRR) (Note 18)	-	70		dB

Note 11. Gain setting by R_{IN} and R_{FB}. It must be in a rage from 0dB to 24dB.

Note 12. Measured by Audio Precision System Two Cascade.

Note 13. f = 1kHz, THD+N = -102dB

Note 14. Analog In to TVOUT. Path : AINLP/N → TVOUTL, AINRP/N → TVOUTR, R_{IN}=10 kΩ, R_{FB}=20 kΩ. At 2Vrms single input, THD+N is -100dB (typ), on path AINLP → TVOUTL, AINRP → TVOUTR, Volume=0dB

Note 15. -82dB (typ) referred to 0.5Vrms output level. R_{IN}=4.7 kΩ, R_{FB}=47 kΩ
: path = AINLP/N → TVOUTL, AINRP/N → TVOUTR.

Note 16. Analog In to TVOUT.
Path : AINLP/N → TVOUTL, AINRP/N → TVOUTR

Note 17. 86dB (typ), referred to 0.5Vrm output level at Gain = +20dB. R_{IN}=4.7 kΩ, R_{FB}=47 kΩ
: path = AINLP/N → TVOUTL, AINRP/N → TVOUTR.

Note 18. The PSRR is applied to VD1 and VD2 and VVD with 1kHz, 100mV.

ANALOG CHARACTERISTICS (SD VIDEO)

(Ta = 25°C; VD1=VD2= VVD= 3.3V; unless otherwise specified.)

Parameter	Conditions	min	typ	max	Unit
External Resistance		35		1000	Ω
External Capacitance		0.05	0.1	0.2	µF
Gain	Input = 0.3Vp-p, 100kHz	5.5	6	6.5	dB
Frequency Response	Input=0.3Vp-p, C1=C2=0pF. 100kHz to 6MHz. at 10MHz. at 27MHz.	-1.0	 -3 -40	0.5 -25	dB dB dB
Pedestal Level	Video Input	-100	0	100	mV
Group Delay Distortion (Note 19)	At 4.43MHz with respect to 1MHz.			20	ns
Input Impedance (Note 20)	Chrominance input (internally biased)	80	100	-	kΩ
Input Signal	f = 100kHz, maximum with distortion < 1.0%, gain = 6dB.	-	-	1.25	Vpp
Load Resistance	(Figure 1)	-	150	-	Ω
Load Capacitance	C1 (Figure 1) C2 (Figure 1)			400 15	pF pF
Dynamic Output Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	2.5	Vpp
Y/C Crosstalk (Note 20)	f = 4.43MHz, 1Vp-p input. Among HDY and ENCPB outputs.	-	-50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW = 15kHz to 5MHz.	-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	1.3	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	1.4	-	Degree
Power Supply Rejection (PSRR)	(Note 21)	-	45		dB

Note 19 HDY/HDPB/HDPR Group Delay Distortion when FL1-0 bits= "00"

Note 20. When CLAMP2 bit = "0", CLAMP1 bit = "1" for Y/C, Y signal is input to the ENCY pin and C signal is input to the ENCPB pin.

Note 21. The PSRR is applied to VD1 and VD2 and VVD and with 100kHz, 100mV.

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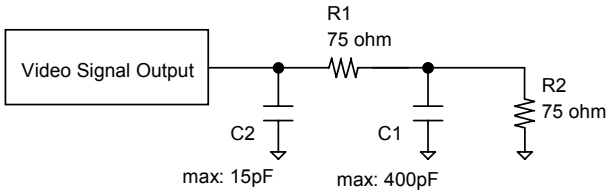


Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

ANALOG CHARACTERISTICS (HD VIDEO)

(Ta = 25°C; VD1=VD2=VVD= 3.3V, unless otherwise specified.)

Parameter	Conditions		min	typ	max	Unit
External Resistance			35		1000	Ω
External Capacitance			0.05	0.1	0.2	µF
Gain	Input=0.3Vp-p, 100kHz		5.5	6	6.5	dB
Frequency response	Input=0.3Vp-p, C1=C2=0pF (Figure 1)	FL1-0 bits = "10" 100kHz to 23MHz, at 30MHz. at 74.25MHz.	-1.0	 -1.0 -36	1.3 -25	dB dB dB
		FL1-0 bits = "01" 100kHz to 15MHz, at 54MHz.	-1.0	 -40	1.0 -25	dB dB
		FL1-0 bits = "00" 100kHz to 6MHz, at 27MHz.	-1.0	 -40	0.5 -25	dB dB
Pedestal Level	Video Input		-100	0	100	mV
Group Delay Distortion (Note 22)	At 4.43MHz with respect to 1MHz.				20	ns
Input Signal	f=100kHz, distortion < 1.0%, gain=6dB		-	-	1.25	Vpp
Crosstalk	at 1MHz		-	-60	-	dB
Load Resistance	(Figure 1)		150	-	-	Ω
Load Capacitance	C1 (Figure 1) C2 (Figure 1)				400 10	pF pF
Dynamic Output Signal	f=100kHz, distortion < 1.0%		-	-	2.5	Vpp
S/N	Reference Level = 0.7Vp-p, unweighted. BW = 100kHz to 30MHz.		-	61	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz. FL1-0 bits = "00"		-	1.0	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz. FL1-0 bits = "00"		-	0.6	-	Degree
Power Supply Rejection (PSRR)	(Note 21)		-	45		dB

Note 22 HDY/HDPB/HDPR Group Delay Distortion when FL1-0 bits = "10"

SWITCHING CHARACTERISTICS

(Ta = 25°C; VD1=VD2= VVD= 3.13 ~ 3.47V)

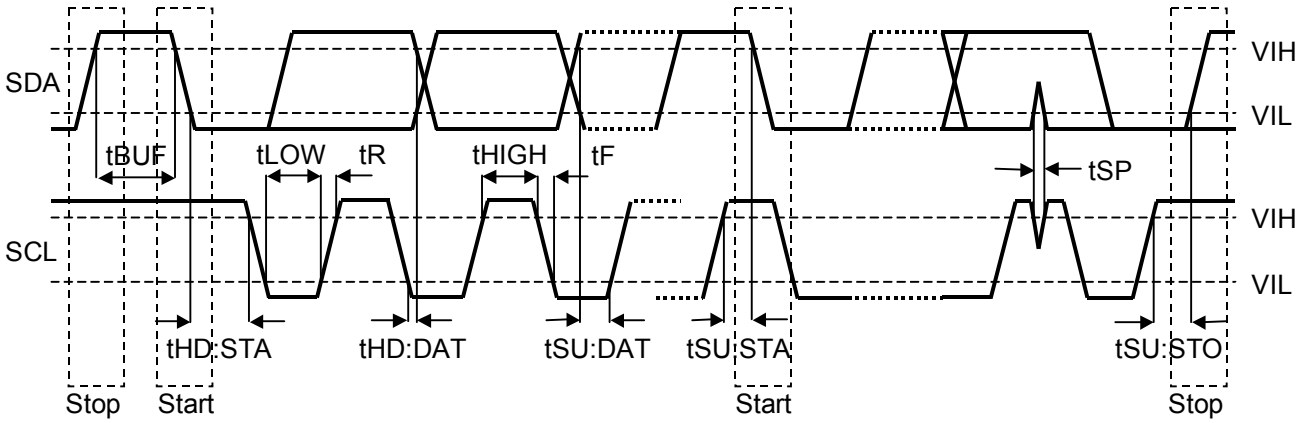
Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 23)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF
Reset Timing					
PDN Pulse Width (Note 24)	tPD	150			ns

Note 23. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

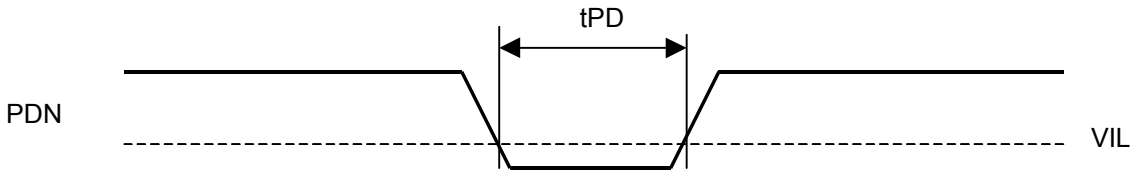
Note 24. The AK4712 should be reset once by bringing the PDN pin = “L” after all power supplies are supplied.

Note 25. I^2C-bus is a trademark of NXP B.V.

■ **Timing Diagram**



I^2C Bus mode Timing



Power-down Timing

OPERATION OVERVIEW

1. System Reset and Power-down Options

■ System Reset and Full Power-down Mode

The AK4712 should be reset once by bringing the PDN pin = "L" after all power supplies are supplied.

PDN pin: Power down pin
L: Full Power-down Mode. Power-down, reset and initializes control registers.
H: Device active.

■ I2C Mode and Hard Wired Mode

The AK4712 can be controlled via I2C or Hard Wired.

When the I2CSEL pin = "L", the SDA/MUTEN pin is used for audio mute and SCL pin must be connected to PDN pin.
When the I2CSEL pin = "H", several operation modes are selectable via the I^2C-bus.

I2CSEL pin: I2C Control Enable pin
L: Disable (Hard Wired)
H: Enable (I2C)

■ Audio and Video Power Management

The AK4712 detects video signal inputs and power up/down video and audio blocks automatically. When DETN bit = "1", power management of audio block is independent from video input detector.

SD block can be powered down via the control registers.

SDAPW: SD block power-up bit (SD Video output)
0: SD block power-down, RCAVOUT pin is Hi-z
1: SD block power-up (default)

HD block can be powered down via the control registers.

HDAPW: HD block power-up bit (HD Video output)
0: HD block power-down, HDY/HDPB/HDPR pins are Hi-z.
1: HD block power-up (default)

PDN pin	DETN bit	Video Input	MUTEN pin/bit	Register Control	Audio block	Video block
L	*	*	*	Not Available	Power down	Power down
H	0	None	*	Available	Power down	Power down
		Detected	L		Power down	Active (Note 26)
			H		Active	
	1	None	L		Power down	Power down
			H		Active	
		Detected	L		Power down	Active (Note 26)
			H		Active	

Note 26. When SDAPW=HDAPW bit = "0"("1"), Video block is powered down (up).

Table 2. Status of Each Operation Modes (*: Don't care) (Figure 2)

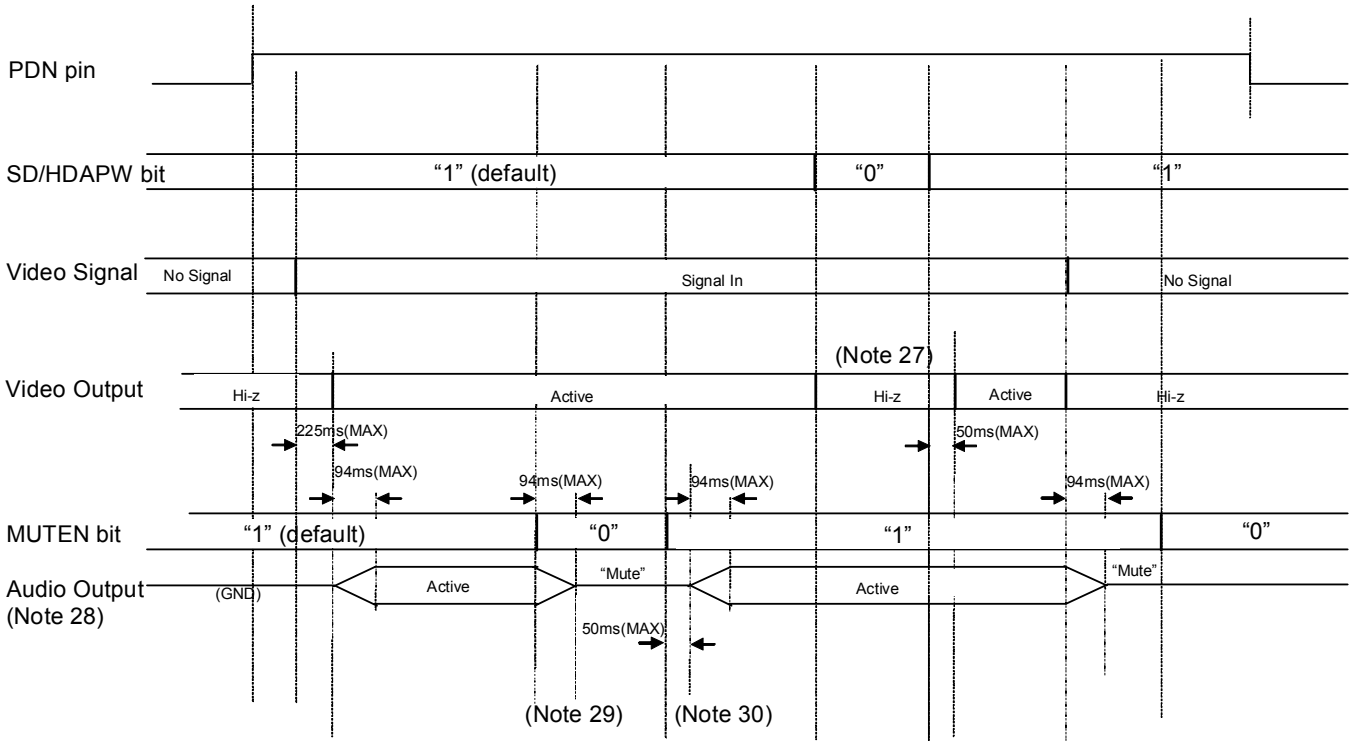
When the I2CSEL pin = "L" (Hard Wired), the SDA/MUTEN pin is used for audio mute.
When the I2CSEL pin= "H" (I2C), MUTEN bit is used for audio mute. The SDA/MUTEN pin is used for Control Data Input.

I2CSEL pin	MUTEN bit	MUTEN pin	Audio block
L	*	L	Power down
		H	Active
H	0	*	Power down
	1		Active

Table 3. Audio Output Status

■ Typical Operation Sequence

Figure 2 shows an example of the system timing in I2C mode. (DETN bit = "0")



Note 27. The RCAVOUT pin =Hi-z when SDAPW bit = "0". HDY=HDPB=HDPR pins =Hi-z when HDAPW bit = "0". Video Charge pump is powered down when SDAPW bit = HDAPW bit = "0".
Note 28. When Video signal is detected, audio output goes active after audio charge pump power up time (max. 225ms) and Mute transition time (Table 5). A click noise does not occur at this time.
Note 29. Audio charge pump is powered down after Mute transition time (Table 5). A click noise does not occur at this time.
Note 30 When MUTEN bit changes from "1" to "0", audio output goes active after audio charge pump power up time (max. 50ms) and Mute transition time (Table 5). A click noise does not occur at this time.

Figure 2. Typical Operating Sequence

2. Audio Block

■ Volume Control (Gain Setting Resistors)

Voltage gain is defined as R_{FB}/R_{IN}. Table 4 lists the gain setting examples.

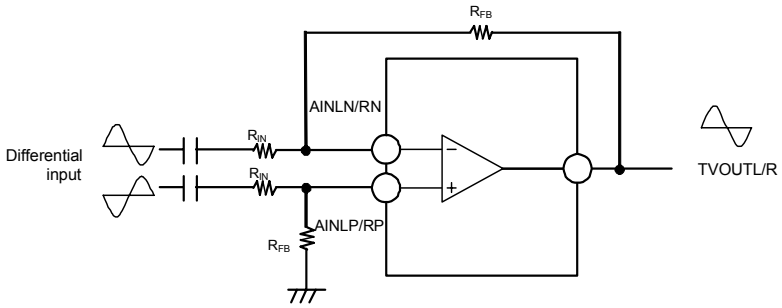


Figure 3. Full Differential Stereo Input

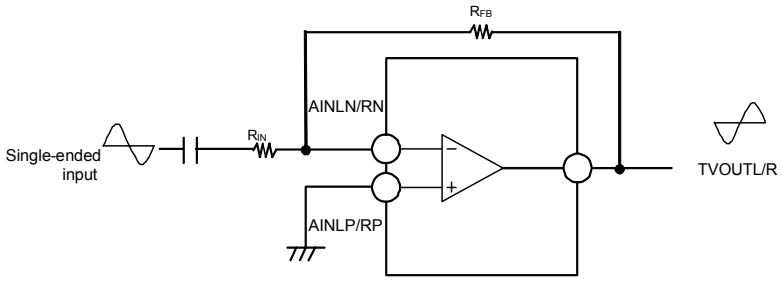


Figure 4. Inverting Single-ended Input

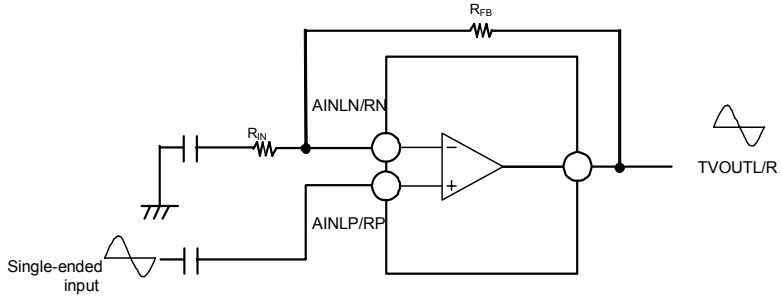


Figure 5. Non-Inverting Single-ended Input

Input Resistors Value, RIN	Feedback Resistors Value, RFB	Figure 3 GAIN	Figure 4 GAIN	Figure 5 GAIN
10 kΩ	10 kΩ	× 1.0	× -1.0	× 2.0
10 kΩ	15 kΩ	× 1.5	× -1.5	× 2.5
10 kΩ	20 kΩ	× 2.0	× -2.0	× 3.0
4.7 kΩ	47 kΩ	× 10	× -10	× 11

Table 4. Gain Setting Examples

■ Analog Output Block

The AK4712 has a charge pump circuit generating negative power supply rail from a 3.3V(typ) power supply. (Figure 6) It allows the AK4712 to output audio signal centered at VSS (0V, typ) as shown in Figure 7. The negative power generating circuit (Figure 6) needs 1.0uF low ESR (Equivalent Series Resistance) capacitors (Ca, Cb). When using polarized capacitors, the positive pin of Ca and Cb capacitors should be connected to CP and VSS, respectively. When MUTEN bit = "0", the charge pump circuit is in power-down mode and its analog outputs become VSS (0V, typ).

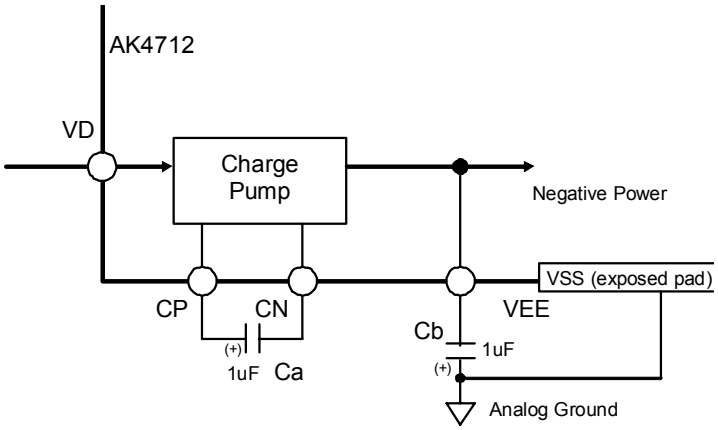


Figure 6. Negative Power Generate Circuit

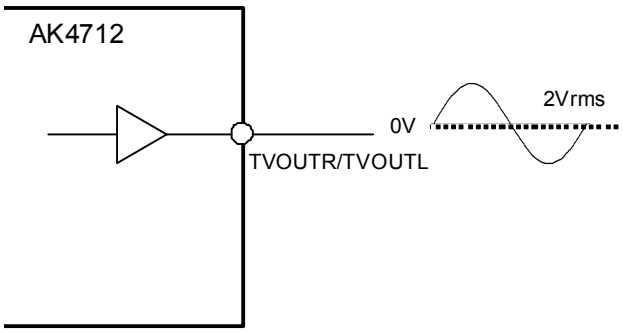


Figure 7. Audio Signal Output

■ Mute Control

When MOD bit = "1" (default), mute control does not cause a pop noise. When MUTEN bit (I2C mode) changes from "1" to "0", the audio output is muted within the transition time selected by MDT1-0 bits (Table 5). When SDA/MUTEN pin (hard wired mode) changes from "H" to "L" , the audio output is muted within the transition time of 94.0ms (max). A mute status switching like this operation (unmute to mute or vice versa) can not be canceled until the end of transition time.

When MOD bit = "0", there is no transition time and mute control may cause a pop noise.

MOD	MDT1	MDT0	Transition Time (typ)	Transition Time (max)	
0	*	*	0ms	0ms	
1	0	0	5.1ms	11.6ms	
1	0	1	10.2ms	23.6ms	
1	1	0	20.5ms	46.8ms	
1	1	1	41.0ms	94.0ms	(default)

Table 5. Mute Transition Time (typ.) (*: Don't care)

3. Video Block

■ HD Video Control (05H: D1-D0)

FL1/0 bits set the HD video filter response.

FL1 bit	FL0 bit	LFP response
0	0	6MHz LPF
0	1	15MHz LPF
1	0	30MHz LPF (default)
1	1	(Reserved)

Table 6. HD Video Filter Control

■ Clamp and DC-restore Circuit Control (03H: D7-D3)

The CLAMP1 and CLAMP2 bits select the input circuit for the ENCPB pin (Encoder Blue/Pb), the ENCPR pin (Encoder Red/Pr) and the ENCY pin (Encoder Green/Y) respectively. When CLAMP2 bit = CLAMP1 bit = "0" (setting for RGB signal), Sync Source of DC Restore is CVBS. When CLAMP2 bit = "0", CLAMP1 bit = "1" (setting for Y/C signal), Y signal is input to the ENCY pin, C signal is input to the ENCPB pin and the ENCPR input circuit is powered down. When CLAMP2 bit = "1", CLAMP1 bit = "1" (setting for Y/Pb/Pr signal), Y signal is input to the ENCY pin, Pb signal is input to the ENCPB pin and Pr signal is input to the ENCPR.

CLAMP2	CLAMP1	ENCY Input Circuit	ENCPB/PR Input Circuit	note	
0	0	DC restore clamp active (-0.6V at sync timing/output pin)	DC restore clamp active (-0.6V at sync timing/output pin)	for RGB	
0	1	DC restore clamp active (-0.572V at sync timing output pin)	Biased (ENCPB) Power down (ENCPR) (0.0V at sync timing/output pin)	for Y/C	
1	0	DC restore clamp active (-0.6V at sync timing/output pin)	DC restore clamp active (0.0V at sync timing/output pin)	for Y/Pb/Pr	(default)
1	1	(Reserved)	(Reserved)		

Table 7. DC-restore control for Encoder Input

■ Video Output Block

The AK4712 has a video amplifier with drivability for a load resistance of 150Ω and a LPF. There are 1 channel composite and HD inputs and outputs. The Internal negative power supply circuit supplies the negative voltage to the video amplifier and the video amp 0V output is used for a pedestal level. Therefore, an output coupling capacitor can be removed. (Figure 8)

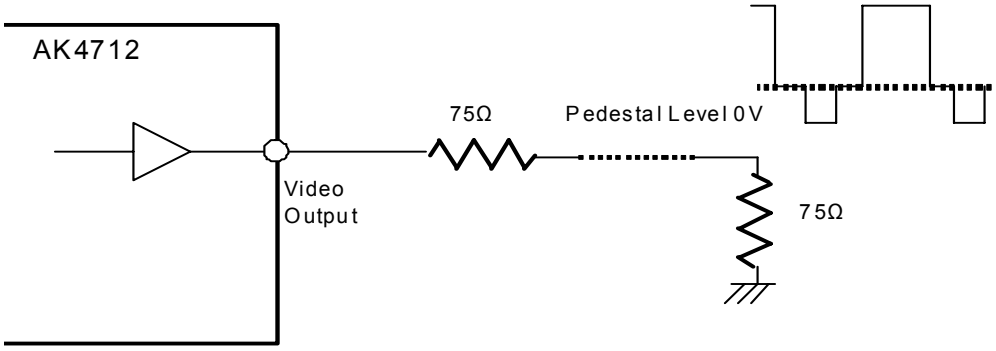


Figure 8. Video Output Block

4. Control Interface (I^2C-bus Control)

1. WRITE Operations

Figure 9 shows the data transfer sequence in I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 15). After the START condition, a slave address is sent. This address is 7bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4712, the AK4712 generates an acknowledge and the operation is executed. The master must generate an acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 17). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4712. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 11). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 12). The AK4712 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 15).
The AK4712 can execute more than one byte write operation per sequence. After receipt of the third byte, the AK4712 generates an acknowledge, and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving of each data packet, the internal address counter is incremented by one, and the next data is taken into the next address automatically. If the address exceeds 02H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 17) except for the START and the STOP conditions.

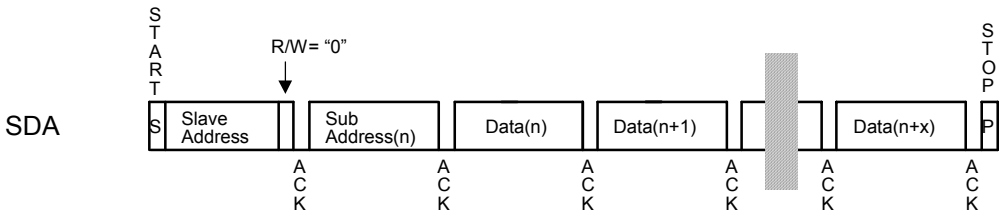


Figure 9. Data transfer sequence at the I^2C-bus mode

0	0	1	0	0	0	1	R/W

Figure 10. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 11. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 12. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After receiving each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 02H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4712 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4712 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit set to "1", the AK4712 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generate a stop condition instead, the AK4712 ceases transmission.

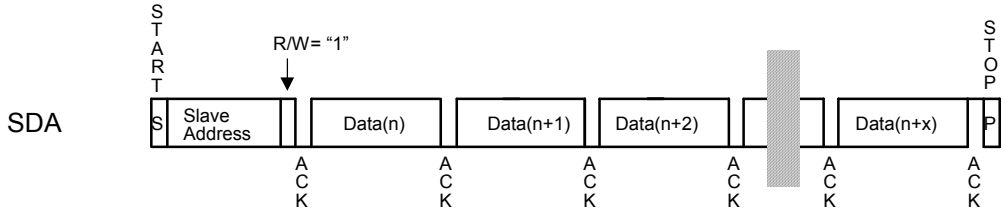


Figure 13. CURRENT ADDRESS READ

2-2. RANDOM READ

The Random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit set to "1", the master must execute a "dummy" write operation. The master issues a start condition, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". The AK4712 then generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge but generate a stop condition instead, the AK4712 ceases the transmission.

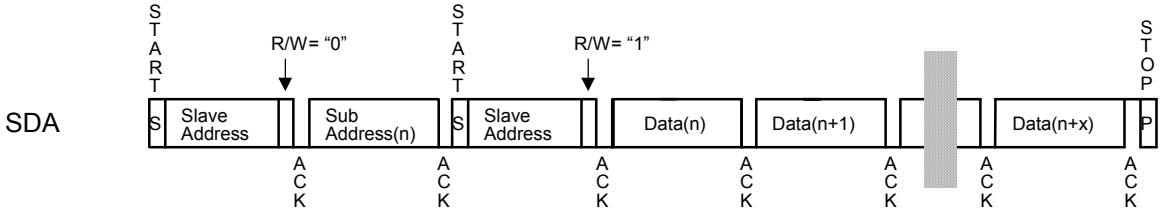


Figure 14. RANDOM ADDRESS READ

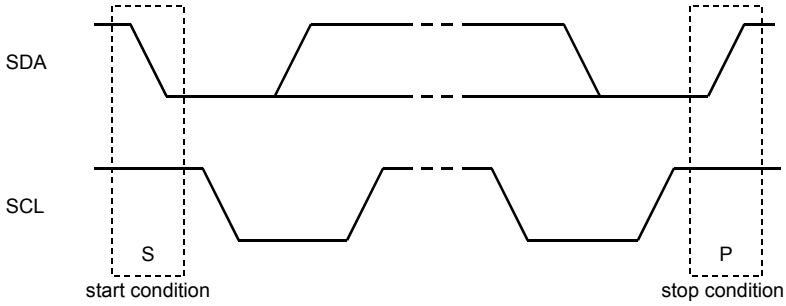


Figure 15. START and STOP Conditions

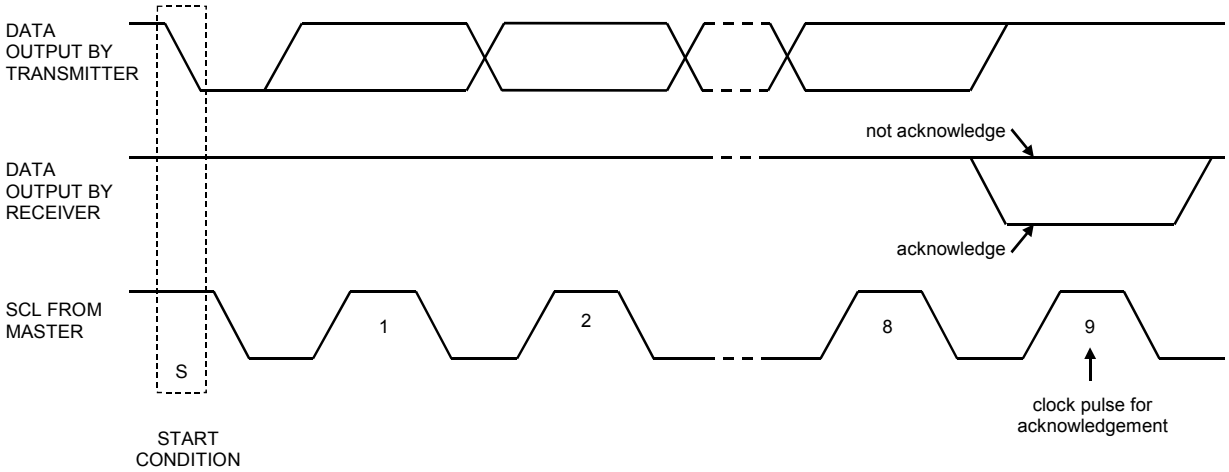


Figure 16. Acknowledge on the I^2C-bus

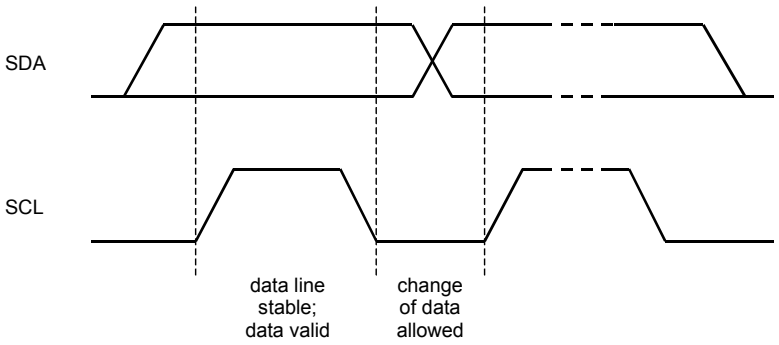


Figure 17. Bit Transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Audio Volume control	0	0	0	0	MOD	MDT1	MDT0	MUTEN
01H	Video control	FLT	DETN	CLAMP2	CLAMP1	FL1	FL0	HDAPW	SDAPW
02H	Reserve	0	0	0	0	0	0	0	0

When the PDN pin goes "L", the registers are initialized to their default values.
While the PDN pin = "H" and I2CSEL pin = "H", all registers can be accessed.
Do not write any data to the register over 02H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	MOD	MDT1	MDT0	MUTEN
R/W		R/W							
Default		0	0	0	0	1	1	0	1

MUTEN: Audio output control
0: ALL Audio outputs to GND
1: Normal operation (default)

MDT1-0: The time length control of mute/unmute transition time
00: typ. 5.1 ms / max. 11.6 ms
01: typ. 10.2 ms / max. 23.6 ms
10: typ. 20.5 ms / max. 46.8 ms
11: typ. 41.0 ms / max. 94.0 ms (default)

MOD: Soft transition enable for mute/unmute control
0: Disable
The audio output is muted/unmated immediately without soft transition.
1: Enable (default)
The audio output is muted/unmuted with soft transition.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Video Control	FLT	DETN	CLAMP2	CLAMP1	FL1	FL0	HDAPW	SDAPW
R/W		R/W							
Default		0	0	1	0	1	0	1	1

SDAPW: SD block power-up bit(SD Video output)
0: SD block power-down, RCAVOUT pin is Hi-z.
1: SD block power-up (default)

HDAPW: HD block power-up bit(HD Video output)
0: HD block power-down, HDY/HDPB/HDPR pins are Hi-z.
1: HD block power-up. (default)

FL1-0: HD Video Filter Control
Refer to Table 6.

CLAMP2, CLAMP1: Clamp control.
Refer to Table 7

DETN: Video input detector control of audio block
0: Power management of audio block is dependent on video input detector. (default).
1: Power management of audio block is independent from video input detector.

FLT: HD Sync detection filter (500kHz band-width)
0: filter OFF (default).
1: filter ON

SYSTEM DESIGN

Figure 18 shows the system connection diagram example (I2C mode). An evaluation board (AKD4712) demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

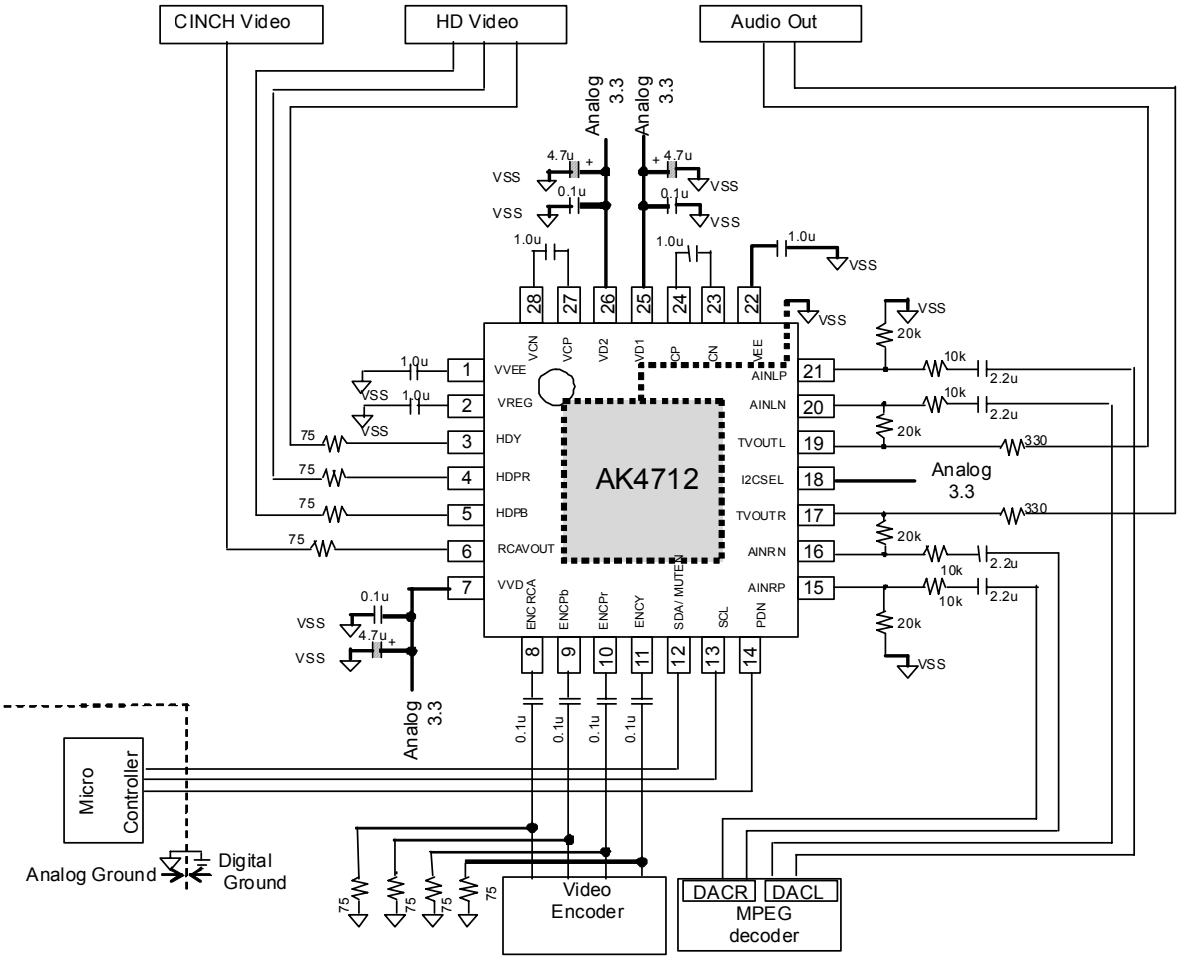


Figure 18. Typical Connection Diagram (I2C Mode: the I2CSEL pin = "H")

The SCL pin must be connected to the PDN pin when the I2CSEL pin = “L”

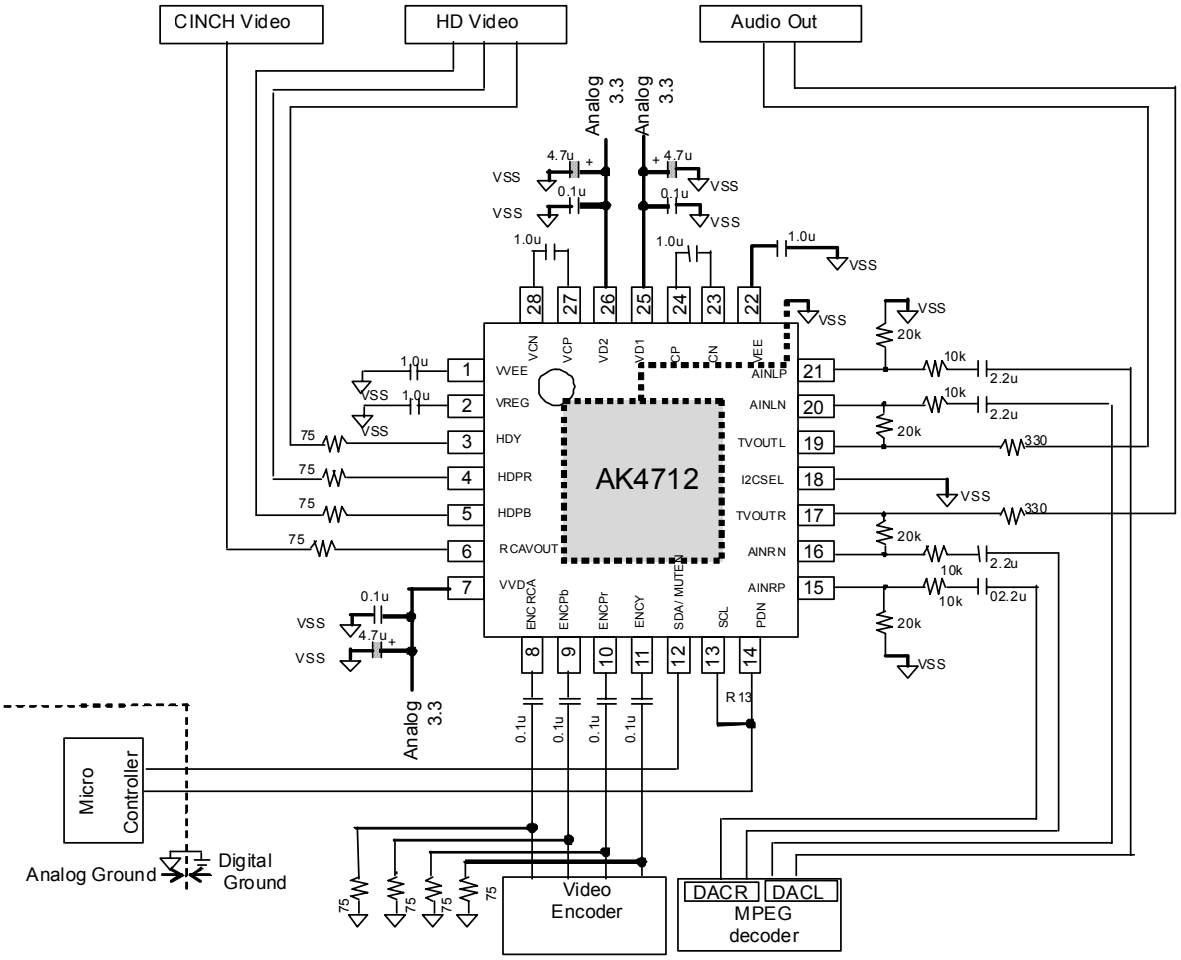


Figure 19. Typical Connection Diagram (Hard Wired Mode: the I2CSEL pin = “L”)

■ Grounding and Power Supply Decoupling

VD1, VD2, VVD should be supplied from analog supply unit with low impedance and be separated from system digital supply. A 4.7μF electrolytic capacitor parallel with a 0.1μF ceramic capacitor should be connected to each VD1 pin, VD2 pin, VVD pin, VSS (exposed pad) to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitors should be placed as near to the VD1 (VD2, VVD) pin as possible.

■ Analog Audio Outputs

The analog outputs are also single-ended and centered on 0V(typ.). The output signal ranges typically 2Vrms .

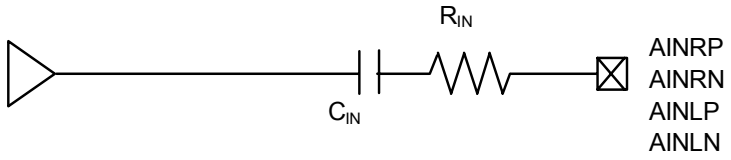
■ Attention to the PCB Wiring

AINLN and AINRN pins are the summing nodes of the Pre-Amp. Attention should be given to avoid coupling with other signals on those nodes. This can be accomplished by making the wire length of the input resistors and the feedback resistors as short as possible.

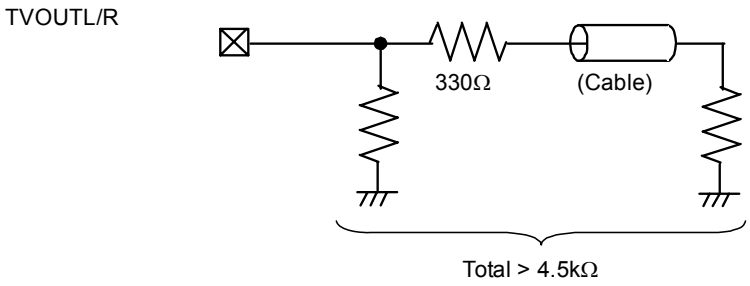
■ External Circuit Example

The analog audio input pin must have input series resistor(R_{IN}) and capacitor(C_{IN}).

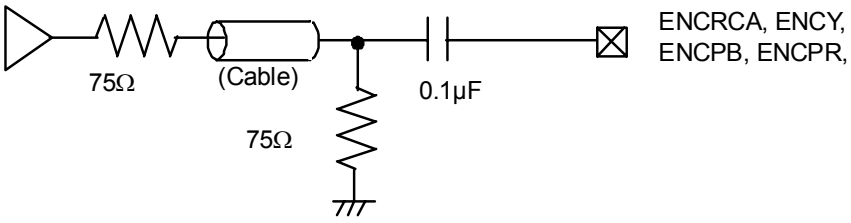
Analog Audio Input pin



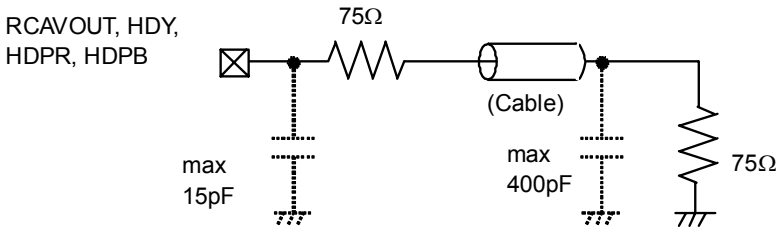
Analog Audio Output pin



Analog Video Input pin

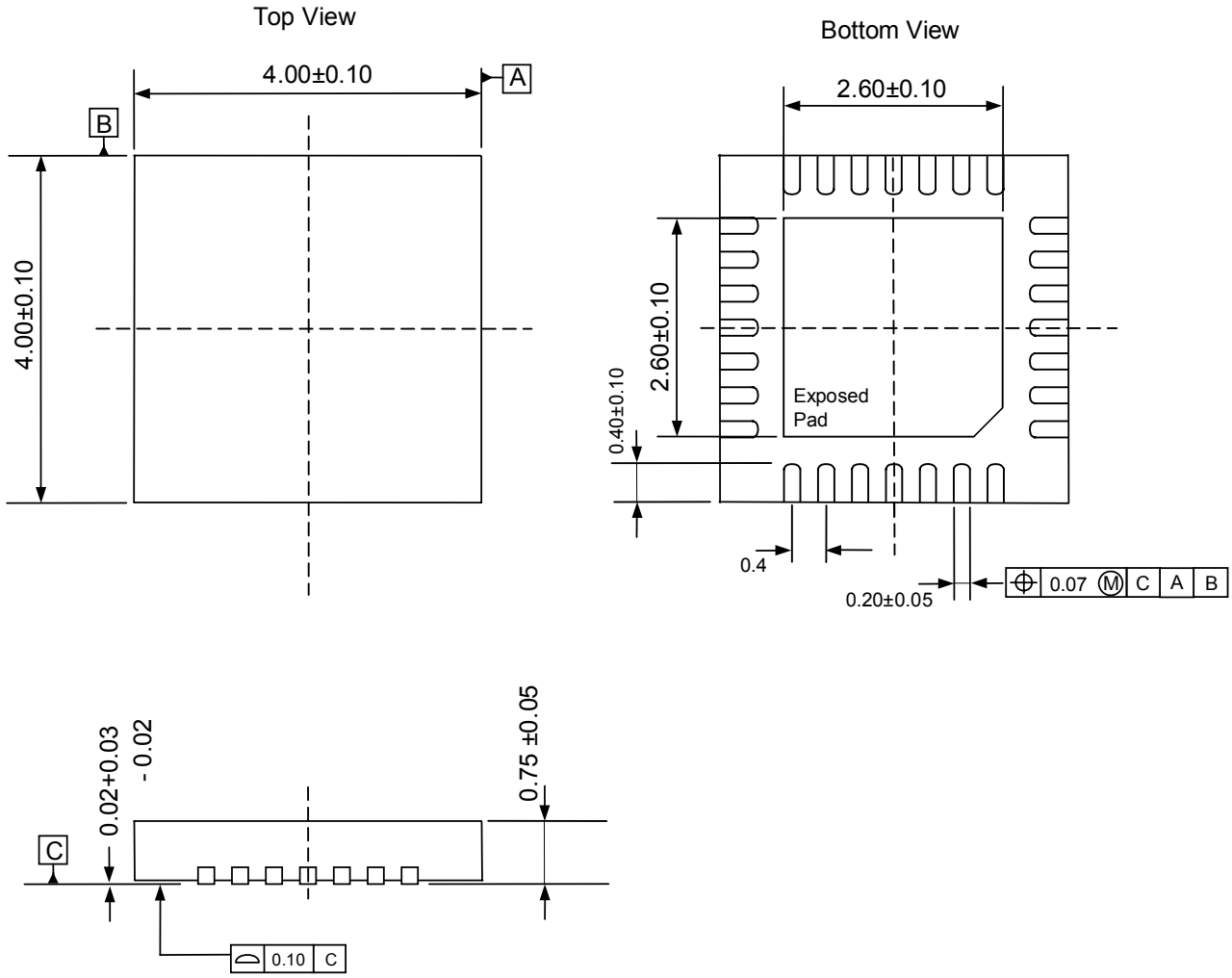


Analog Video Output pin



PACKAGE

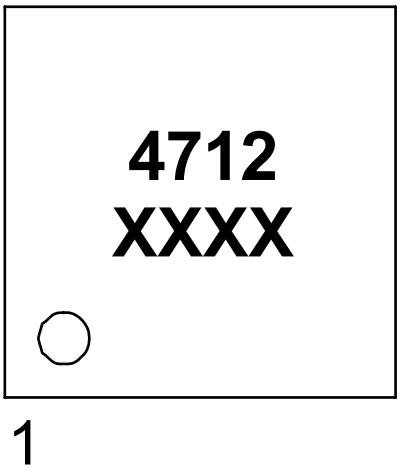
28pin QFN (Unit: mm)



■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code identifier: XXXX (4 digits)

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
13/01/30	00	First Edition		

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