1. General Description
The AK5720 is a low voltage 24-bit A/D converter for digital audio systems. The AK5720 includes an Input Gain Amplifier, making it suitable for microphone applications. The analog signal input of the AK5720 is single-ended, eliminating the need for external filters. The AK5720 is housed in a space-saving 16-pin TSSOP package.

2. Features
1. Resolution: 24bits
2. Recording Functions
   - Gain Amplifier (0dB / +15dB)
   - Digital HPF for DC-offset cancellation (fc=1.0Hz@fs=48kHz)
3. ADC Characteristics
   - Single-ended Input
   - Input Level: 1.8Vpp@VA=3.0V (= 0.6 × VA), 3.0Vpp@VA=5.0V (=0.6 × VA)
   - S/(N+D): 94dB
   - DR, S/N: 102dB
4. Master Clock: 256fs/384fs/512fs/768fs
5. Sampling Frequency: 8kHz ~ 96kHz
6. Audio Data Format: MSB First, 2’s compliment
   - 24-bit MSB justified, I²S and TDM
7. Power Supply
   - VA, VD: 2.7 ~ 5.5V (typ. 3V, 5V)
8. Power Supply Current: 6.1mA(VA-VD=5.0V, fs=48kHz)
9. Operating Temperature: Ta = -40 ~ 105°C
10. Package: 16-pin TSSOP
3. Table of Contents

1. General Description ............................................................................................................ 1
2. Features ................................................................................................................................ 1
3. Table of Contents .................................................................................................................. 2
4. Pin Configurations and Functions .......................................................................................... 3
   ▪ Ordering Guide .................................................................................................................. 3
   ▪ Pin Layout ......................................................................................................................... 3
   ▪ Functions ............................................................................................................................ 4
   ▪ Handling of Unused Pin ...................................................................................................... 4
5. Absolute Maximum Ratings ............................................................................................... 5
6. Recommended Operating Conditions ................................................................................ 5
7. Analog Characteristics (VA=VD=5.0V) ............................................................................... 6
8. Analog Characteristics (VA=VD=3.0V) ............................................................................... 7
9. Filter Characteristics (fs=48kHz) ...................................................................................... 8
10. Filter Characteristics (fs=96kHz) ..................................................................................... 9
11. DC Characteristics ............................................................................................................. 9
12. Switching Characteristics .................................................................................................. 10
   ▪ Timing Diagram ................................................................................................................ 12
13. Functional Descriptions .................................................................................................... 16
   ▪ System Clock ................................................................................................................... 16
   ▪ Audio Interface Format ................................................................................................... 16
   ▪ Digital High Pass Filter ................................................................................................... 18
   ▪ Power Down .................................................................................................................... 18
   ▪ System Reset ..................................................................................................................... 19
   ▪ TDM Cascade Mode .......................................................................................................... 19
14. Recommended External Circuits ..................................................................................... 21
15. Package .............................................................................................................................. 23
   ▪ Outline Dimensions ......................................................................................................... 23
   ▪ Material & Lead Finish .................................................................................................... 23
   ▪ Marking ............................................................................................................................. 24
16. Revision History .................................................................................................................. 24

IMPORTANT NOTICE................................................................................................................. 25
4. Pin Configurations and Functions

■ Ordering Guide

AK5720  
−40 ~ +105°C  
16-pin TSSOP (0.65mm pitch)

AKD5720  
Evaluation Board for AK5720

■ Pin Layout

<table>
<thead>
<tr>
<th>Pin</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
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<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCOM</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>RIN</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>VA</td>
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<td>GSEL</td>
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</tr>
<tr>
<td>REGO</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

Top View
### Functions

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
<th>Power Down Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCOM</td>
<td>O</td>
<td>ADC Common Voltage Output Pin</td>
<td>Pull-down to VSS with NMOS (0.5kΩ)</td>
</tr>
<tr>
<td>2</td>
<td>RIN</td>
<td>I</td>
<td>Rch Input Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>3</td>
<td>LIN</td>
<td>I</td>
<td>Lch Input Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
<td>-</td>
<td>Ground Pin</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>VA</td>
<td>-</td>
<td>Analog Power Supply Pin</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>VD</td>
<td>-</td>
<td>Digital Power Supply Pin</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>GSEL</td>
<td>I</td>
<td>Input Gain Select Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>“L”: 0dB, “H”: +15dB</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>REGO</td>
<td>O</td>
<td>Regulator Output Pin</td>
<td>Pull-down to VSS with 500Ω</td>
</tr>
<tr>
<td>9</td>
<td>SDTO</td>
<td>O</td>
<td>Audio Serial Data Output Pin</td>
<td>“L” (VSS)</td>
</tr>
<tr>
<td>10</td>
<td>LRCK</td>
<td>I/O</td>
<td>Input/Output Channel Clock Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>11</td>
<td>MCLK</td>
<td>I</td>
<td>Master Clock Input Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>12</td>
<td>BICK</td>
<td>I/O</td>
<td>Audio Serial Data Clock Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>13</td>
<td>PDN</td>
<td>I</td>
<td>Reset &amp; Power Down Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>“L”: Reset &amp; Power down, “H”: Normal operation</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>DIF/TDMI</td>
<td>I</td>
<td>Audio Data Format Select Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>“L”: MSB justified, “H”: I’S</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TDM Data Input Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>15</td>
<td>FSEL</td>
<td>I</td>
<td>Digital Filter select Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td>16</td>
<td>CKS</td>
<td>I</td>
<td>Mode Select Pin</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Parasitic capacitance of the pin should be less than 20pF.</td>
<td></td>
</tr>
</tbody>
</table>

Note: All digital input pins must not be allowed to float.

Note: The GSEL pin must be fixed to “H” or “L” when the PDN pin = “H” to avoid starting the test mode.

### Handling of Unused Pin

Unused I/O pins must be connected appropriately.

<table>
<thead>
<tr>
<th>Classification</th>
<th>Pin Name</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog</td>
<td>RIN, LIN</td>
<td>This pin should be open.</td>
</tr>
</tbody>
</table>
### 5. Absolute Maximum Ratings

(VSS=0V; Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supplies:</td>
<td>VA</td>
<td>−0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Analog</td>
<td>VD</td>
<td>−0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Input Current, Any Pin Except Supplies</td>
<td>IIN</td>
<td>-</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>Analog Input Voltage (LIN, RIN pins)</td>
<td>VINA</td>
<td>−0.3</td>
<td>VA+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Digital Input Voltage</td>
<td>VIND</td>
<td>−0.3</td>
<td>VD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>Ta</td>
<td>−40</td>
<td>105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes. The AK5720 will be damaged if a voltage higher than 2.5V is input to the REGO pin.

### 6. Recommended Operating Conditions

(VSS=0V; Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supplies</td>
<td>VA</td>
<td>2.7</td>
<td>3 or 5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Analog (VA pin)</td>
<td>VD</td>
<td>2.7</td>
<td>3 or 5</td>
<td>VA</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.
### 7. Analog Characteristics (VA=VD=5.0V)

(Ta=25°C; VA=VD=5.0V; fs=48kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADC Analog Input Characteristics:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>24</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input Voltage (Note 2)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain = 0dB</td>
<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>Vpp</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>0.48</td>
<td>0.53</td>
<td>0.58</td>
<td></td>
</tr>
<tr>
<td><strong>S/(N+D) (-1.0dBFS)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA=5V, Gain = 0dB</td>
<td>fs=48kHz, fs=96kHz</td>
<td>84</td>
<td>94</td>
<td>dB</td>
</tr>
<tr>
<td>VA=5V, Gain = +15dB</td>
<td>fs=48kHz, fs=96kHz</td>
<td>74</td>
<td>84</td>
<td>dB</td>
</tr>
<tr>
<td><strong>DR (-60dBFS)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA=5V, Gain = 0dB</td>
<td>fs=48kHz, A-weighted fs=96kHz</td>
<td>94</td>
<td>102</td>
<td>dB</td>
</tr>
<tr>
<td>VA=5V, Gain = +15dB</td>
<td>fs=48kHz, A-weighted fs=96kHz</td>
<td>83</td>
<td>91</td>
<td>dB</td>
</tr>
<tr>
<td><strong>S/N</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA=5V, Gain = 0dB</td>
<td>fs=48kHz, A-weighted fs=96kHz</td>
<td>94</td>
<td>102</td>
<td>dB</td>
</tr>
<tr>
<td>VA=5V, Gain = +15dB</td>
<td>fs=48kHz, A-weighted fs=96kHz</td>
<td>83</td>
<td>91</td>
<td>dB</td>
</tr>
<tr>
<td><strong>Input Resistance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain = 0dB</td>
<td>fs=48kHz fs=96kHz</td>
<td>29</td>
<td>41</td>
<td>kΩ</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>fs=48kHz fs=96kHz</td>
<td>15</td>
<td>22</td>
<td>kΩ</td>
</tr>
<tr>
<td><strong>Interchannel Isolation (RIN, LIN)</strong></td>
<td>Gain = 0dB</td>
<td>90</td>
<td>110</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>90</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Interchannel Gain Mismatch (RIN, LIN)</strong></td>
<td>0</td>
<td>0.5</td>
<td>dB</td>
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<tr>
<td><strong>Gain Drift</strong></td>
<td>100</td>
<td>ppm/°C</td>
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<td></td>
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<tr>
<td><strong>Power Supply Rejection</strong></td>
<td>(Note 3)</td>
<td>-</td>
<td>50</td>
<td>dB</td>
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</table>

### Power Supplies

<table>
<thead>
<tr>
<th>Power Supply Current</th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Normal Operation (PDN pin = “H”)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA</td>
<td>3.8</td>
<td>5.7</td>
<td>mA</td>
</tr>
<tr>
<td>VD (fs=48kHz)</td>
<td>2.3</td>
<td>3.5</td>
<td>mA</td>
</tr>
<tr>
<td>VD (fs=96kHz)</td>
<td>4.4</td>
<td>6.7</td>
<td>mA</td>
</tr>
<tr>
<td>Power down mode (PDN pin = “L”) (Note 4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA+VD</td>
<td>10</td>
<td>100</td>
<td>μA</td>
</tr>
</tbody>
</table>

Note 2. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage. Vin = 0.6 × VA (Vpp).

Note 3. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 4. All digital input pins and CKS1 pin are held VD or VSS.
8. Analog Characteristics (VA=VD=3.0V)

(Ta=25°C; VA=VD=5.0V; fs=48kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data;
Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise
specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Analog Input Characteristics:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td></td>
<td>24</td>
<td>Bits</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain = 0dB</td>
<td>1.65</td>
<td>1.8</td>
<td>1.95</td>
<td>Vpp</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>0.29</td>
<td>0.32</td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1.0dBFS)</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>VA=3V Gain = 0dB</td>
<td>84</td>
<td>94</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>71</td>
<td>81</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>VA=3V Gain = 0dB</td>
<td>84</td>
<td>94</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>71</td>
<td>81</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS)</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>VA=3V Gain = 0dB</td>
<td>90</td>
<td>98</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>90</td>
<td>98</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>VA=3V Gain = 0dB</td>
<td>90</td>
<td>98</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
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<td>98</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>S/N</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA=3V Gain = 0dB</td>
<td>29</td>
<td>41</td>
<td>-</td>
<td>kΩ</td>
</tr>
<tr>
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<td>15</td>
<td>22</td>
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<td>kΩ</td>
</tr>
<tr>
<td>Input Resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain = 0dB</td>
<td>29</td>
<td>41</td>
<td>-</td>
<td>kΩ</td>
</tr>
<tr>
<td>Gain = +15dB</td>
<td>15</td>
<td>22</td>
<td>-</td>
<td>kΩ</td>
</tr>
<tr>
<td>Interchannel Isolation</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain = 0dB</td>
<td>90</td>
<td>110</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Gain = +15dB</td>
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<td>110</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Interchannel Gain Mismatch</td>
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<td>0</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Drift</td>
<td>100</td>
<td>-</td>
<td>50</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
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<td>dB</td>
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<td>Power Supply Current</td>
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<tr>
<td>Normal Operation (PDN pin = “H”)</td>
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<tr>
<td>VA</td>
<td>3.4</td>
<td>5.1</td>
<td>mA</td>
<td></td>
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<tr>
<td>VD (fs=48kHz)</td>
<td>1.9</td>
<td>2.9</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VD (fs=96kHz)</td>
<td>3.7</td>
<td>5.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Power down mode (PDN pin = “L”)</td>
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<tr>
<td>VA+VD</td>
<td>10</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

Note 2. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.
Vin = 0.6 × VA (Vpp).

Note 3. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 4. All digital input pins and CKS1 pin are held VD or VSS.

MS1641-E-02 2014/12
### 9. Filter Characteristics (fs=48kHz)

(Ta=25°C; VA=VD=2.7 ~ 5.5V, fs=48kHz)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
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<tr>
<td><strong>ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (FSEL pin=&quot;L&quot;)</strong></td>
<td></td>
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<tr>
<td>Passband (Note 5)</td>
<td></td>
<td>±0.16dB</td>
<td>PB</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>−0.28dB</td>
<td>-</td>
<td>20.0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>−3.0dB</td>
<td>-</td>
<td>22.8</td>
<td>-</td>
</tr>
<tr>
<td>Stopband (Note 5)</td>
<td>SB</td>
<td>28.4</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>Stopband Attenuation</td>
<td>SA</td>
<td>71</td>
<td>-</td>
<td>-</td>
<td>dB</td>
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<tr>
<td>Group Delay Distortion 0 ~ 20.0kHz</td>
<td>ΔGD</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>l/fs</td>
</tr>
<tr>
<td>Group Delay (Note 6)</td>
<td>GD</td>
<td>-</td>
<td>15.5</td>
<td>-</td>
<td>l/fs</td>
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<td>PB</td>
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<td></td>
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<td>−0.28dB</td>
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<tr>
<td></td>
<td></td>
<td>−3.0dB</td>
<td>-</td>
<td>22.8</td>
<td>-</td>
</tr>
<tr>
<td>Stopband (Note 5)</td>
<td>SB</td>
<td>28.4</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
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<td>72</td>
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<td>Group Delay Distortion 0 ~ 20.0kHz</td>
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<td>-</td>
<td>-</td>
<td>2.4</td>
<td>l/fs</td>
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<tr>
<td>Group Delay (Note 6)</td>
<td>GD</td>
<td>-</td>
<td>5.5</td>
<td>-</td>
<td>l/fs</td>
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<td><strong>ADC Digital Filter (HPF):</strong></td>
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<td></td>
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<td>−0.5dB</td>
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<td>2.5</td>
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<td>−0.1dB</td>
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<td>6.5</td>
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</tbody>
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Note 5. The passband and stopband frequencies scale with fs.
For example, PB=0.45 × fs(@−0.1dB).

Note 6. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the output register.
### 10. Filter Characteristics (fs=96kHz)

(Ta=25°C; VA=VD=2.7 ~ 5.5V; fs=96kHz)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
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<th>typ</th>
<th>max</th>
<th>Unit</th>
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<td>kHz</td>
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<tr>
<td>±0.16dB</td>
<td></td>
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<td></td>
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<tr>
<td>-0.28dB</td>
<td></td>
<td>40.0</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>-3.0dB</td>
<td></td>
<td>45.6</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>Stopband (Note 5)</td>
<td>SB</td>
<td>56.8</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>Stopband Attenuation</td>
<td>SA</td>
<td>71</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Group Delay Distortion 0 ~ 20.0kHz</td>
<td>ΔGD</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>l/fs</td>
</tr>
<tr>
<td>Group Delay (Note 6)</td>
<td>GD</td>
<td>-</td>
<td>15.5</td>
<td>-</td>
<td>l/fs</td>
</tr>
<tr>
<td><strong>ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (FSEL pin=“H”)</strong></td>
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<td>kHz</td>
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<td>±0.16dB</td>
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<td>-0.28dB</td>
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<tr>
<td>-3.0dB</td>
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<td>45.6</td>
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<td>-</td>
<td>kHz</td>
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<tr>
<td>Stopband (Note 5)</td>
<td>SB</td>
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<td>kHz</td>
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<td>Stopband Attenuation</td>
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<td>dB</td>
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<tr>
<td>Group Delay Distortion 0 ~ 20.0kHz</td>
<td>ΔGD</td>
<td>-</td>
<td>-</td>
<td>2.4</td>
<td>l/fs</td>
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<td>l/fs</td>
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<td><strong>ADC Digital Filter (HPF):</strong></td>
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<td>-</td>
<td>Hz</td>
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<td>(Note 5)</td>
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<td>-</td>
<td>Hz</td>
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<td></td>
<td></td>
<td>-</td>
<td>13.0</td>
<td>-</td>
<td>Hz</td>
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</table>

Note 5. The passband and stopband frequencies scale with fs.
For example, PB=0.45 × fs(@-0.1dB).

Note 6. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the output register.

### 11. DC Characteristics

(Ta=25°C, VA=VD=2.7 ~ 5.5V)

<table>
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<tr>
<th>Parameter</th>
<th>Symbol</th>
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<th>typ</th>
<th>max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>High-Level Input Voltage</td>
<td>VIH</td>
<td>75%VD</td>
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<td>-</td>
<td>V</td>
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<tr>
<td>Low-Level Input Voltage</td>
<td>VIL</td>
<td>-</td>
<td>-</td>
<td>25%VD</td>
<td>V</td>
</tr>
<tr>
<td>High-Level Output Voltage (Iout=−80µA)</td>
<td>VOH</td>
<td>VD−0.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Low-Level Output Voltage (Iout=80µA)</td>
<td>VOL</td>
<td>-</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>Iin</td>
<td>-</td>
<td>-</td>
<td>±10</td>
<td>µA</td>
</tr>
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</table>
12. Switching Characteristics

\( \text{Ta}= -40^\circ \text{C} \sim 105^\circ \text{C}; \ \text{VA}= \text{VD}= 2.7 \sim 5.5 \text{V}; \ C_L= 20 \text{pF}, \text{unless otherwise specified} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Master Clock Timing</td>
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<tr>
<td>Master Clock</td>
<td>fCLK</td>
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<td>12.288</td>
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<td>Pulse Width Low</td>
<td>tCLKL</td>
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<tr>
<td>Pulse Width High</td>
<td>tCLKH</td>
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<tr>
<td>384fs:</td>
<td>fCLK</td>
<td>3.072</td>
<td>18.432</td>
<td>36.864</td>
<td>MHz</td>
</tr>
<tr>
<td>Pulse Width Low</td>
<td>tCLKL</td>
<td>11</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse Width High</td>
<td>tCLKH</td>
<td>11</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>512fs:</td>
<td>fCLK</td>
<td>4.096</td>
<td>24.576</td>
<td>24.576</td>
<td>MHz</td>
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<tr>
<td>Pulse Width Low</td>
<td>tCLKL</td>
<td>16</td>
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<td></td>
<td>ns</td>
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<tr>
<td>Pulse Width High</td>
<td>tCLKH</td>
<td>16</td>
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<tr>
<td>768fs:</td>
<td>fCLK</td>
<td>6.144</td>
<td>36.864</td>
<td>36.864</td>
<td>MHz</td>
</tr>
<tr>
<td>Pulse Width Low</td>
<td>tCLKL</td>
<td>11</td>
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<td>ns</td>
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<tr>
<td>Pulse Width High</td>
<td>tCLKH</td>
<td>11</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**LRCK Timing (Slave Mode)**

| Normal mode                    |        |      |      |      |       |
| LRCK Frequency                 | fs     | 8    | 96   |      | kHz   |
| Duty Cycle                     | Duty   | 45   | 55   |      | %     |

**TDM256 MODE**

| LRCK Frequency                 | fs     | 8    | 96   |      | kHz   |
| “H” time                       | tLRH   | 1/256fs |      |    | ns |
| “L” time                       | tLRL   | 1/256fs |      |    | ns |

**LRCK Timing (Master Mode)**

| Normal mode                    |        |      |      |      |       |
| LRCK Frequency                 | fs     | 8    | 96   |      | kHz   |
| Duty Cycle                     | Duty   | 50   |      |      | %     |

**TDM256 MODE**

| LRCK Frequency                 | fs     | 8    | 96   |      | kHz   |
| “H” time                       | tLRH   | 1/8fs |      |    | ns |

*Note 7.* It will be “L” time in \( ^1 \text{S} \) format.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
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<tbody>
<tr>
<td><strong>Audio Interface Timing (Slave mode)</strong></td>
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<tr>
<td><strong>Normal mode</strong></td>
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<tr>
<td>BICK Period</td>
<td>tBCK</td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BICK Pulse Width Low</td>
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<td>65</td>
<td></td>
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<tr>
<td>Pulse Width High</td>
<td>tBCKH</td>
<td>65</td>
<td></td>
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</tr>
<tr>
<td>LRCK Edge to BICK “↑” (Note 8)</td>
<td>tLRB</td>
<td>30</td>
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<td></td>
<td>ns</td>
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<tr>
<td>BICK “↑” to LRCK Edge (Note 8)</td>
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<td>LRCK to SDTO (MSB) (Except FS mode)</td>
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<tr>
<td>BICK “↓” to SDTO</td>
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<td>BICK Period</td>
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<tr>
<td>BICK Pulse Width Low</td>
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<td>ns</td>
</tr>
<tr>
<td>LRCK Edge to BICK “↑” (Note 8)</td>
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<td>BICK “↑” to LRCK Edge (Note 8)</td>
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<td>ns</td>
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<td>SDTO Setup time BICK “↑”</td>
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<td>TDMI Setup Time</td>
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<td>ns</td>
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<td><strong>Audio Interface Timing (Master mode)</strong></td>
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<td>BICK Frequency</td>
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<tr>
<td>BICK Duty</td>
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<td>%</td>
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<tr>
<td>BICK “↓” to SDTO</td>
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<td>BICK Frequency</td>
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<td>256fs</td>
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<td>ns</td>
</tr>
<tr>
<td>BICK Duty</td>
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<td></td>
<td></td>
<td>%</td>
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<tr>
<td>BICK “↓” to LRCK</td>
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<td>TDMI Hold Time</td>
<td>tSDH</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TDMI Setup Time</td>
<td>tSDS</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Power-Down & Reset Timing**

- **PDN Pulse Width** (Note 10) tPD 150 30 ns
- **PDN Reject Pulse Width** (Note 10) tRPD
- **PDN “↑” to SDTO valid** (Note 11) tPDV 4129 1/fs

---

**Notes:**

Note 8. BICK rising edge must not occur at the same time as LRCK edge.
Note 9. In the case of MCLK duty cycle is 50%.
Note 10. The AK5720 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must held “L” for more than 150ns for a certain reset. The AK5720 is not reset by the “L” pulse less than 30ns.
Note 11. This is the count of LRCK “↑” from the PDN pin = “H”.
Figure 1. Clock Timing (Slave mode)

Figure 2. Clock Timing (Master mode)
Figure 3. Audio Interface Timing (Normal mode & Slave mode)

Figure 4. Audio Interface Timing (TDM mode & Slave mode)
Figure 5. Audio Interface Timing (Normal mode & Master mode)

Figure 6. Audio Interface Timing (TDM mode & Master mode)
Figure 7. Power-down & Reset Timing
13. Functional Descriptions

**System Clock**

MCLK, BICK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = “L”. If the external clocks are not present, place the AK5720 in power-down mode (PDN pin = “L”). In master mode, the master clock (MCLK) must be provided unless PDN pin = “L”.

<table>
<thead>
<tr>
<th>fs</th>
<th>MCLK</th>
<th>128fs</th>
<th>192fs</th>
<th>256fs</th>
<th>384fs</th>
<th>512fs</th>
<th>768fs</th>
</tr>
</thead>
<tbody>
<tr>
<td>32kHz</td>
<td>N/A</td>
<td>N/A</td>
<td>8.192MHz</td>
<td>12.288MHz</td>
<td>16.384MHz</td>
<td>24.576MHz</td>
<td></td>
</tr>
<tr>
<td>44.1kHz</td>
<td>N/A</td>
<td>N/A</td>
<td>11.2896MHz</td>
<td>16.9344MHz</td>
<td>22.5792MHz</td>
<td>33.8688MHz</td>
<td></td>
</tr>
<tr>
<td>48kHz</td>
<td>N/A</td>
<td>N/A</td>
<td>12.288MHz</td>
<td>18.432MHz</td>
<td>24.576MHz</td>
<td>36.864MHz</td>
<td></td>
</tr>
<tr>
<td>96kHz</td>
<td>N/A</td>
<td>N/A</td>
<td>24.576MHz</td>
<td>36.864MHz</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. System Clock Example

**Audio Interface Format**

MCLK frequency, the relationship of BICK frequency and fs, and master/slave mode are set by external resistance value of the CKS pin and the CKS pin connection as shown in Table 2.

When the CKS pin is connected to GND or VA directly, or via an external 4.7kΩ resistor (Normal mode), the DIF/TDMI pin becomes an audio data format select pin. Two kinds of data formats: 24bit MSB justified and I²S formats can be chosen by the DIF pin. The audio data is output on the falling edge of BICK from the SDTO pin. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output and they are input in slave mode. In master mode, LRCK frequency is fixed to 1fs and the BICK frequency is fixed to 64fs.

When the CKS pin is connected to GND or the VA pin via an external resistor of 18kΩ or 82kΩ (TDM mode), the DIF/TDMI pin becomes a TDM data input pin. In TDM mode, the audio data is output on a rising edge of BICK from the SDTO pin. When inputting the SDTO output data to the TDMI pin, this SDTO data has a delay which fills set-up or hold time of BICK rising.

<table>
<thead>
<tr>
<th>Mode</th>
<th>CKS</th>
<th>DIF/TDMI</th>
<th>SDTO</th>
<th>Master/Slave</th>
<th>MCLK</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>&lt; 10Ω to GND (Short to GND)</td>
<td>L</td>
<td>MSB</td>
<td>Slave</td>
<td>256/384fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>≥ 48fs or 32fs</td>
</tr>
<tr>
<td>1</td>
<td>&lt; 10Ω to VA (Short to VA)</td>
<td>H</td>
<td>I²S</td>
<td>Master</td>
<td>512/768fs (8k≤fs≤48k)</td>
<td>L/H</td>
<td>64fs</td>
</tr>
<tr>
<td>2</td>
<td>4.7kΩ±10% to GND</td>
<td>L</td>
<td>MSB</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>3</td>
<td>4.7kΩ±10% to VA</td>
<td>H</td>
<td>I²S</td>
<td>Master</td>
<td>384fs (8k≤fs≤96k)</td>
<td>L/H</td>
<td>64fs</td>
</tr>
<tr>
<td>4</td>
<td>4.7kΩ±10% to VA</td>
<td>L</td>
<td>MSB</td>
<td>Master</td>
<td>512fs (8k≤fs≤48k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>5</td>
<td>18kΩ±10% to GND</td>
<td>TDMI</td>
<td>MSB</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>8</td>
<td>18kΩ±10% to VA</td>
<td>TDMI</td>
<td>I²S</td>
<td>Slave</td>
<td>256fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>9</td>
<td>82kΩ±10% to GND</td>
<td>TDMI</td>
<td>I²S</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>10</td>
<td>82kΩ±10% to VA</td>
<td>TDMI</td>
<td>I²S</td>
<td>Slave</td>
<td>256fs (8k≤fs≤96k)</td>
<td>H/L</td>
<td>64fs</td>
</tr>
</tbody>
</table>

Table 2. Operation Mode Select

Note 12. SDTO outputs 16-bit data when BICK=32fs.
Figure 8. Mode 0, 2, 4, 6 Timing (Normal mode, MSB justified)

Figure 9. Mode 1, 3, 5, 7 Timing (Normal mode, I2S Compatible)

Figure 10. Mode 8, 9 Timing (TDM256 mode, MSB justified)

Figure 11. Mode 10, 11 Timing (TDM256 mode, I2S Compatible)
**Digital High Pass Filter**

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

**Power Down**

The AK5720 is placed in the power-down mode by bringing the PDN pin to “L”. The digital filter is also reset at the same time. This reset should always be executed upon power-up. In power-down mode, VCOM becomes VSS level. The AK5720 will be in analog initialization cycle after exiting the power-down mode. Therefore, the SDTO output data becomes valid after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode when power up the AK5720. During initialization, both L and R channels of ADC digital data outputs are forced to “0” in 2’s complement. The ADC outputs settle as a data corresponding to the input signals after the end of initialization (this settling takes approximately group delay time).

---

**Figure 12. Power-down/up Timing Example**

**Notes:**

1. The PDN pin must be “L” when power up the AK5720 and set to “H” after all poweres are supplied.
2. The internal power-down state is released after 147456/ MCLK cycles.
3. There is a delay about 3~4fs from internal power-up to the start of initialization cycle.
4. Digital block of the ADC is initialized after internal power-down is released.
   - When start-up the AK5720, ADC input voltage should be operation common voltage.
   - A charge-up time of DC cut capacitor is necessary to wait until the RIN and LIN pins settle to the common voltage. When the external capacitor is 10µF, the status of these pin settles in τ= 400ms (typ).
5. Click noise occurs at the end of initialization in the digital part. Mute the ADC output externally if the click noise influences system applications.
6. Digital output corresponds to analog input has group delay (GD).
7. ADC outputs “0” data in power-down state.
■ System Reset

The AK5720 should be reset once by bringing the PDN pin to “L” after power-up. In slave mode, reset and power-down are released on the rising edge (falling edge in I²C compatible mode) of LRCK after setting the PDN pin = “H”. In master mode, reset and power-down are released by MCLK input after setting the PDN pin = “H”.

■ TDM Cascade Mode

TDM256mode
Four or less devices can be connected in cascades at the TDM256 mode. In Figure 13, the SDTO pin of device #1/#2/#3 is connected with the TDMI pin of device #2/#3/#4. It is possible to output 8 channel TDM data from the SDTO pin of device #4 as shown in Figure 14.

![Figure 13. Cascade TDM Connection Diagram](image-url)
Figure 14. Cascade TDM Timing (TDM256 Mode (Left Justified))
14. Recommended External Circuits

Figure 15 shows the system connection diagram. An evaluation board (AKD5720) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Note:
- All digital input pins should not be left floating.

Figure 15. Typical Connection Diagram
1. Grounding and Power Supply Decoupling

The AK5720 requires careful attention to power supply and grounding arrangements. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. VSS of the AK5720 must be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5720 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM is 50%VA and used as the common voltage of analog signals. The VCOM pin is connected to VSS. A 0.47μF ceramic capacitor should be connected as close to the VCOM pin as possible between VSS and the VCOM pin. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5720.

3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50%VA) with 41kΩ (typ@fs=48kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6×VA Vpp (typ). The ADC output data format is 2’s complement. The internal HPF removes the DC offset (includes the DC offset that is caused by the ADC).

The AK5720 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK5720 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. External Resistor of the CKS pin

The external resistor of the CKS pin should be close as possible to the pin and kept away from the signal lines to prevent noises into the CKS pin.
### 15. Package

#### Outline Dimensions

16pin TSSOP (Unit: mm)

![Diagram of 16pin TSSOP package]

**NOTE:** Dimension "*" does not include mold flash.

#### Material & Lead Finish

- **Package molding compound:** Epoxy
- **Lead frame material:** Cu
- **Lead frame surface treatment:** Solder (Pb free) plate
**Marking**

![Marking Diagram]

1) Pin #1 indication
2) Date Code: XXXYY (5 digits)
   - XXX: Week Code
   - YY: Factory Control Code
3) Marketing Code : 5720VT
4) Asahi Kasei Logo

---

### 16. Revision History

<table>
<thead>
<tr>
<th>Date (Y/M/D)</th>
<th>Revision</th>
<th>Reason</th>
<th>Page</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>14/04/17</td>
<td>00</td>
<td>First Edition</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 14/10/17     | 01       | Error Correction  | 22   | 3. Analog Inputs
   - The AK5720 samples the analog inputs at 64fs(@fs=48kHz).
   - The AK5720 samples the analog inputs at 64fs. |
| 14/12/18     | 02       | Error Correction  | 16   | Table 2 Mode 8-11
   - The tolerances of resistors were corrected.
   - $\pm 5\% \rightarrow \pm 10\%$ |
|              |          | Description Change| 16   | Table 2 and Table 3 were combined. |
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