# AK7719B

## Low Power DSP for Voice and Audio Processing

## 1. General Description

The AK7719B is a highly integrated digital signal processor (DSP) with five digital interface ports. The built-in asynchronous sample rate converter (SRC) enables flexible connectivity in various system configurations. AKM's DSP core is optimized for both narrowband and wideband voice processing, as well as full bandwidth digital audio processing. An integrated clock generator for the DSP master clock eliminates the need for external clocks. The RAM-based DSP can be programmed for user requirements. The AK7719B is housed in a 30-pin CSP package. It is a very low power device, suitable for mobile applications.

## 2. Features

□ **Embedded DSP**
- **Flexible programming with built-in program and data memories**
- **Hardware accelerator**
- **Word length: 24-bits (Data RAM 24-bit floating point)**
- **Multiplier 20 x 20 → 40-bits (double precision available)**
- **Divider 20 / 20 → 20-bits**
- **ALU: 44-bit arithmetic operation (with 4-bit overflow margin)**
  **24-bit floating point arithmetic and logic operation**
- **Program RAM: 4096w x 36-bits**
- **Coefficient RAM: 2048w x 20-bits**
- **Data RAM: 2048w x 24-bits (24-bit floating point)**
- **Offset Register: 32w x 15-bits**
- **Delay RAM: 16384w x 24-bits(24-bit floating point)**
- **5625 steps at 16kHz sampling rate, 1875 steps at 48kHz sampling rate**
- **Internal clock generator**

□ **Audio Interface Format**
- **Left justified, PCM, $I^2S$,**
- **16/24bit linear**
- **Sampling rate 8kHz ~ 48kHz**
- **Up/Down Sampling Rate Converter: Port#1 (8kHz ↔ 16kHz)**

□ **Asynchronous Sample Rate Converters**

□ **µC I/F: $I^2C$-Compatible, SPI**

□ **Operational, Sleep and Power-down Modes**

□ **Power Supply**
**VDD (DSP Core): 1.2V ±0.1V**
**TVDD (PCM I/F): 1.6V ~ 3.6V**

□ **Operating Temperature Range: -40°C ~ 85°C**

□ **Package: 30-Pin WL-CSP (2.94mm x 3.14mm, 0.5mm pitch)**

□ **Power Consumption: 9.2mA (11mW) typ. (Narrowband Handset mode operation)**

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# 4. Block Diagram

## ■ Block Diagram

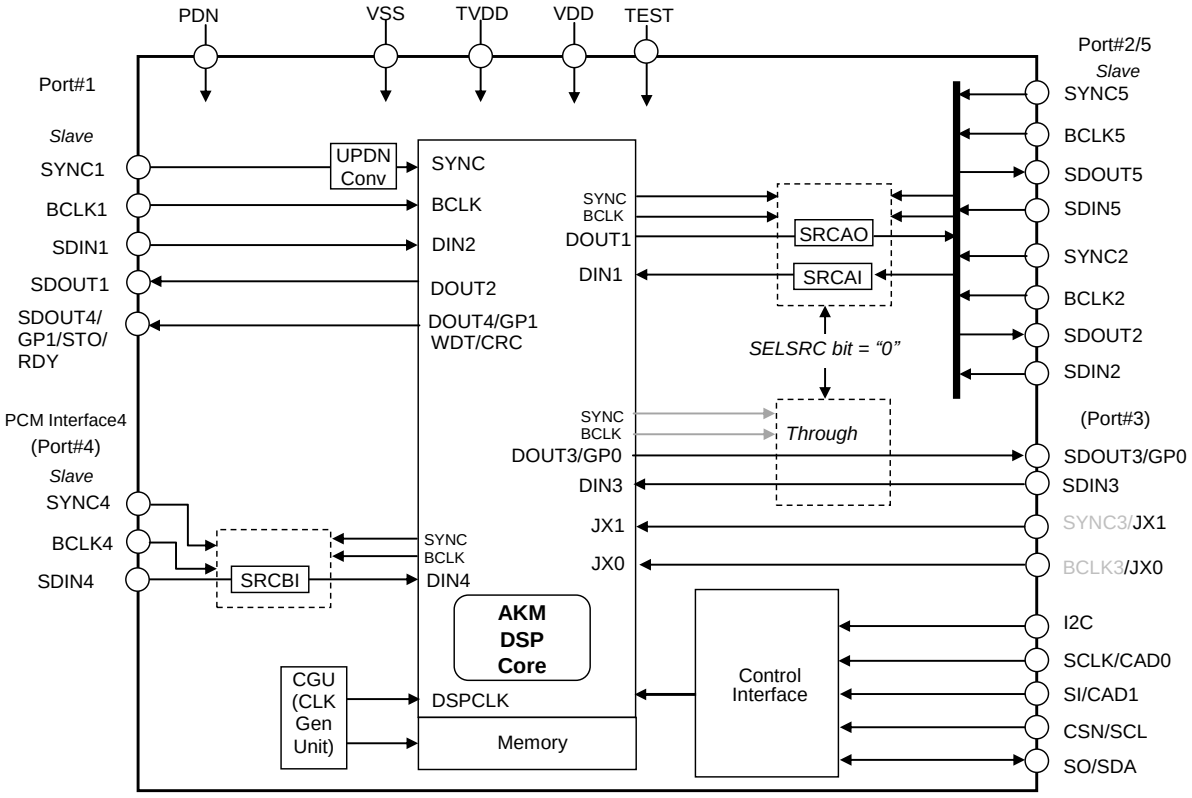



Figure 1. Block Diagram (SELSRC bit = "0")

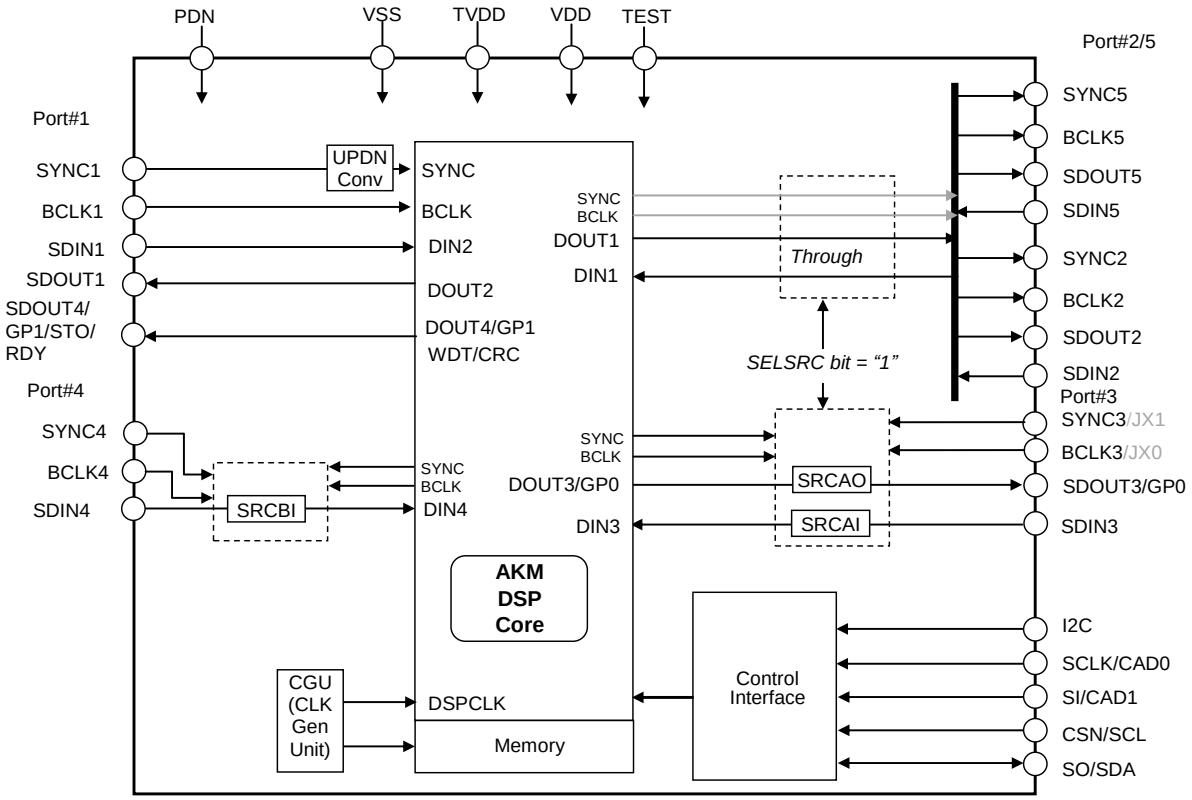
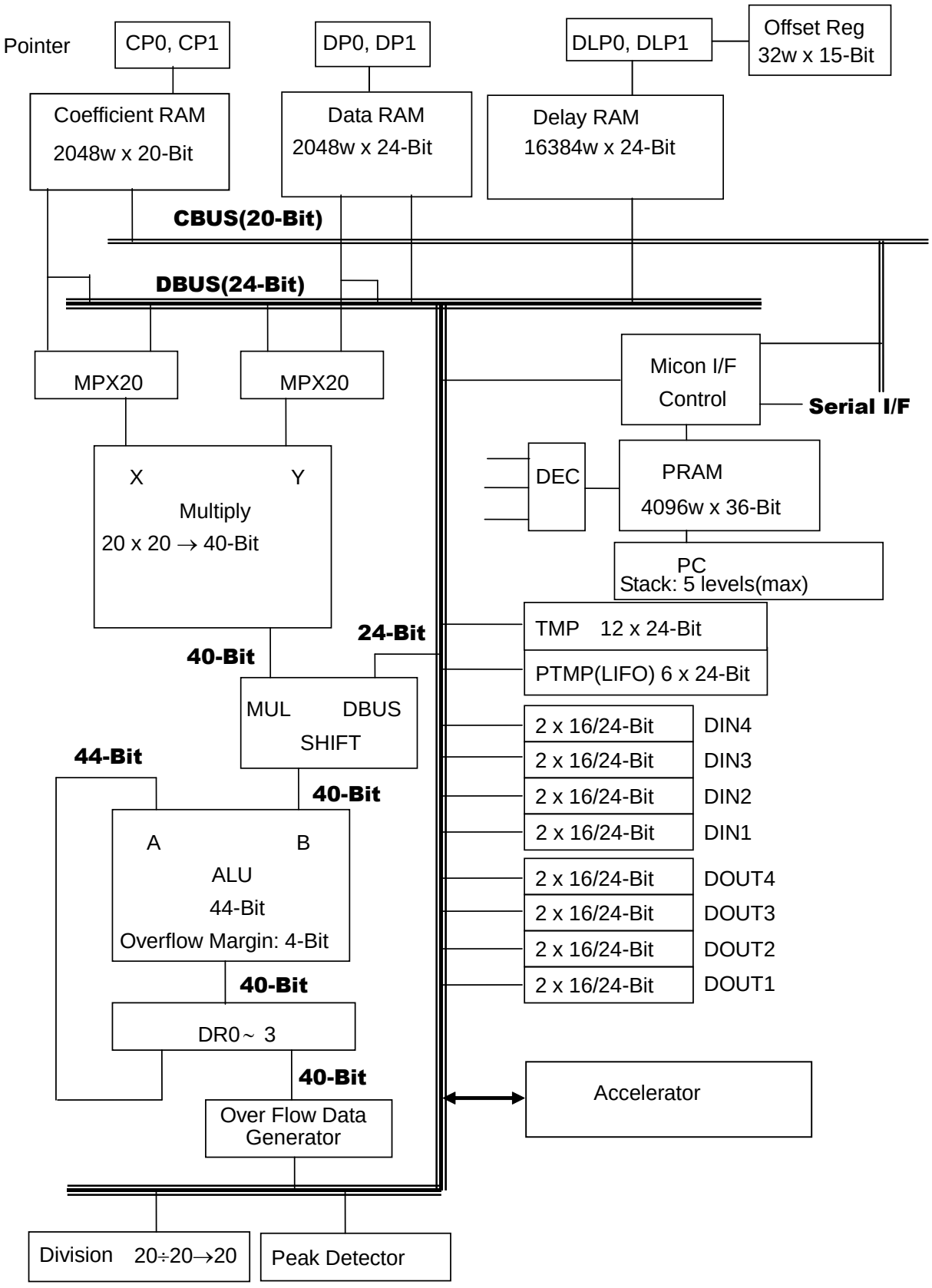



Figure 2. Block Diagram (SELSRC bit = "1")

## ■ DSP Block Diagram

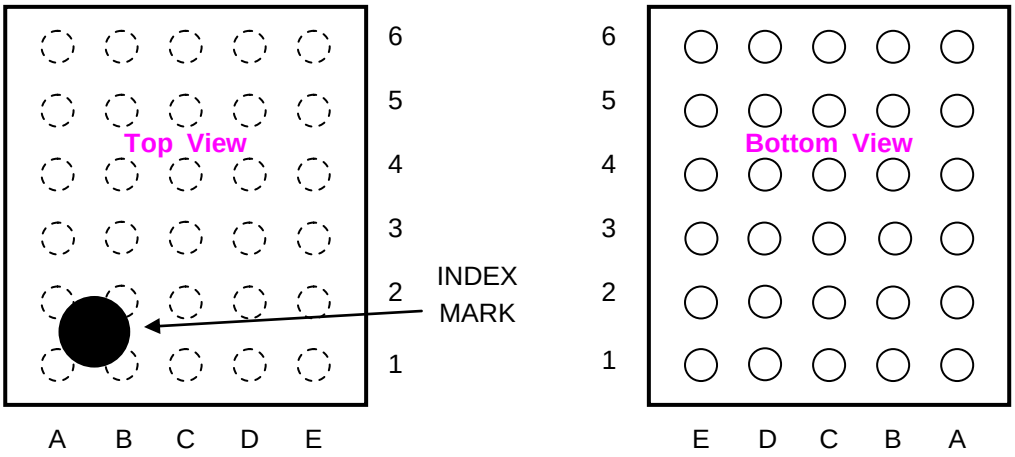


## 5. Pin Configurations and Functions

### ■ Ordering Guide

| | | |
|---|---|---|
| AK7719BECB | -40 ~ +85°C | 30-pin CSP (0.5mm pitch) Black type |
| AKD7719 | Evaluation board for AK7719B | |

### ■ Pin Layout




| | | | | | |
|---|---|---|---|---|---|
| 6 | PDN | SDIN1 | SDOUT1 | BCLK1 | SYNC1 |
| 5 | VDD | BCLK3/ JX0 | SDIN3 | SDOUT3/ GP0 | SYNC2 |
| 4 | VSS | SYNC3/ JX1 | TEST | SDOUT5 | BCLK2 |
| 3 | TVDD | I2C | SDIN4 | SDOUT 4 /GP1/STO/ RDY | SDIN2 |
| 2 | SI/CAD1 | SCLK/ CAD0 | CSN/ SCL | SO/SDA | SDOUT2 |
| 1 | BCLK4 | SYNC4 | SDIN5 | BCLK5 | SYNC5 |
| | A | B | C | D | E |

**TOP View**

## ■ Pin Function

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| A5 | VDD | - | Core Power Supply Pin 1.2V |
| A3 | TVDD | - | I/O power Supply Pin 1.6~3.6V |
| A4 | VSS | - | Ground Pin 0V |
| A6 | PDN | I | Power-Down Mode Pin<br>"H": Power-up, "L": Power-down, reset the control register.<br>The AK7719B must be reset once upon power-up. |
| E6 | SYNC1 | I | Frame Sync 1 pin |
| D6 | BCLK1 | I | Serial Data Clock 1 Pin<br>AK7719B goes into stanby state when BCLK1 is not present. |
| B6 | SDIN1 | I | Serial Data Input 1 Pin |
| C6 | SDOUT1 | O | Serial Data Output 1 Pin |
| D3 | SDOUT4 | O | Serial Data Output 4 Pin (SELDO4[1:0] bits = "00") |
| | GP1 | | DSP Programmable output 1 Pin (SELDO4[1:0] bits = "01") |
| | STO | | Status Output Pin (Active High) (SELDO4[1:0] bits = "10") |
| | RDY | | Data Write Ready output pin for control I/F (SELDO4[1:0] bits = "11") |
| E5 | SYNC2 | I | Frame Sync 2 Pin (Internal Pull-down pin) (PT25N bit = "0") |
| | | O | Frame Sync 2 Pin (PT25N bit = "1") |
| E4 | BCLK2 | I | Serial Data Clock 2 Pin (Internal Pull-down pin) (PT25N bit = "0") |
| | | O | Serial Data Clock 2 Pin (PT25N bit = "1") |
| E3 | SDIN2 | I | Serial Data Input 2 Pin |
| E2 | SDOUT2 | O | Serial Data Output 2 Pin ("L" output at PORTSEL25 bit= "1") |
| B4 | SYNC3 | I | Frame Sync 3 pin (SELSRC bit = "1") |
| | JX1 | | Conditional Jump 1 Pin (SELSRC bit = "0") |
| B5 | BCLK3 | I | Serial Data Clock 3 Pin (SELSRC bit = "1") |
| | JX0 | | Conditional Jump 0 Pin (SELSRC bit = "0") |
| C5 | SDIN3 | I | Serial Data Input 3 Pin |
| D5 | SDOUT3 | O | Serial Data Output 3 Pin (SELDO3 bit = "0") |
| | GP0 | | DSP Programmable output 0 Pin (SELDO3 bit = "1") |
| B1 | SYNC4 | I | Frame Sync 4 Pin |
| A1 | BCLK4 | I | Serial Data Clock 4 Pin |
| C3 | SDIN4 | I | Serial Data Input 4 Pin |
| E1 | SYNC5 | I | Frame Sync 5 Pin (Internal Pull-down pin) (PT25N bit = "0") |
| | | O | Frame Sync 5 Pin (PT25N bit = "1") |
| D1 | BCLK5 | I | Serial Data Clock 5 Pin (Internal Pull-down pin) (PT25N bit = "0") |
| | | O | Serial Data Clock 5 Pin (PT25N bit = "1") |
| C1 | SDIN5 | I | Serial Data Input 5 Pin |
| E4 | SDOUT5 | O | Serial Data Output 5 Pin ( "L" output at PORTSEL25 bit= "0") |
| B3 | I2C | I | Control Interface Mode Select Pin "H": $I^2C$, "L": SPI |
| B2 | SCLK | I | Serial Clock Input pin SPI (I2C pin = "L") |
| | CAD0 | | Slave Address 0 Input pin $I^2C$ (I2C pin = "H") |
| C2 | CSN | I | Chip select pin SPI (I2C pin = "L") |
| | SCL | | Control Interface clock input pin $I^2C$ (I2C pin = "H") |
| D2 | SO | O | Serial data output pin SPI (I2C pin = "L") |
| | SDA | I/O | Control Interface input/output acknowledge pin $I^2C$ (I2C pin = "H") |
| A2 | SI | I | Serial data input pin SPI (I2C pin = "L") |
| | CAD1 | | Slave Address 1 Input pin $I^2C$(I2C pin = "H") |
| C4 | TEST | I | Test pin (pull-down resistor) must be connected to VSS. |

Note 1. All input pins must not be allowed to float.
Note 2. $I^2C$ and CAD0/1 pins must be fixed to "L" (VSS) or "H" (TVDD).

## ■ Handling of Unused Pins

Unused I/O pins must be connected appropriately:

| Pin Name | Setting |
|---|---|
| ,SDOUT3/GPO, SDOUT4/GP1/STO/RDY, SDOUT5 | Leave Open |
| SYNC2, BCLK2, SYNC5, BCLK5<br>SYNC3/JX1, BCLK3/JX0, SDIN3, TEST<br>SYNC4, BCLK4, SDIN4,<br>SYNC5, BCLK5, SDIN5, | Connect to VSS. |

## ■ Pin States in Power-down Mode

The table below shows pin states when the PDN pin= "L".

| No. | Pin Name | I/O (Note 3) | Power Down Pin State |
|---|---|---|---|
| C6 | SDOUT1 | O | "L" Output |
| E5 | SYNC2 | I/O | Input (internal pull-down) |
| E4 | BCLK2 | I/O | Input (internal pull-down) |
| E1 | SYNC5 | I/O | Input (internal pull-down) |
| D1 | BCLK5 | I/O | Input (internal pull-down) |
| E2 | SDOUT2 | O | "L" Output |
| D5 | SDOUT3 | O | "L" Output |
| | GP0 | | |
| D3 | SDOUT4 | O | "L" Output |
| | GP1 | | |
| | STO | | |
| | RDY | | |
| D4 | SDOUT5 | O | "L" Output |
| D2 | SO | O | SPI (I2C pin = "L") "L" Output |
| | SDA | I/O | $I^2C$ (I2C pin = "H") Hi-z |

Note 3. Indicates the pin attribute.

## 6. Absolute Maximum Ratings

(VSS=0V; All voltages are with respect to ground.)

| Parameter | Symbol | min | max | Unit |
|---|---|---|---|---|
| Power Supply Voltage (DSP Core) | VDD | –0.3 | 1.6 | V |
| Power Supply Voltage (Digital I/O) | TVDD | –0.3 | 4.1 | V |
| Input Current (except for power supply pins) | IIN | - | ±10 | mA |
| Input Voltage | VIND | –0.3 | TVDD+0.3 | V |
| Operating Ambient Temperature | Ta | –40 | 85 | °C |
| Storage Temperature | Tstg | –65 | 150 | °C |

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## 7. Recommended Operation Condition

(VSS=0V; All voltages are with respect to ground.)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply Voltage Range (DSP core) | VDD | 1.1 | 1.2 | 1.3 | V |
| Supply Voltage Range (I/Os) | TVDD | 1.6 | 1.8 | 3.6 | V |

Note 4. The power-up sequence with VDD and TVDD is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
Note 5. The external pull-up resistors at the SDA and SCL pins should be connected to TVDD voltage or less.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

## 8. SRC Characteristics

(Ta= -40°C~85°C; VDD=1.2V, TVDD=1.8V; VSS=0V; Signal Frequency = 1kHz, data = 24bit; Measurement Bandwidth = 20Hz~FSO/2kHz; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Resolution | | | | 24 | Bits |
| Input Sample Rate | FSI | 8 | | 48 | kHz |
| Output Sample Rate | FSO | 8 | | 48 | kHz |
| THD+N (Input= 1kHz, 0dBFS)<br>FSO/FSI=48kHz/8kHz<br>FSO/FSI=16kHz/48kHz<br>FSO/FSI=8kHz/48kHz | | | <br>-111<br>-113<br>-113 | <br>-103 | <br>dB<br>dB<br>dB |
| Dynamic Range (Input= 1kHz, -60dBFS)<br>FSO/FSI=48kHz/8kHz<br>FSO/FSI=16kHz/48kHz<br>FSO/FSI=8kHz/48kHz | | <br>108 | <br>113<br>113<br>111 | | <br>dB<br>dB<br>dB |
| Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)<br>FSO/FSI=8kHz/48kHz | | | <br>110 | | dB<br>dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.167 | | 6 | - |

## 9. DC Characteristics

(Ta=-40ºC~85ºC; VDD=1.2V, TVDD =1.6V~3.6V; VSS =0V)

| Parameter | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | 2.2V≤TVDD≤3.6V | VIH | 70%TVDD | | | V |
| | 1.6V≤TVDD<2.2V | VIH | 80%TVDD | | | |
| Low level input voltage | 2.2V≤TVDD≤3.6V | VIL | | | 30%TVDD | V |
| | 1.6V≤TVDD<2.2V | VIL | | | 20%TVDD | |
| High level inptu voltage Iout=-200μA (Note 6) | | VOH | TVDD-0.2 | | | V |
| Low level input voltage Iout= 200μA (Note 6) | | VOL | | | 0.2 | V |
| SDA low level output voltage Iout=3mA | TVDD ≥ 2.0V | VOL | | | 0.4 | V |
| | TVDD < 2.0V | | | | 20%TVDD | V |
| Input leak current | | Iin | | | ±10 | μA |
| Pull down resistance (Note 7) | | Rpd | | 40 | | kΩ |

Note 6. Except for the SDA pin.

Note 7. The SYNC2, BCLK2, SYNC5 and BCLK5 pins are internally pulled-down (PDS2 bit = PDS5 bit= “0” (default)).

## 10. Power Consumption

(Ta=25ºC; VSS =0V, unless otherwise specified.)

| Parameter | | | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| **Power Supplies:** | | | | | | |
| Power-Up (PDN pin = "H") | | | | | | |
| Loopback mode (DSP reset mode, SRCA, B: Powe-down) Port1(fs=8kHz, $I^2S$ fin=1kHz, slave mode) to Port2(master mode) | | | | | | |
| | VDD | VDD=1.2V | - | 0.8 | - | mA |
| | TVDD | TVDD=1.8V | - | 0.6 | - | mA |
| | Power Consumption | | - | 2.1 | | mW |
| All Circuit Power-up (Note 9) (DSP, SRC power-up running at Port#1: fs=8kHz, Port#2/4: fs=48kHz) | | | | | | |
| | VDD | VDD=1.3V | - | - | 36 | mA |
| | TVDD | TVDD=3.6V | - | - | 2 | mA |
| | Power Consumption | | - | - | 54 | mW |
| Power-Down state (PDN pin = "L"), (Note 8) | | | | | | |
| | VDD | VDD=1.2V | - | 2.4 | 8 | μA |
| | TVDD | TVDD=1.8V | - | 0.2 | 1 | μA |

Note 8. All digital input pins are fixed to TVDD or VSS.

Note 9. The current of VDD, TVDD changes depending on the system frequency and contents of the DSP program.

## 11. Filter Characteristics

### ■ SRC Block

(Ta= -40°C~85°C, VDD=1.1V~1.3V, TVDD=1.6~3.6V, VSS =0V)

| Parameter | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Passband -0.01dB | 0.980≦FSO/FSI≦6.000 | PB | 0 | | 0.4583FSI | kHz |
| | 0.900≦FSO/FSI＜0.990 | PB | 0 | | 0.4167FSI | kHz |
| | 0.533≦FSO/FSI＜0.909 | PB | 0 | | 0.2182FSI | kHz |
| | 0.490≦FSO/FSI＜0.539 | PB | 0 | | 0.2177FSI | kHz |
| | 0.450≦FSO/FSI＜0.495 | PB | 0 | | 0.1948FSI | kHz |
| | 0.225≦FSO/FSI＜0.455 | PB | 0 | | 0.1312FSI | kHz |
| Passband -0.50dB | 0.167≦FSO/FSI＜0.227 | PB | 0 | | 0.0658FSI | kHz |
| Stopband | 0.980≦FSO/FSI≦6.000 | SB | 0.5417FSI | | | kHz |
| | 0.900≦FSO/FSI＜0.990 | SB | 0.5021FSI | | | kHz |
| | 0.533≦FSO/FSI＜0.909 | SB | 0.2974FSI | | | kHz |
| | 0.490≦FSO/FSI＜0.539 | SB | 0.2812FSI | | | kHz |
| | 0.450≦FSO/FSI＜0.495 | SB | 0.2604FSI | | | kHz |
| | 0.225≦FSO/FSI＜0.455 | SB | 0.1802FSI | | | kHz |
| | 0.167≦FSO/FSI＜0.227 | SB | 0.0970FSI | | | kHz |
| Passband Ripple | 0.225≦FSO/FSI≦6.000 | PR | | | ±0.01 | dB |
| | 0.167≦FSO/FSI＜0.227 | PR | | | ±0.50 | dB |
| Stopband Attenuation | 0.450≦FSO/FSI≦6.000 | SA | | 95.2 | | dB |
| | 0.167≦FSO/FSI＜0.455 | SA | | 90.0 | | dB |
| Group Delay (Note 10) | | GD | | 52.5×Tsi + 9.5×Tso | | Sec |

Note 10. Group delay is a calculated time from a rising edge of SYNC at the input to a rising edge of SYNC at the output.

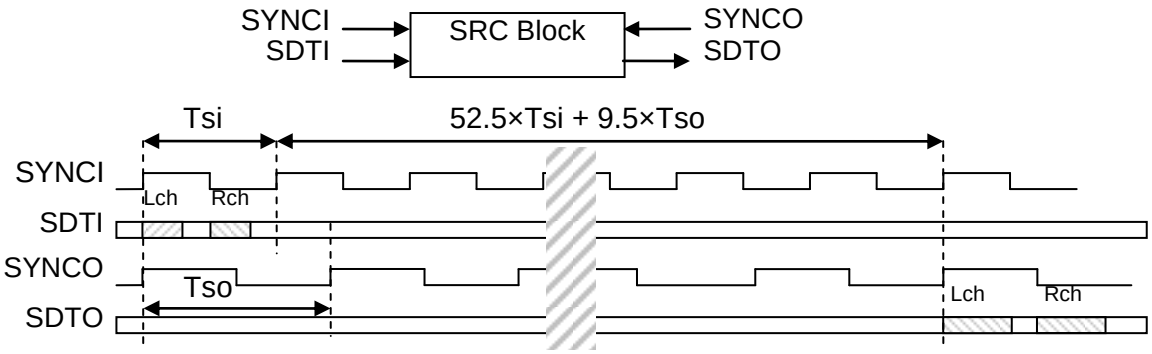



Figure 3. SRC Filter Group Delay (Left Justified)

# 12. Switching Characteristics

## ■ System Clock

(Ta= -40ºC ~ 85ºC, VDD=1.2V, TVDD= 1.6V ~ 3.6V, VSS=0V); CL=20pF (except SDA pin) or 400pF (SDA pin); unless otherwise specified)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| **Normal Operation mode: SYNCx, BCLKx (x=1~5) Input Timing** (Note 11) | | | | | |
| Input Timing | | | | | |
| SYNCx frequency | fs | 8 | | 48 | kHz |
| BCLKx Input Timing (Note 12) | fBCLK | 256 | | 4096 | kHz |
| BCLKx Pulse width Low | tBCKL | 0.4 x tBCLK | | | ns |
| BCLKx Pulse width High | tBCKH | 0.4x tBCLK | | | ns |

Note 11. SYNCx and BCLKx (x=1~5) should be synchronized and their sampling rates (fs) should be stable for each port.

Note 12. Required to meet the following expression: fBCLK ≥ 2 (Data length) × SYNCx frequency.

## ■ Reset and Power-down

(Ta= -40ºC ~ 85ºC, VDD=1.2V, TVDD= 1.6V ~ 3.6V, VSS=0V)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| PDN (Note 13) | tPDN | 600 | | | ns |

Note 13. The AK7719B can be reset by bringing the PDN pin = "L" upon power-up.

## ■ Serial Data Interface

(Ta= -40ºC ~ 85ºC, TVDD= 1.6V ~ 3.6V, VSS=0V, CL=20pF)

| Parameter | Symbols | min | typ | max | Unit |
|---|---|---|---|---|---|
| **SDINx, SDOUTx (x = 1~5) (x=2, 5: slave mode)** | | | | | |
| Delay Time from BCLKx "↑" to SYNCx "↑" (Note 14) | tBSYD | 20 | | | ns |
| Delay Time from SYNCx "↓" to BCLKx "↑" (Note 14) | tSYBD | 100 | | | ns |
| Serial Data Input Latch Setup Time | tB1IDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tB1IDH | 40 | | | ns |
| Delay Time from SYNC1 to Serial Data Output | tSY1OD | | | 40 | ns |
| Delay Time from BCLK1 "↓" to Serial Data Output (Note 15) | tB1OD | | | 40 | ns |
| **SDIN2/5, SDOUT2/5 (master mode)** | | | | | |
| SYNC2 Duty cycle | | | 50 | | % |
| Serial Data Input Latch Setup Time | tB2IDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tB2IDH | 40 | | | ns |
| Delay Time from SYNC2 to Serial Data Outputs | tSY2OD | | | 40 | ns |
| Delay Time from BCLK2 "↓"to Serial Data Output (Note 16) | tB2OD | | | 40 | ns |
| **SDIN1 → SDOUT2/5, SDIN2/5 → SDOUT1** | | | | | |
| Delay Time in Loopback Mode (Note 17) | tIOD | | | 60 | ns |

Note 14. When the polarity of BCLK1 is inverted, delay time is from BCLK1 "↓"

Note 15. When the polarity of BCLK1 is inverted, delay time is from BCLK1 "↑".

Note 16. When the polarity of BCLK2 is inverted, delay time is from BCLK2 "↑".

Note 17. When LPDO1 bit = "0", LPDO2 bit = "0"

## ■ Timing Diagram

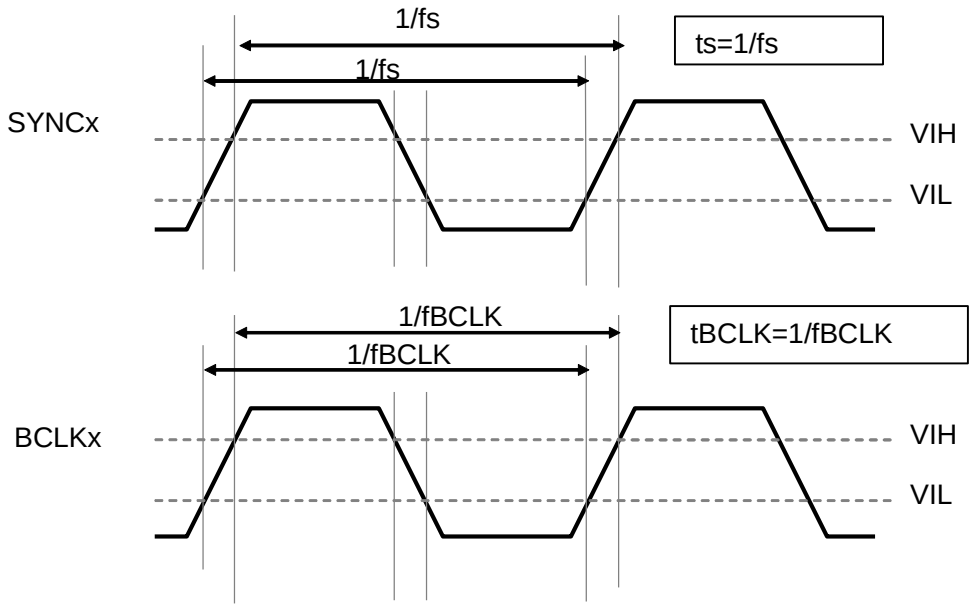



Figure 4. System Clock (x=1~5)

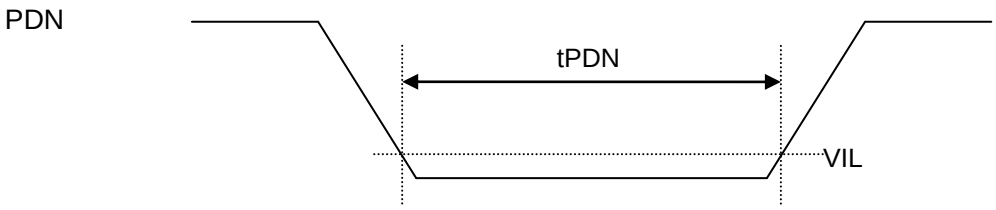



Figure 5. Power-down

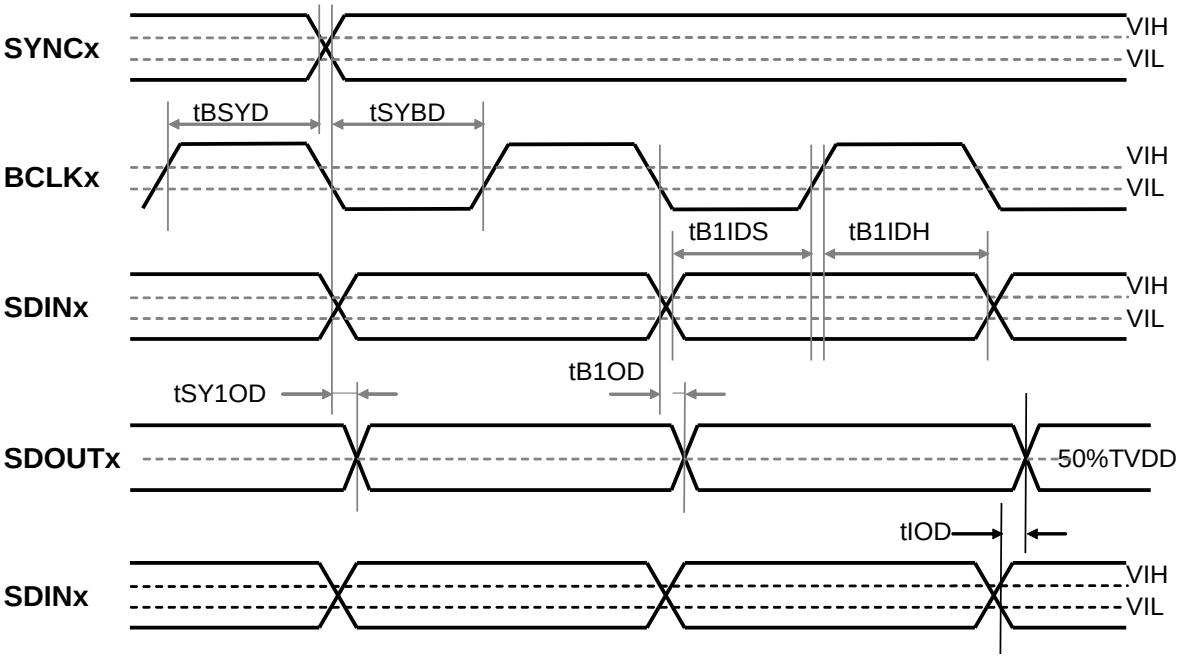



Figure 6. Serial Data Interface (x=1~5) (x=2, 5: slave mode)

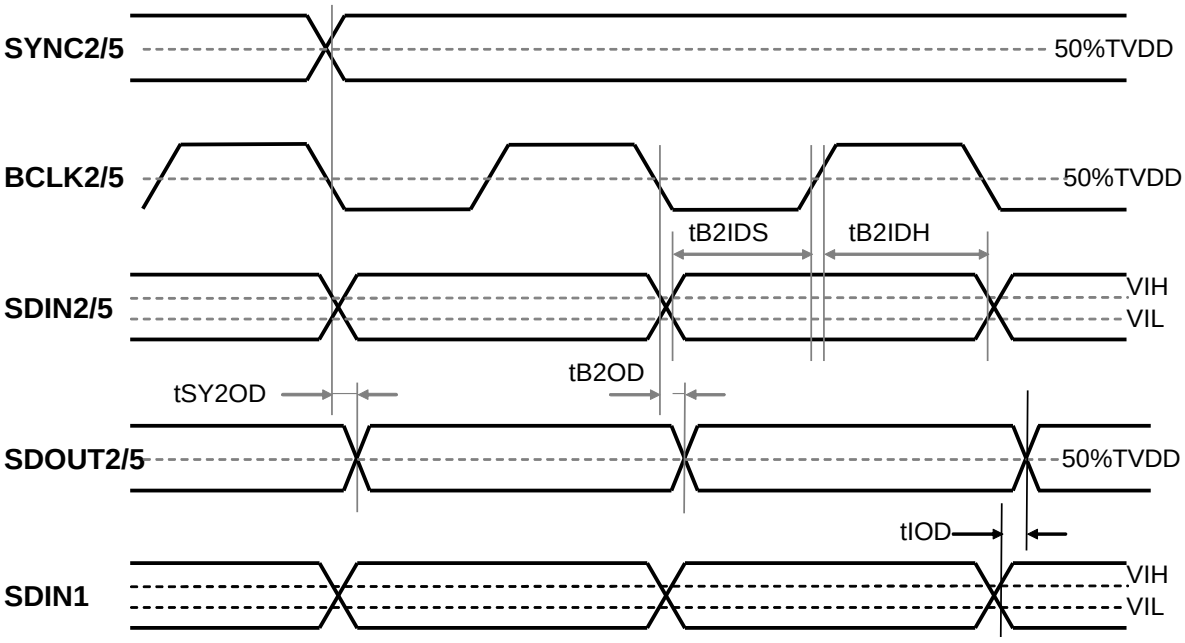



Figure 7. Serial Data Interface (SDIN2/5, SDOUT2/5 master mode)

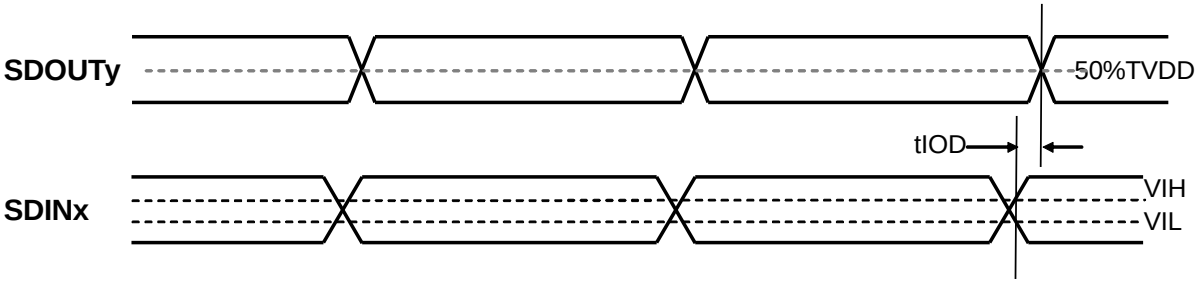



Figure 8. Serial Data Interface (x=1, y=2/5 or x=2/5, y=1: loopback mode)

## ■ µP Interface (SPI Mode)

(Ta= -40ºC ~ 85ºC, VDD=1.2V; TVDD=1.6~3.6V, VSS =0V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| **µP Interface Timing (SPI mode)** | | | | | |
| SCLK Fall Time | tSF | | | 30 | ns |
| SCLK Rise Time | tSR | | | 30 | ns |
| SCLK Frequency | fSCLK | | | 4.0 | MHz |
| SCLK Low Level Width | tSCLKL | 120 | | | ns |
| SCLK High Level Width | tSCLKH | 120 | | | ns |
| CSN High Level Width | tWRQH | 500 | | | ns |
| From CSN "↑" to PDN "↑" | tRST1 | 600 | | | ns |
| From PDN "↑" to CSN "↓" | tIRRQ | 100 | | | µs |
| From CSN "↓" to SCLK " ↓ " | tWSC | 500 | | | ns |
| From SCLK "↑" to CSN "↑" | tSCW | 800 | | | ns |
| SI Latch Setup Time | tSIS | 100 | | | ns |
| SI Latch Hold Time | tSIH | 100 | | | ns |
| **AK7719B → µP** | | | | | |
| Delay Time from SCLK "↓"to SO Output | tSOS | | | 100 | ns |
| Hold Time from SCLK "↑" to SO Output (Note 18) | tSOH | 100 | | | ns |

Note 18. Except when input the eighth bit of the command code.

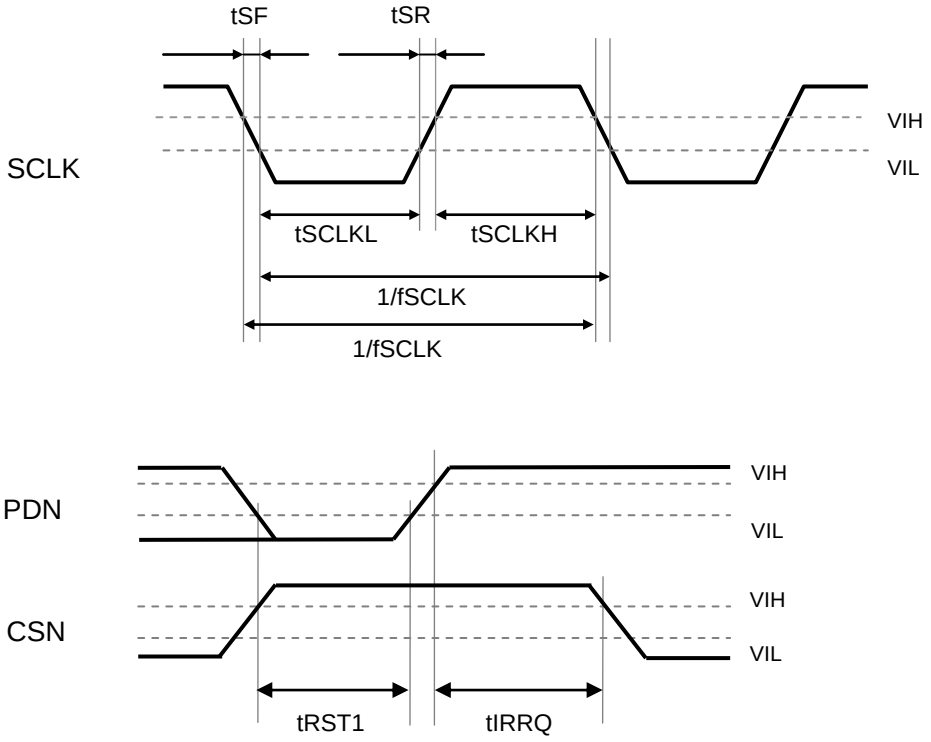



Figure 9. µP Interface 1 (SPI)

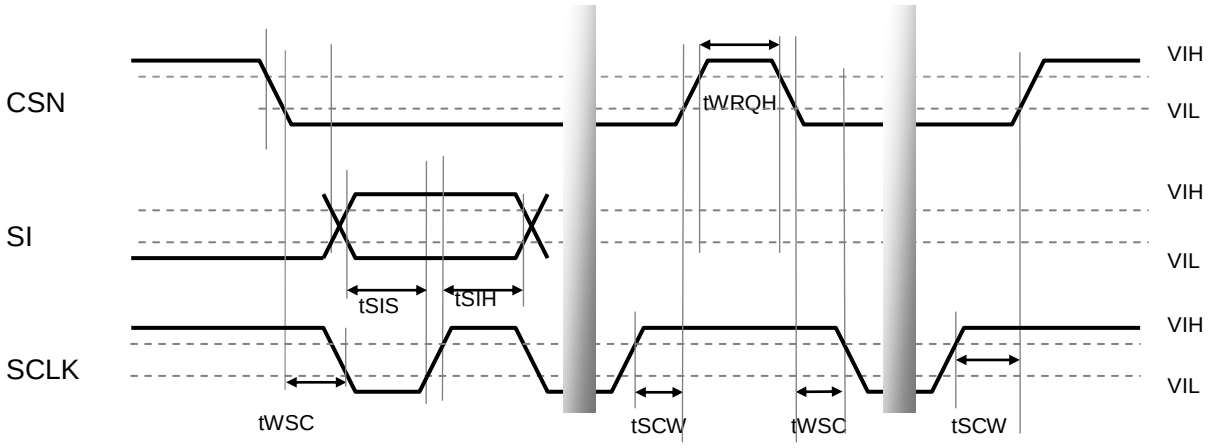



Figure 10. µP Interface 2 (SPI)

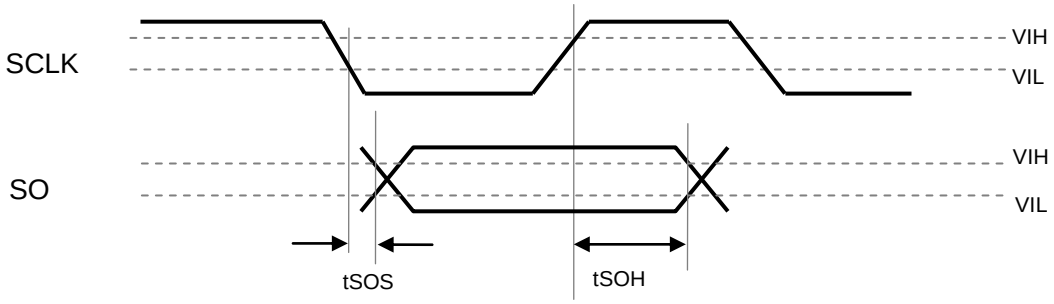



Figure 11. µP Interface 3 (SPI)

## ■ I²C Bus Interface

(Ta=-40ºC~85ºC, VDD=1.2V, VDD=1.6~3.6V, VSS =0V, CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| **I²C Timing** | | | | | |
| SCL clock frequency | fSCL | 30 | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | µs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | µs |
| Clock Low Time | tLOW | 1.3 | | | µs |
| Clock High Time | tHIGH | 0.6 | | | µs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | | µs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | | 0.9 | µs |
| SDA Setup Time from SCL Rising | tSU: DAT | 0.1 | | | µs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | µs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | µs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | µs |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | | | 400 | pF |

Note 19. I²C-bus is a trademark of NXP B.V.

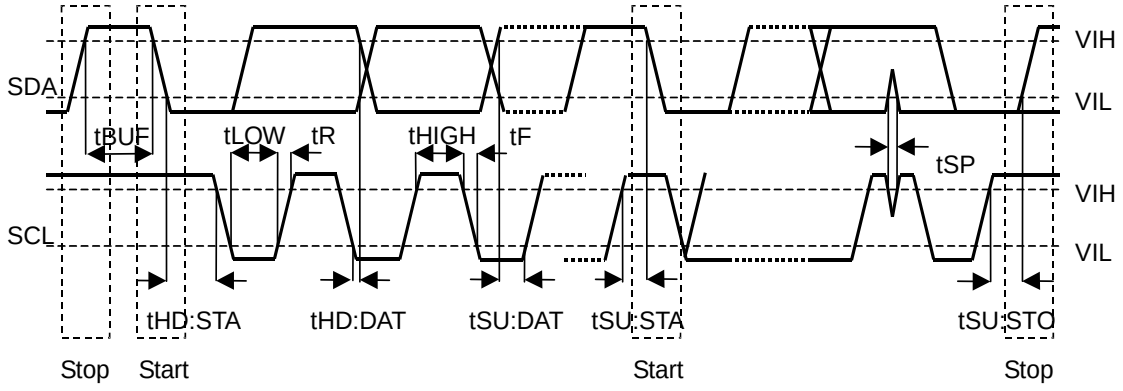
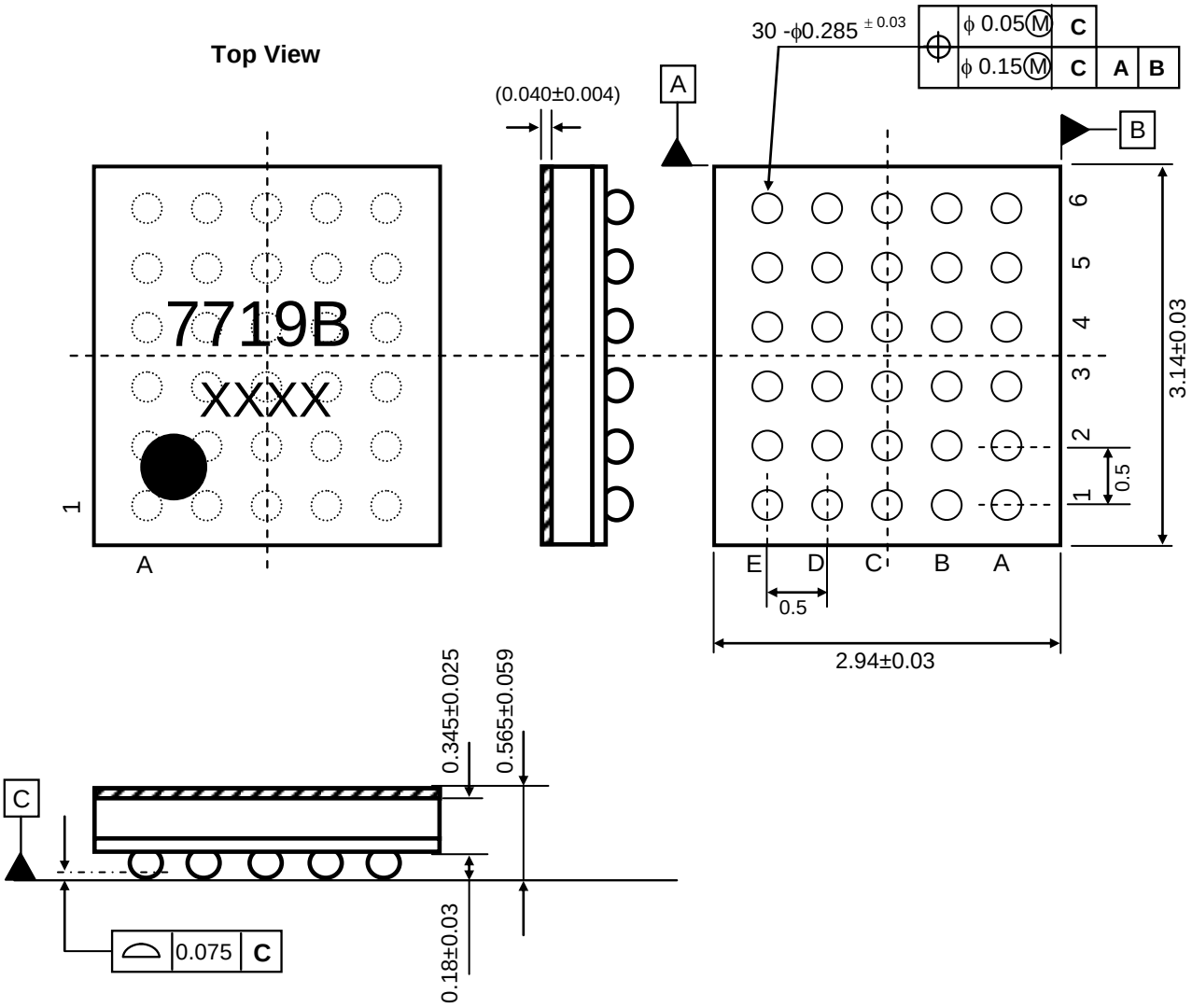



Figure 12. I²C Bus Interface

## 13. Package

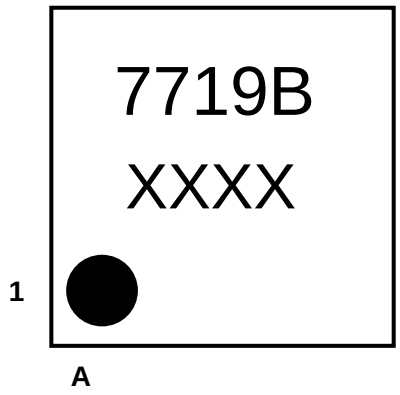
30pin CSP (Unit: mm)




### ■ Material & Lead Finish

Package: Epoxy, Halogen (Br and Cl) free
Solder ball material: SnAgCu

## 14. Marking




XXXX: Date code (4 digit)

## 15. Revision History

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 13/11/01 | 00 | First Edition | | |

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