AK7754

Audio DSP with Stereo CODEC + MIC/HP-AMP

GENERAL DESCRIPTION

The AK7754 is a highly integrated audio digital signal processor (DSP) with two Audio I/F's, Microphone and Headphone Amplifier. The audio DSP has 1536step/fs (at 48KHz sampling) parallel processing power, and AKM's original Hands-free technology provides high performance noise and echo cancelling. The 96k-bit delay memory allows surround processing, acoustic effect and parametric equalizers. As the AK7754 is a RAM based DSP, it is programmable for user requirements. The internal SRC has various sampling rate converting modes, corresponds many sampling rates without changing the DSP operating sampling frequency. The AK7754 is available in a space saving small 48pin QFN package.

FEATURES

□ **DSP Block**

- **Word length: 24bit (Coefficient RAM & Data RAM: F24 floating point)**
- **Processing Speed: 13.6 ns (1536step/fs fs=48kHz; 9216step/fs fs=8kHz)**
- **Multiplication: 20 x 16 → 36-bit Double precision arithmetic available**
- **Divider 20 / 20 → 20bit**
- **ALU: 40bit arithmetic operation (overflow margin 4bit) 24bit floating point arithmetic and logic operation**
- **Program RAM: 2048 x 36bit**
- **Coefficient RAM: 2048 x 16bit (F24 floating point)**
- **Data RAM: 512 x 24-bit (F24 floating point)**
- **Offset Register: 32 x 12bit**
- **Delay RAM1: 3072 x 24bit**
- **Delay RAM2: 2048 x 12bit**
- **Sampling rate: fs= 8.0k ~ 48kHz**
- **Master/Slave Operation**
- **Master Clock: 1536fs (generated from 32fs, 48fs, 64fs, 128fs, 256fs, 384fs by internal PLL)**

□ **Two Digital Interfaces (I/F 1, I/F 2)**

- **Digital Signal Input Port (4ch) MSB justified 24bit/LSB justified 24/20/16bit and I^2S**
- **Digital Signal Input Port (6ch) MSB justified 24bit/ LSB justified 20/16bit and I^2S**
- **Short / Long Frame**
- **-24 bit linear, 8 bit A-law, 8 bit μ-law**

□ **Stereo 24bit ADC Block**

- **Sampling rate: 8 ~ 48kHz**
- **ADC Characteristics S/(N+D): 82dB ,DR, S/N: 89dB**
- **Three Analog Input Selectors (Differential, Single-ended Inputs)**
- **Channel Independent MIC, Analog Line Gain Amp (0dB, 9dB~27dB, 3dBstep)**
- **Channel Independent Digital Volume (24dB ~ -103dB, 0.5dB Step, Mute)**
- **Integrated DC offset canceling High Pass Filter**

□ **Digital Microphone I/F**

□ **Stereo 24bit DAC**
- **Sampling rate: 8 ~ 48kHz**
- **Digital Volume (12dB~-115dB, 0.5dB Step, Mute)**
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**

□ **Line Outputs**
- **Single-ended or Differential Outputs**
- **S/(N+D): 91dB ,DR, S/N: 96dB**
- **Stereo Analog Volume (+0 ~ -28dB, 2.0dB Step, Mute)**

□ **Stereo Headphone Amplifier with a Volume Control**
- **Rated Output Power: 27mW/ch @16Ω**
- **S/(N+D): 70dB , S/N: 89dB**
- **Stereo Analog Volume (+0 ~ -50dB,1.0/2.0/4.0dB Step, Mute)**
- **Click Noise Free at Power ON/OFF**

□ **SRC Block**
- **2ch x 1 system**
- **Input Sampling Frequency: 8kHz ~ 96kHz**
- **Output Sampling Frequency: 8kHz ~ 48kHz**

□ **Analog Bypass Mode**
- **Bypass Amplifier (0dB~-21dB, 3dB step)**

□ **Output Mixer**

□ **μP Interface: I^2C Bus (400KHz Fast-Mode)**

□ **Power Supply**

Analog	**AVDD: 3.0V ~ 3.6V (typ.3.3V)**
Digital1	**DVDD: 3.0V ~ 3.6V (typ.3.3V)**
Digital2	**DVDD18: 1.7V ~ 1.9V (typ.1.8V)**
HP-Amp	**HVDD: 3.0V ~ 3.6V (typ.3.3V)**

□ **Operating temperature range: -20°C ~ 85°C**

□ **Package: 48pin QFN (0.5mm pitch)**

■ Block Diagram

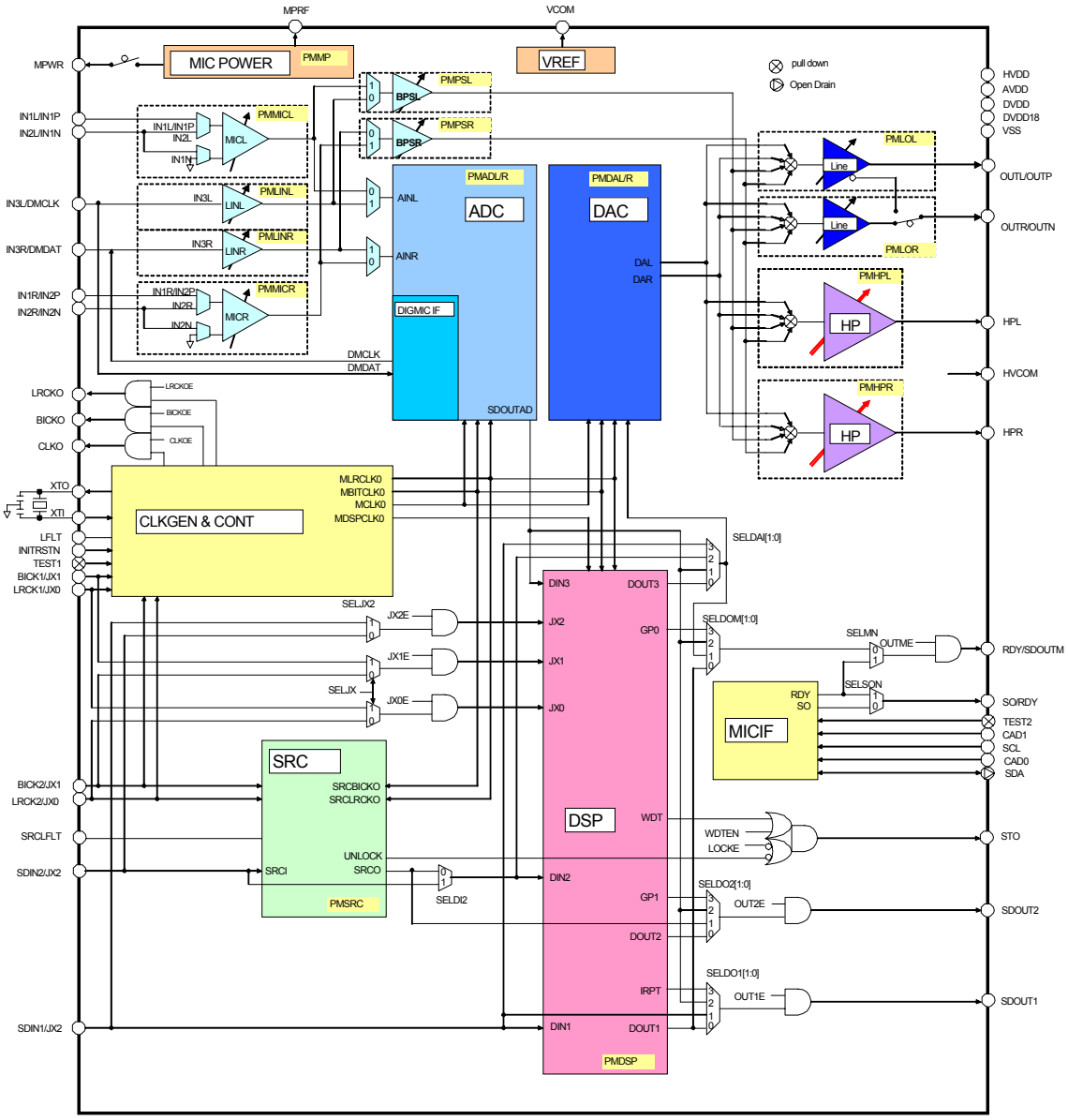
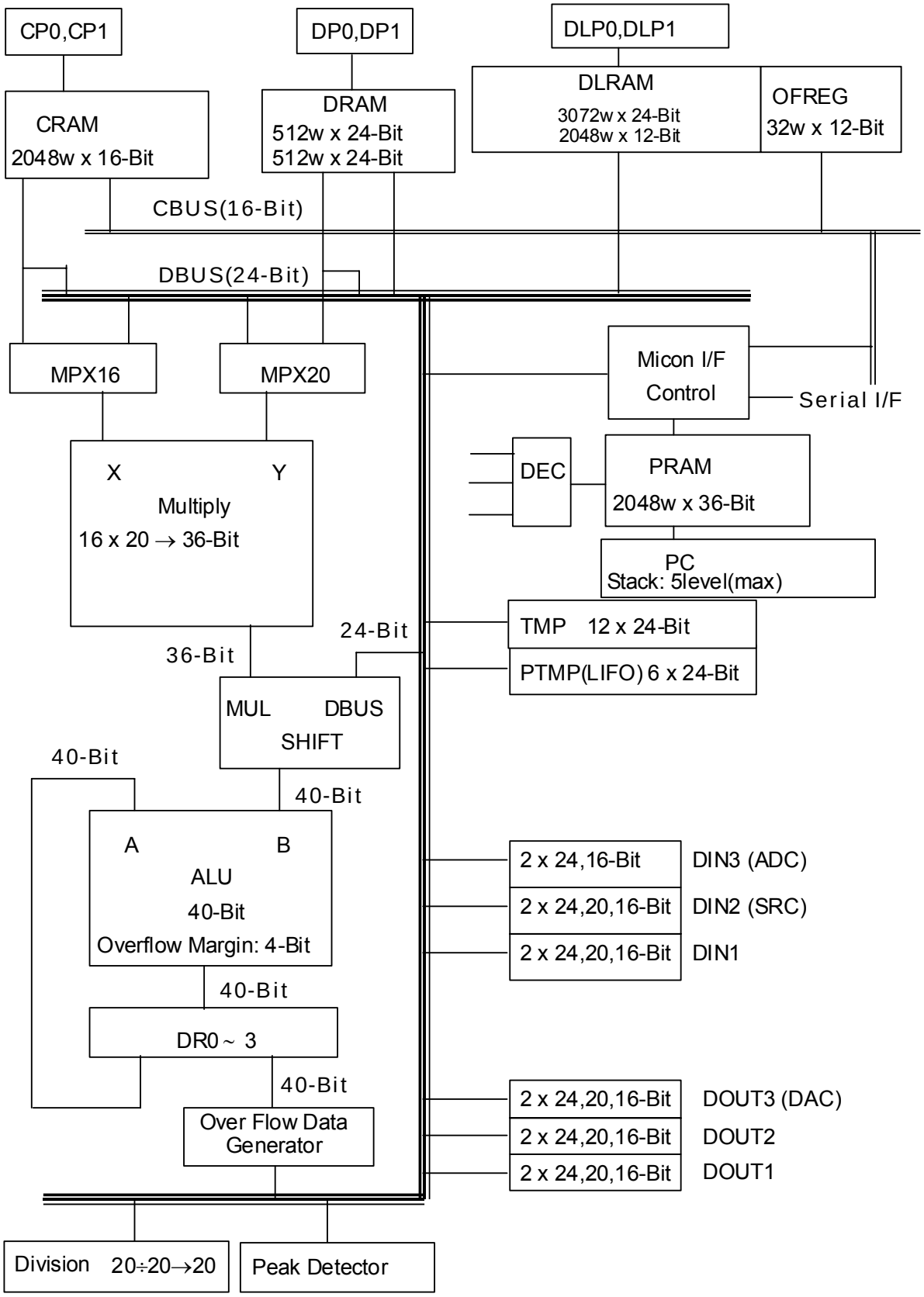


Figure 1. Block Diagram

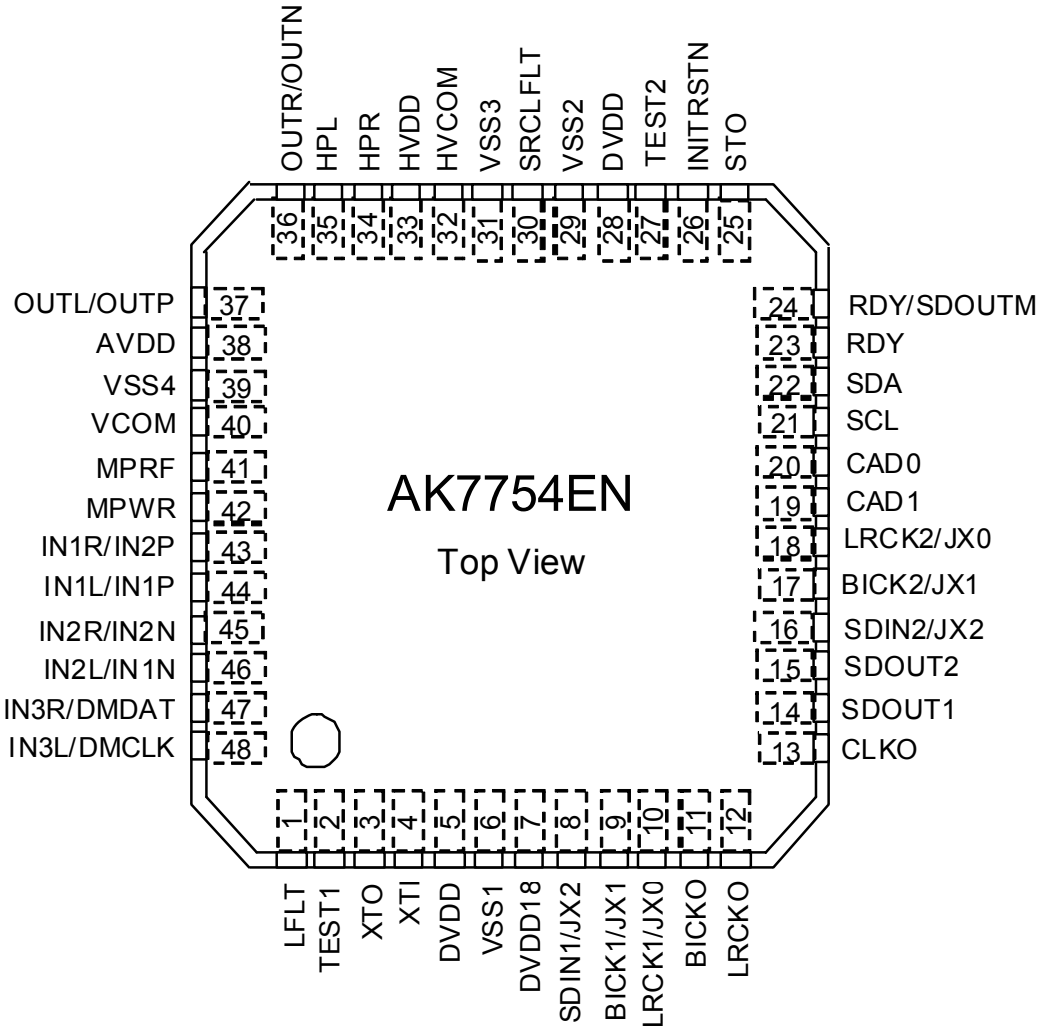
■ **DSP Block Diagram**



■ Ordering Guide

AK7754EN	-20 ~ +85°C	48pin QFN (0.5mm pitch)
AKD7754	Evaluation Board for AK7754	

■ Pin Layout (TBD)



PIN FUNCTION

No.	Name	I/O	Function	Classification
1	LFLT	O	PLL RC component connect pin Connect a capacitor and resistor between this pin and VSS4. This pin outputs “L” during initial reset.	Analog Output
2	TEST1	I	Test1 Pin (Internal pull-down) This pin must be connected to VSS1.	Test
3	XTO	O	Crystal oscillator output pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open. During initial reset, the output of this pin is Hi-Z.	System Clcok
4	XTI	I	Crystal oscillator input pin/ Master Clock input Connect a crystal oscillator between this pin and the XTO pin, or input an external clock to the XTI pin. When CKM[2:0] bits= 0h, 1h, 2h, input “L” to this pin.	
5	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
6	VSS1	-	Ground Pin 0V	
7	DVDD18	-	Digital Power Supply Pin 1.7V~1.9V	
8	JX2	I	Conditional Jump Pin2 (JX2E bit = “1”)	Conditional Input
	SDIN1	I	Serial Data Input Pin1	Data I/F
9	JX1	I	Conditional Jump Pin1 (JX2E bit = “1”)	Conditional Input
	BICK1	I	Serial Bit Clock Input Pin1	Data I/F
10	JX0		Conditional Jump Pin0 (JX2E bit = “1”)	Conditional Input
	LRCK1	I	LR Channel Select Clock Pin1	Data I/F
11	BICKO	O	Serial Bit Clock Output Pin (BICKOE bit = “1”) Outputs “L” during initial reset in master mode.	System Clock Output
12	LRCKO	O	LR Channel Select Clock Pin (LRCKOE bit = “1”) Outputs “L” during initial reset in master mode.	System Clock Output
13	CLKO	O	Clock Output Pin (CLKOE bit = “1”) Outputs “L” during initial reset in master mode.	System
14	SDOUT1	O	Serial Data Output Pin1 Outputs “L” during initial reset in master mode.	Data I/F
15	SDOUT2	O	Serial Data Output Pin2 Outputs “L” during initial reset in master mode.	Data I/F
16	JX2	I	Conditional Jump Pin2 (JX2E bit = “1”)	Conditional Input
	SDIN2	I	Serial Data Input Pin2	Data I/F
17	JX1	I	Conditional Jump Pin1 (JX2E bit = “1”)	Conditional Input
	BICK2	I	Serial Bit Clock Input Pin2 (for SRC)	Data I/F

No.	Name	I/O	Function	Classification
18	JX0	I	Conditional Jump Pin0 (JX0E bit = "1") A conditional jump pin (JX0) is available by setting control register (JX0E) to "1" when SCKSEK bit = "1".	Conditional Input
	LRCK2	I	LR Channel Select Clock Pin2 (for SRC)	Data I/F
19	CAD1	I	I^2C Bus Address Pin1	I2C
20	CAD0	I	I^2C Bus Address Pin0	
21	SCL	I	I^2C Bus Interface	
22	SDA	I/O	I^2C Bus Clock Outputs "Hi-z" during initial reset.	
23	RDY	O	Data Write Ready Output Pin for Microprocessor Interface	Microprocessor I/F
24	RDY	O	Data Write Ready Output Pin for Microprocessor Interface (SELM bit= "0")	Microprocessor I/F
	SDOUTM	O	Serial Data Monitering Selector Output Pin (SELM bit= "0") Outputs "L" during initial reset.	
25	STO	O	Status Output Pin Outputs "H" during initial reset.	Status
26	INITRSTN	I	Initial Reset Pin Use to initialize the AK7754. This pin must be "L" when power up the AK7754.	Reset
27	TEST2	I	Test2 Pin This pin must be connected to DVDD.	Test
28	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
29	VSS2	-	Ground Pin 0V	Digital Power Supply
30	SRCLFLT	O	SRC, PLL RC component connect pin Connect a 1µF capacitor between this pin and VSS2. This pin outputs "L" during initial reset.	Analog Output
31	VSS3	-	Ground Pin 0V	Analog Power Supply
32	HVCOM	O	Headphone Common Voltage Output Pin Connect a of 1µF cap to VSS3. Do not use for an outside circuits. Outputs "L" during initial reset.	Headphone
33	HVDD	-	Headphone Power Supply Pin 3.0V~3.6V	Analog Power Supply
34	HPR	O	Headphone Rch Output Pin Outputs "L" during initial reset	Analog Output
35	HPL	O	Headphone Lch Output Pin Outputs "L" during initial reset	Analog Output
36	OUTR	O	DAC Rch Output Pin (LODIF bit= "0") Outputs "L" during initial reset	Analog Output
	OUTN	O	Inverted Line Output Pin (LODIF bit= "1") Outputs "L" during initial reset	
37	OUTL	O	DAC Lch Output Pin (LODIF bit= "0") Outputs "L" during initial reset	Analog Output
	OUTP	O	DAC Non-inverted differential Analog Output Pin (LODIF bit= "1") Outputs "L" during initial reset	
38	AVDD	-	Analog Power Supply Pin 3.0V~3.6V	Analog Power Supply

No.	Name	I/O	Function	Classification
39	VSS4	-	Ground Pin 0V	Analog Power Supply
40	VCOM	O	Analog common voltage Connect 0.1μF and 2.2μF capacitors in parallel to VSS4. Never to use for an external circuit. Outputs "L" during initial reset	Analog Output
41	MPRF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1uF capacitor between this pin and VSS4.	Analog Output
42	MPWR	O	Power Supply Pin for Microphone Outputs "Hi-Z" during initial reset	Analog Output
43	IN1R	I	Rch Single-end Input Pin1 (MDIFR bit = "0")	Analog Input
	IN2P	I	MIC Differential Non-Inverted Input Pin2 (MDIFR bit = "1")	
44	IN1L	I	Lch Single-end Input Pin1 (MDIFL bit = "0")	Analog Input
	IN1P	I	MIC Differential Non-inverted Input Pin1 (MDIFL bit = "1")	
45	IN2R	I	Rch Single-end Input Pin2 (MDIFR bit = "0")	Analog Input
	IN2N	I	MIC Differential Inverted Input Pin2 (MDIFR bit = "1")	
46	IN2L	I	Lch Single-end Input Pin2 (MDIFL bit = "0")	Analog Input
	IN1N	I	MIC Differential Inverted Input Pin1 (MDIFL bit = "1")	
47	IN3R	I	Rch Single-end Input Pin3 (DMIC bit = "0")	Analog Input
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")	Digital Microphone
48	IN3L	I	Lch Single-end Input Pin3 (DMIC bit = "0")	Analog Input
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")	Digital Microphone

Note: Do not leave digital input pins open.

■ Handling of Unused Pin

The following table illustrates recommended states for open pins:

Classification	Pin Name	Setting
Analog	IN1L/IN1P,IN1R/IN2P,IN2L/IN1N,IN2R/IN2N,IN3L,IN3R	Leave Open
Digital	CLKO, BICKO, LRCKO, SDOUT1-2, SDOUTM, STO, SOUTM/RDY,XTO	Leave Open
	SDIN1, SDIN2, BICK1, BICK2, LRCK1, LRCK2, XTI	Connect to VSS1

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4= 0V: Note 1)

Parameter	Symbol	min	max	Unit
Power Supply Voltage (AVDD=DVDD)				
Analog	AVDD	-0.3	4.3	V
Analog	HVDD	-0.3	4.3	V
Digital	DVDD	-0.3	4.3	V
Digital	DVDD18	-0.3	2.5	V
Difference(VSS1~4)	ΔGND	-0.3	0.3	V
Input Current (except for power supply pin)	IIN	–	±10	mA
Analog Input Voltage (Note 2)	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage (Note 3)	VIND1	-0.3	(DVDD+0.3) or 4.3	V
Operating Ambient Temperature	Ta	-20	85	ºC
Storage Temperature	Tstg	-65	150	ºC

Note 1. All indicated voltages are with respect to ground.
Note 2. VSS1-5 must be connected to the same ground plane.
Note 3. The maximum digital input voltage is smaller value between (DVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V: Note 1)

Parameter	Symbol	min	typ	max	Unit
Power Supply Voltage					
Analog	AVDD	3.0	3.3	3.6	V
Analog	HVDD	3.0	3.3	3.6	V
Digital	DVDD	3.0	3.3	3.6	V
Digital	DVDD18	1.7	1.8	1.9	V
HVDD-AVDD	ΔVDD1	-0.3	0	+0.3	V
HVDD-DVDD	ΔVDD2	-0.3	0	+0.3	V
AVDD-DVDD	ΔVDD3	-0.3	0	+0.3	V

Note 4. The power supply sequence for AVDD, HVDD, DVDD and DVDD18 is not critical but all power supplies must be On before start operating the AK7754.
Note 5. Do not turn off the power supply of the AK7754 with the power supply of the surrounding device turned on. DVDD must not exceed the pull-up of SDA and SCL of I2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

ANALOG CHARACTERISTICS (CODEC)

■ ADC Characteristics

(Ta=25ºC; AVDD=DVDD=HVDD=3.3V, DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V; BICK1=64fs; Signal Frequency 1kHz; Measurement frequency =20Hz~20kHz, fs=48kHz, PMSRC=PMHPL=PMHPR bits="0", CKM mode 6 (CKM[2:0]=6h) Unless otherwise specified.)

Parameter				min	typ	max	Units
MIC/LINEIN Amplifier: IN1L,IN1R,IN2L,IN2R,IN3L,IN3R pins							
Input Resistance							
				22.5	30	37.5	kΩ
Gain							
	Max (MGNL/R2-0, LINL/R2-0 bits = "0H")			-	0	-	dB
	Min (MGNL/R2-0, LINL/R2-0 bits = "7H")			-	+27	-	dB
Bypass Amplifier: IN1L,IN1R,IN2L,IN2R,IN3L,IN3R pins (MGNL/R2-0 = 0h, LINL/R2-0 = 0h)							
Gain							
	Max (BPGL/R2-0 bit = "0H")			-	0	-	dB
	Min (BPGL/R2-0 bit = "7H")			-	-21	-	dB
MIC Power Supply: MPWR pin							
Output Voltage (Note 6)				2.18	2.3	2.4	V
Output Current				-	-	4	mA
Stereo ADC	Resolution					24	Bits
	Dynamic Characteristics IN1L/IN1R, IN2L/IN2R, IN3L/IN3R pins→ stereo ADC→ SDOUT1/2/M (VOLADL/R=30h(0dB)						
	S/(N+D) (-1dBFS)		(Note 12)	70	77		dB
			(Note 13)	74	82		dB
	Dynamic Range (A-weight)		(Note 12)	74	82		dB
			(Note 13)	81	89		dB
	S/N (A-weight)		(Note 12)	74	82		dB
			(Note 13)	81	89		dB
	Inter-Channel Isolation (fin=1kHz) (Note 7)		(Note 13)	90	105		dB
	DC accuracy						
	Channel Gain Mismatch				0.0	0.3	dB
	Analog Input						
	Input Voltage	Differential (Note 8, Note 10)	(Note 12)		±0.098		Vpp
			(Note 13)	±1.0	±1.1	±1.2	
	Input Voltage	Single-ended (Note 9, Note 11)	(Note 12)		0.196		Vpp
			(Note 13)	2.0	2.2	2.4	

Note 6. The output voltage is proportional to AVDD. Vout=0.76 x AVDD (typ.)
Note 7. Inter-channel isolation between IN1-3L and IN1-3R pins when –1dB FS signal is input.
Note 8. The input voltage is proportional to AVDD. Vin=±0.030 x AVDD (typ.)@MGNL2-0=MGNR2-0 bits = "5h"(+21dB), Vin=±0.33 x AVDD (typ.) @MGNL2-0=MGNR2-0 bits = "0h"(+0dB)
Note 9. The input voltage is proportional to AVDD. Vin=0.059 x AVDD (typ.)@MGNL2-0=MGNR2-0 bits = "5h"(+21dB), Vin=0.67 x AVDD (typ.) @MGNL2-0=MGNR2-0 bits = "0h"(+0dB)
Note 10. IN1P, IN1N, IN2P and IN2N pins
Note 11. IN1L, IN1R, IN2L, IN2R, IN3L and IN3R pins
Note 12. MGNL2-0=MGNR2-0 bits = "5h" (+21dB)
Note 13. MGNL2-0=MGNR2-0 bits = "0h" (+0dB)

■ DAC Characteristics

(Ta=25ºC; AVDD=DVDD=HVDD=3.3V, DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V; BICK1=64fs; Signal frequency 1kHz; Measurement frequency=20Hz~20kHz, fs=48kHz, PMSRC=PMHPL=PMHPR bits = "0", CKM mode 6 (CKM[2:0]=6h, Unless otherwise specified.)

	Parameter		min	typ	max	Unit
Stereo DAC	Resolution				24	Bits
	Dynamic Characteristics; Stereo DAC→OUTL/R pins VOLDAL/R=18h(0dB) LODIF="0"					
	S/(N+D) (0dBFS)		80	91		dB
	Dynamic Range (A-weight)		88	96		dB
	S/N (A-weight)		88	96		dB
	Inter-Channel Isolation (fin=1kHz) (Note 14)		90	110		dB
	DC accuracy					
	Channel Gain Mismatch			0.0	0.5	dB
	Analog Volume Characteristics					
	Gain Amount	Min		0.0		dB
		Max		28.0		dB
	Step width			2.0		dB
	Analog Output					
	Output Voltage (Note 15)	Single-End	2.06	2.17	2.28	Vpp
		Differential	±2.06	±2.17	±2.28	Vpp
	Load Resistance		10			kΩ
	Load Capacitance				30	pF

Note 14. Inter-channel isolation between Lch and Rch of the DAC.
Note 15. Full scale output voltage. The output voltage is proportional to AVDD. Vout=0.67 x AVDD (typ.)

ANALOG CHARACTERISTICS (HP-Amp)

(Ta=25ºC; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V; Signal frequency 1kHz; Measurement frequency=20Hz~20kHz@48kHz; PMSRC bit="0"), R_L =16Ω; Circuit External Capacitance: C1=C2=OPEN. CKM mode6, Unless otherwise specified.)

Parameter		min	typ	max	Units
Analog Volume Characteristics					
Gain	Max (HPGL,HPGR[4:0] bits= "1FH")	-	+0	-	dB
	Min (HPGL,HPGR[4:0] bits= "01H")	-	-50	-	dB
Step width	+0dB ~ -16dB	0.1	1	-	dB
	-16dB ~ -38dB	0.1	2	-	dB
	-38dB ~ -50dB	-	4	-	dB
Headphone-Amp Characteristics: DAC → HPL/HPR pins, RL=16Ω (Note 16)					
Output Voltage		1.68	1.87	2.06	Vpp
S/(N+D)	(-3dBFS)	60	70	-	dB
S/N	(A-weighted)	83	89	-	dB
Inter channel Isolation		60	75	-	dB
Inter channel Gain Mismatch		-	0.0	1.0	dB
Load Resistance	(RL, Figure 2)	16	-	-	Ω
Load Capacitance	(C1, Figure 2)	-	-	30	pF
Load Capacitance	(C2, Figure 2)	-	-	300	pF

Note 16. Because of an asynchronous circuit operation, the characteristic may deteriorate when SRC is in operation.

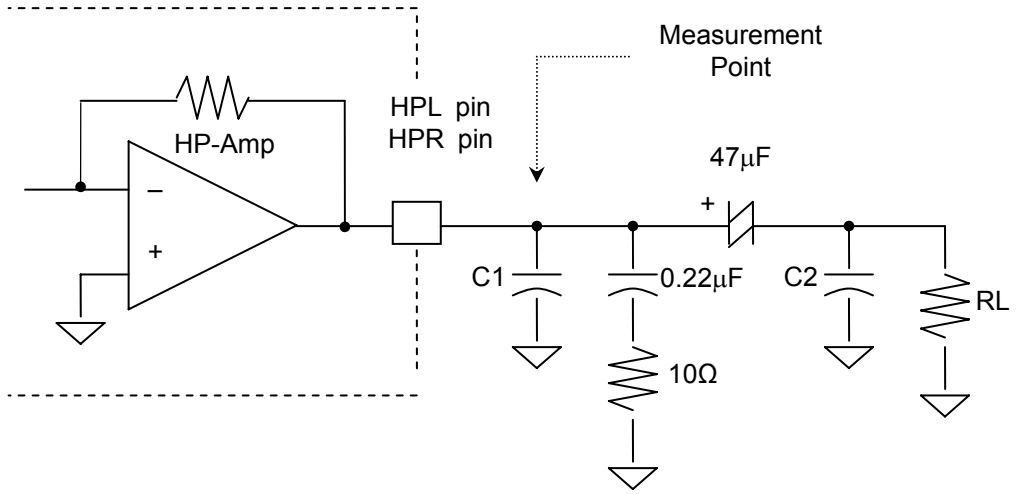


Figure 2. Headphone Amp Output Circuit

SRC CHARACTERISTICS

(Ta=25°C; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V; Signal frequency 1kHz; Measurement frequency= 20Hz~FSO/2)

Parameter	Symbol	min	typ	max	Units
Resolution				24	Bits
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO	8		48	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=44.1kHz/48kHz			-111		dB
FSO/FSI=44.1kHz/96kHz			-104		dB
FSO/FSI=48kHz/44.1kHz			-111		dB
FSO/FSI=48kHz/96kHz			-111		dB
FSO/FSI=48kHz/8kHz			-111	-103	dB
FSO/FSI=16kHz/48kHz			-111		dB
FSO/FSI=16kHz/44.1kHz			-104		dB
FSO/FSI=8kHz/48kHz			-111		dB
FSO/FSI=8kHz/44.1kHz			-78		dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=44.1kHz/48kHz			112		dB
FSO/FSI=44.1kHz/96kHz			112		dB
FSO/FSI=48kHz/44.1kHz			112		dB
FSO/FSI=48kHz/96kHz			112		dB
FSO/FSI=48kHz/8kHz		108	112		dB
FSO/FSI=16kHz/48kHz			112		dB
FSO/FSI=16kHz/44.1kHz			112		dB
FSO/FSI=8kHz/48kHz			112		dB
FSO/FSI=8kHz/44.1kHz			112		dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)					
FSO/FSI=44.1kHz/48kHz			115		dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

DC CHARACTERISTICS

(Ta=-20ºC~85ºC; AVDD= HVDD= 3.0V~3.6V; DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V)

Parameter	Symbol	min	typ	max	Unit
High level input voltage (Note 17)	VIH	80%DVDD			V
Low level input voltage (Note 17)	VIL			20%DVDD	V
SCL, SDA High level input voltage	VIH	70%DVDD			V
SCL, SDA Low level input voltage	VIL			30%DVDD	V
DMDAT High level input voltage	VIH	65%DVDD			V
DMDAT Low level input voltage	VIL			35%DVDD	V
High level output voltage: Iout=-100µA (Note 18)	VOH	DVDD-0.4			V
Low level output voltage: Iout=100µA (Note 18)	VOL			0.4	V
SDA Low level output voltage Iout=3mA	VOL			0.4	V
Input leak current (Note 19)	Iin			±10	µA
Input leak current TEST1/2 pin (Note 20)	Iid		22		µA
Input leak current XTI pin	Iix		26		µA

Note 17. Except for the SCL, SDA pin.
Note 18. Except for the SDA pin. The DMCLK pin is included.
Note 19. Except for the TEST2 pin, TEST1 pin and XTI pin.
Note 20. The TEST1 pin has an internal pull-down device, nominally 150kΩ.

POWER CONSUMPTION

(Ta=-20ºC ~ 85ºC; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=VSS4=0V, fin=1 KHz, 24 bit, fs=48kHz, BICK1=64fs (CKM mode=4, BITFS mode=0), CODEC (Full-duplex mode, no output loads) and DSP running with programmed that connects DSP DIN3 with DOUT1 and DIN1 with DOUT3.

Parameter			min	typ	max	Units
Power Supplies: (Note 21)						
Power-Up (IRSTN pin = "H") CODEC + DSP + LineOut + HP						
All Circuit Power-up						
	AVDD+DVDD	AVDD=DVDD=HVDD=3.3V, DVDD18=1.8V		21	-	mA
	HVDD			4.8		mA
	DVDD18			29	-	mA
	Power Consumption			137		mW
	AVDD+DVDD	AVDD=DVDD=HVDD=3.6V, DVDD18=1.9V		22	38	mA
	HVDD			5.0	7.5	mA
	DVDD18			31	70	mA
Reset (IRSTN pin = "L"), Reset condition (Note 22)						
	AVDD+DVDD+HVDD		-	1	10	µA
	DVDD18			3	200	µA

Note 21. The actual power consumption of DVDD18 depends on the master clock frequency and the step size of the DSP program. (BITFS bit = "2h" and DSPS bit = "0")
Note 22. All digital input pins must be fixed to Logic High /Low.

DIGITAL FILTER CHARACTERISTICS

■ ADC Block

1. fs=8kHz

(Ta=-20ºC~85ºC, AVDD= HVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1=VSS2=VSS3=VSS4=0V; fs=8 kHz; Note 23)

Parameter	Symbol	min	typ	max	Units
Passband (±0.1dB) (Note 24)	PB	0		3.15	kHz
(-1.0dB)			3.63		kHz
(-3.0dB)			3.83		kHz
Stopband	SB	4.66			kHz
Passband Ripple (Note 24)	PR			±0.1	dB
Stopband Attenuation (Note 25, Note 26)	SA	68			dB
Group Delay Distortion	ΔGD			0	μs
Group Deley (Ts=1/fs)	GD		16		Ts

Note 23. Frequencies of each amplitude characteristics are in proportion to fs (sampling rate). The characteristic of the high pass filter is not included.
Note 24. The passband is from DC to 3.15kHz when fs=8kHz.
Note 25. The stopband is 4.66kHz to 507.34kHz when fs=8kHz.
Note 26. When fs = 8kHz, the analog modulator samples the input signal at 512kHz.

2. fs=48kHz

(Ta=-20ºC~85ºC, AVDD=HVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1=VSS2=VSS3=VSS4=0V; fs=48 kHz; Note 27)

Parameter	Symbol	min	typ	max	Units
Passband (±0.1dB) (Note 28)	PB	0		18.9	kHz
(-0.2dB)			20.0		kHz
(-3.0dB)			23.0		kHz
Stopband	SB	28.0			kHz
Passband Ripple (Note 28)	PR			±0.04	dB
Stopband Attenuation (Note 29,Note 30)	SA	68			dB
Group Delay Distortion	ΔGD			0	μs
Group Delay (Ts=1/fs)	GD		16		Ts

Note 27. Frequencies of each amplitude characteristics are in proportion to fs (sampling rate).
Note 28. The passband is from DC to 18.9kHz when fs=48kHz.
Note 29. The stopband is 28kHz to 3.044MHz when fs=48kHz.
Note 30. When fs = 48kHz, the analog modulator samples the input signal at 3.07MHz.

■ DAC Block

1. fs=8kHz

(Ta=-20ºC ~ 85ºC, AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V; VSS1=VSS2 = VSS3=VSS4=0V; fs=48kHz; DEM1-0 bits= "0", fs=8kHz; Note 27)

Parameter	Symbol	min	typ	max	Units
Passband (±0.05dB) (Note 31)	PB	0		3.62	kHz
(-6.0dB)			4		kHz
Stopband (Note 31)	SB	4.37			kHz
Passband Ripple	PR			±0.01	dB
Stopband Attenuation (Ts=1/fs) (Note 32)	SA	64			dB
Group Delay	GD		24		Ts
Digital Filter + Analog Filter					
Amplitude characteristic 20Hz~3.5kHz			±0.5		dB

2. fs=48kHz

(Ta=-20ºC ~ 85ºC, AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V; VSS1=VSS2=VSS3=VSS4=0V; fs=48kHz; DEM1-0 bits= "0", fs=48kHz; Note 27)

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (±0.05dB) (Note 31)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stopband (Note 31)	SB	26.2			kHz
Passband Ripple	PR			±0.01	dB
Stopband Attenuation	SA	64			dB
Group Delay (Ts=1/fs) (Note 32)	GD	-	24		Ts
Digital Filter + Analog Filter					
Amplitude characteristic 0~20.0kHz			±0.5		dB

Note 31. Pass band and Stop band parameter is related to sampling frequency(fs). PB=0.4535fs (at-0.05dB), SB=0.5465fs.

Note 32. The digital filter's delay is calculated as the time from setting 24-bit data into the input register until an analog signal is output.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta= -20ºC ~ 85ºC, AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=VSS3=VSS4=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
XTI CKM[2:0]bits=4h-7h					
a) with a Crystal Oscillator:					
CKM[2:0]bits=6h	fXTI		11.2896 12.288		MHz
CKM[2:0]bits=7h	fXTI		16.9344 18.432		MHz
b) with an External Clock					
Duty Cycle		40	50	60	%
CKM[2:0]bits=4h,6h	fXTI	11.0	11.2896 12.288	 12.4	MHz
CKM[2:0]bits=5h,7h	fXTI	16.5	16.9344 18.432	 18.6	MHz
LRCK1 Frequency @SCKSEL bit=0 (Note 33)	fs	8		48	kHz
BICK1 Frequency @SCKSEL bit=0 (Note 34)					
High Level Width Low Level Width	tBCLKH tBCLKL	64 64			ns ns
Frequency	fBCLK	0.23	3.072	3.1	MHz
LRCK2 Frequency @SCKSEL bit=1 (Note 35)	fs	8		48	KHz
BICK2 Frequency @SCKSEL bit=1 (Note 36)					
High Level Width Low Level Width	tBCLKH tBCLKL	64 64			ns ns
Frequency	fBCLK	0.23	3.072	3.1	MHz

Note 33. Input LRCK1 frequency is the same as sampling rate (fs).
Note 34. When BICLK1 is used as a master clock reference clock, it should be synchronized with LRCK1.
Note 35. Input LRCK2 frequency is the same as sampling rate (fs).
Note 36. When BICLK2 is used as a master clock reference clock, it should be synchronized with LRCK2.

■ SRC Input Clock

(Ta= -20ºC ~ 85ºC, AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=VSS3=VSS4=0V, @SCKSEL bit =“0”)

Parameter	Symbol	min	typ	max	Units
LRCLKI2 Frequency	fs	8		96	kHz
BITCLKI2 Frequency					
Frequency	fBCLK	0.23	3.072	6.2	MHz
High Level Width Low Level Width	tBCLKH tBCLKL	32 32			ns ns

■ Reset

(Ta= -20 ºC ~ 85 ºC, AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1=VSS2=VSS3=VSS4=0V)

Parameter	Symbol	min	typ	max	Units
INITRSTN (Note 37)	tRST	600			ns

Note 37. The INITRSTN pin should be "L" when power up the AK7754.

■ Audio Interface

1) SDIN1/2, SDOUT1/2/M

(Ta= -20ºC ~ 85ºC, AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=VSS3=VSS4=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
DSP Section Input SDIN1/2					
Delay Time from BICLK1 "↑" to LRCLK1 SCKSEL bit= "0" (Note 38)	tBLRD	20			ns
Delay Time from LRCLK1 to BITCLK1 "↑" SCKSEL bit= "0" (Note 39)	tLRBD	20			ns
Delay Time from BICLK2 "↑" to LRCLK2 SCKSEL bit= "1" (Note 38)	tBLRD	20			ns
Delay Time from LRCLK2 to BITCLK2 "↑" SCKSEL bit= "1" (Note 39)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	80			ns
Serial Data Input Latch Hold Time	tBSIDH	80			ns
SRC Section Input SDIN2 (SCKSEL bit= "1")					
Delay Time from BICLK2 "↑" to LRCLK2 (Note 39)	tBLRD	20			ns
Delay Time from LRCLK2 to BITCLK2 "↑" (Note 39)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	40			ns
Serial Data Input Latch Hold Time	tBSIDH	40			ns
Output SDOUT1, SDOUT2, SDOUTM					
Delay Time from LRCLK1 to Serial Data Output (Note 40)	tLRD			80	ns
Delay Time from BICK1 "↓" to Serial Data Output (Note 41)	tBSOD			80	ns
Delay Time from LRCKO to Serial Data Output (Note 40)	tLRD			80	ns
Delay Time from BICKO to Serial Data Output (Note 42)	tBSOD			80	ns
SDIN1/2 →SDOUT1/2 (Note 43)					
Delay Time from SDIN1/2 to SDOUT1/2 Output	tIOD			60	ns

Note 38. BITCLKI1 edge must not occur at the same time as LRCLKI1 edge.
Note 39. BITCLKI2 edge must not occur at the same time as LRCLKI2 edge.
Note 40. Except I^2S.
Note 41. When BICK1 polarity is reversed, delay time is from BICK1 "↑".
Note 42. When BICK2 polarity is reversed, delay time is from BICK2 "↑".
Note 43. SDIN1 → SDOUT1: SELDO1[1:0] bits= "1h", OUT1E bit= "1"
SDIN2 → SDOUT2: SELDO2[1:0] bits= "1h", OUT2E bit= "1"

■ Digital Microphone (DMIC) Switching Characteristics

(Ta= -20˚C ~85˚C; AVDD=HVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1= VSS2= VSS3= VSS4= 0V, CL=100pF)

Parameter	Symbol	min	typ	max	Units
DMDAT					
DMDAT Setup Time	tDMDS	50			ns
DMDAT Hold Time	tDMDH	0			ns
DMCLK					
Frequency	fDMCK	0.5	64fs	3.1	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise Time	tDMCKR			10	ns
Fall Time	tDMCKF			10	ns

Note 44. Clock frequency is depend on the sampling rate (fs) which is set by CKM[1:0] or DFS[1:0] bits.

■ I²C BUS Interface

(Ta= -20ºC ~ 85ºC; AVDD=HVDD=DVDD= 3.0V ~ 3.6V, DVDD18= 1.7V ~ 1.9V, VSS1=VSS2=VSS3=VSS4=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL			400	KHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 45. I²C-bus is a trademark of NXP B.V.

■ **Timing Diagram**

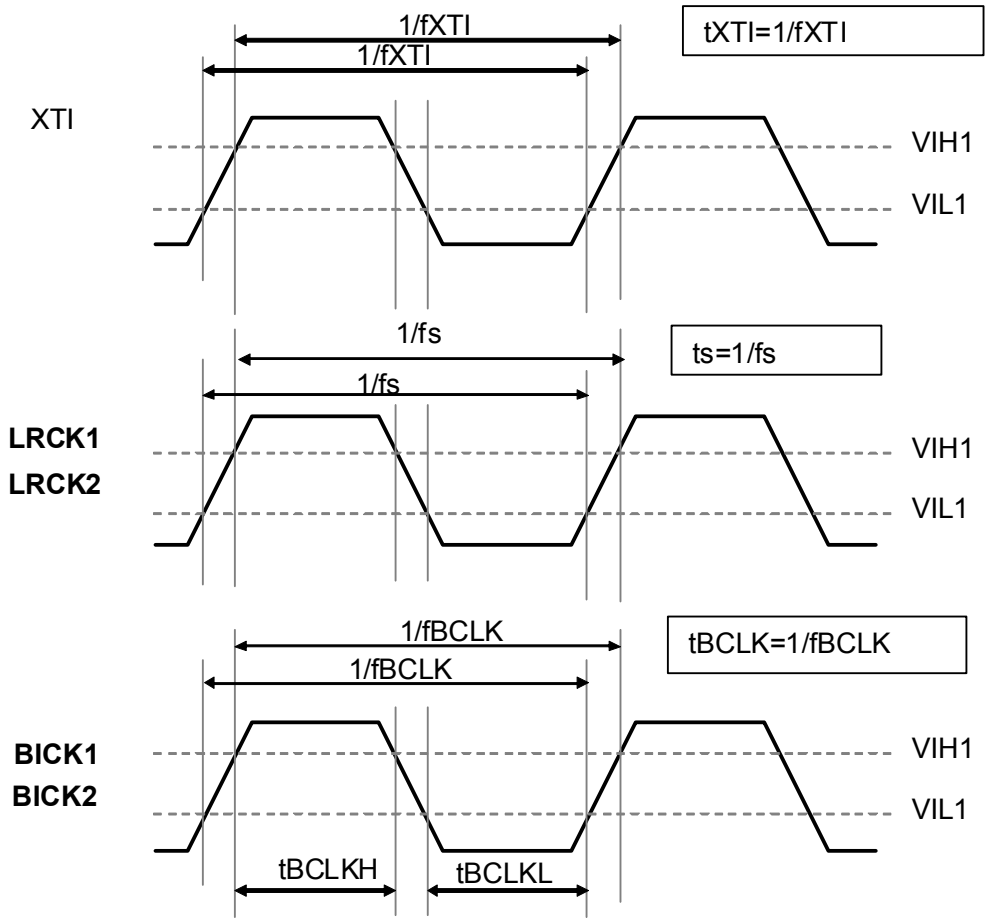


Figure 3. System Clock

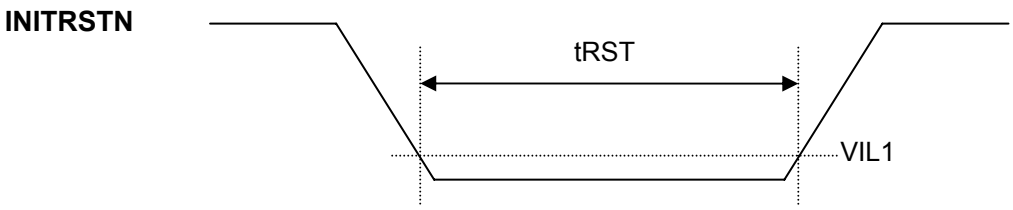


Figure 4. Reset

Note 46. The INITRSTN pin must be “L” when power-up/power-down the AK7754.

■ Audio Interface

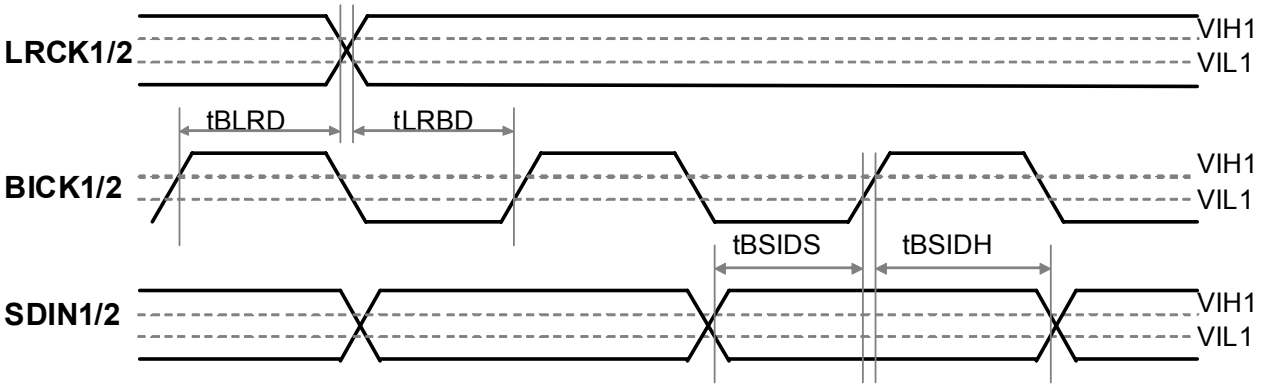


Figure 5. Audio Interface (DSP Section Slave Mode Input)

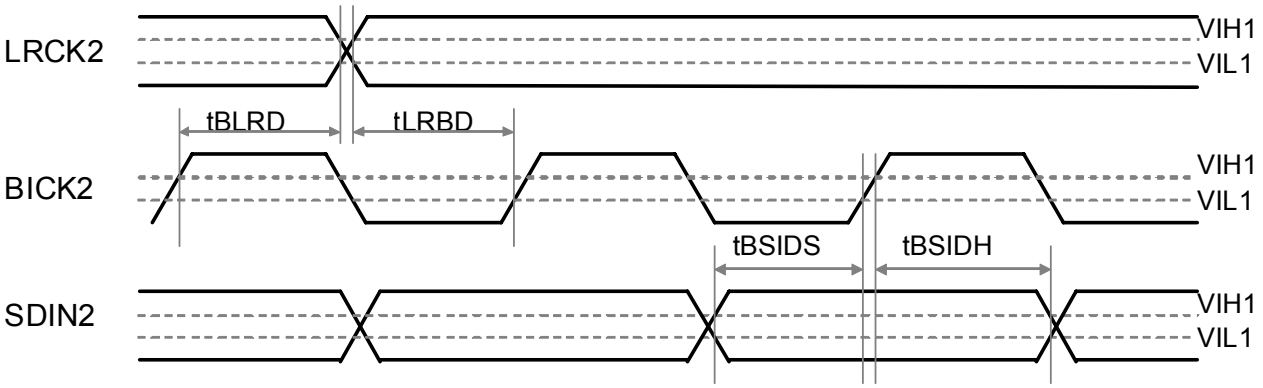


Figure 6. Audio Interface (SRC Section Input)

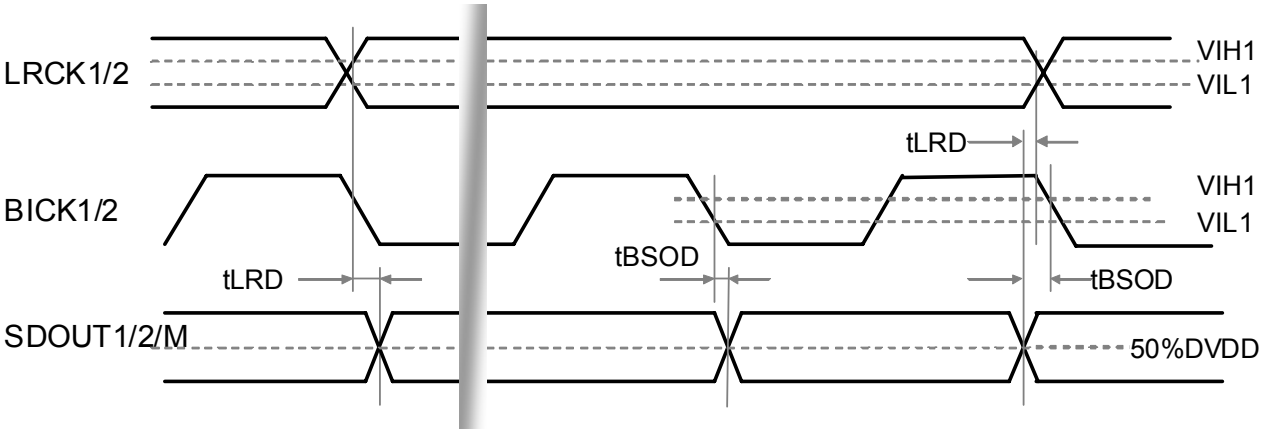


Figure 7. Audio Interface (Slave Mode Output)

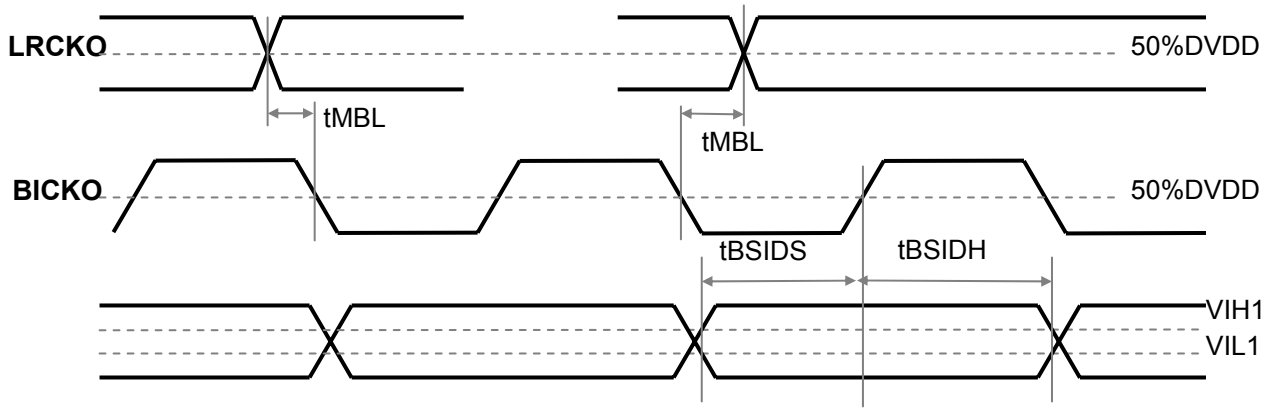


Figure 8. Audio Interface (Master Mode Input)

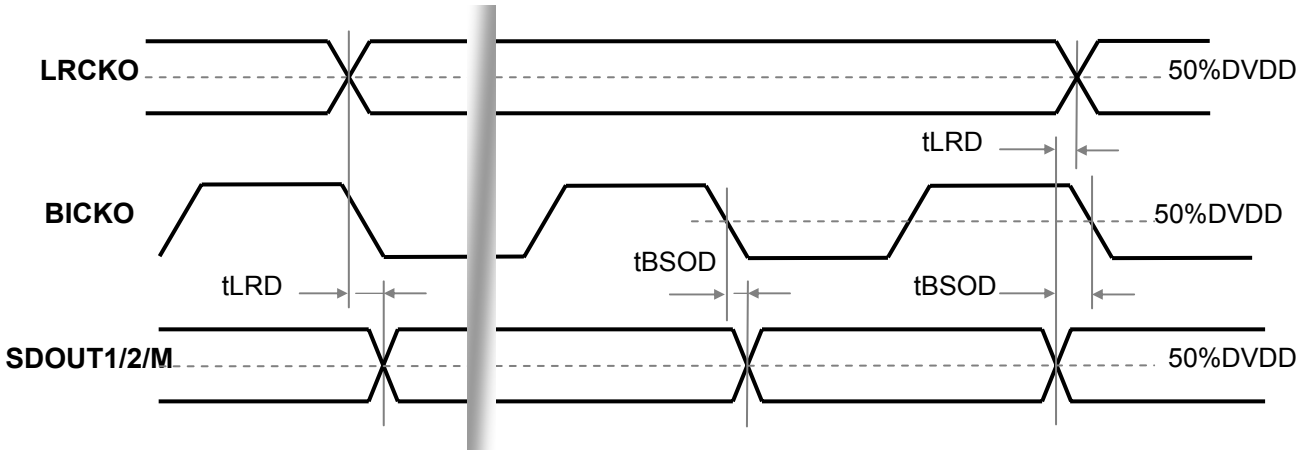


Figure 9. Audio Interface (Master Mode Output)

■ Digital Microphone Interface

Input Interface

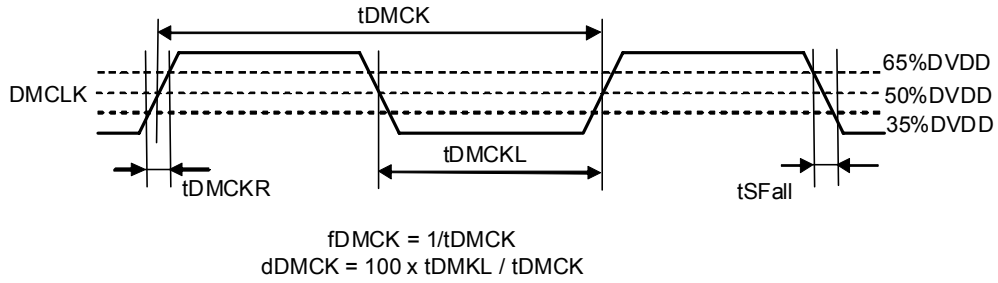


Figure 10. DMCLK Clock Timing

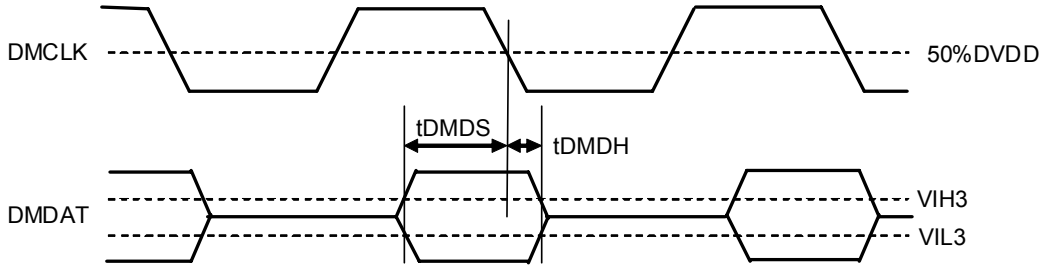


Figure 11. Audio Interface Timing, DCLKP bit = "1")

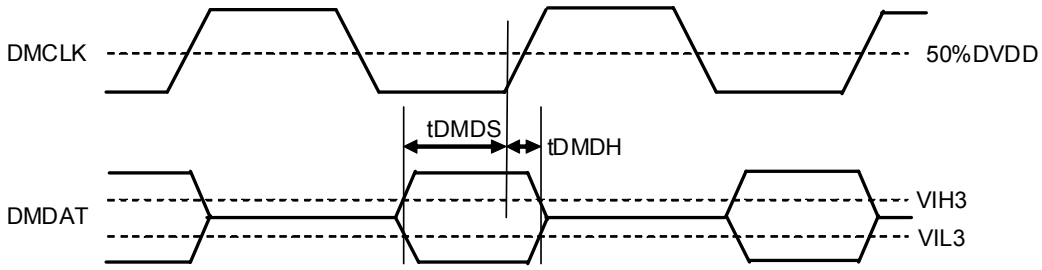


Figure 12. Audio Interface Timing, DCLKP bit = "0")

I²C Bus Interface

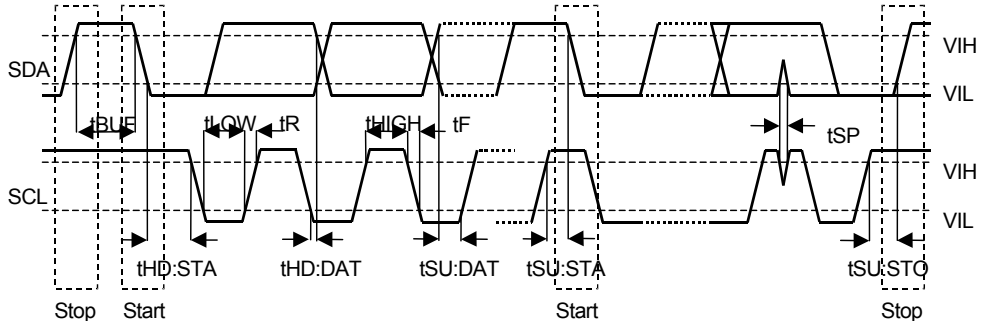
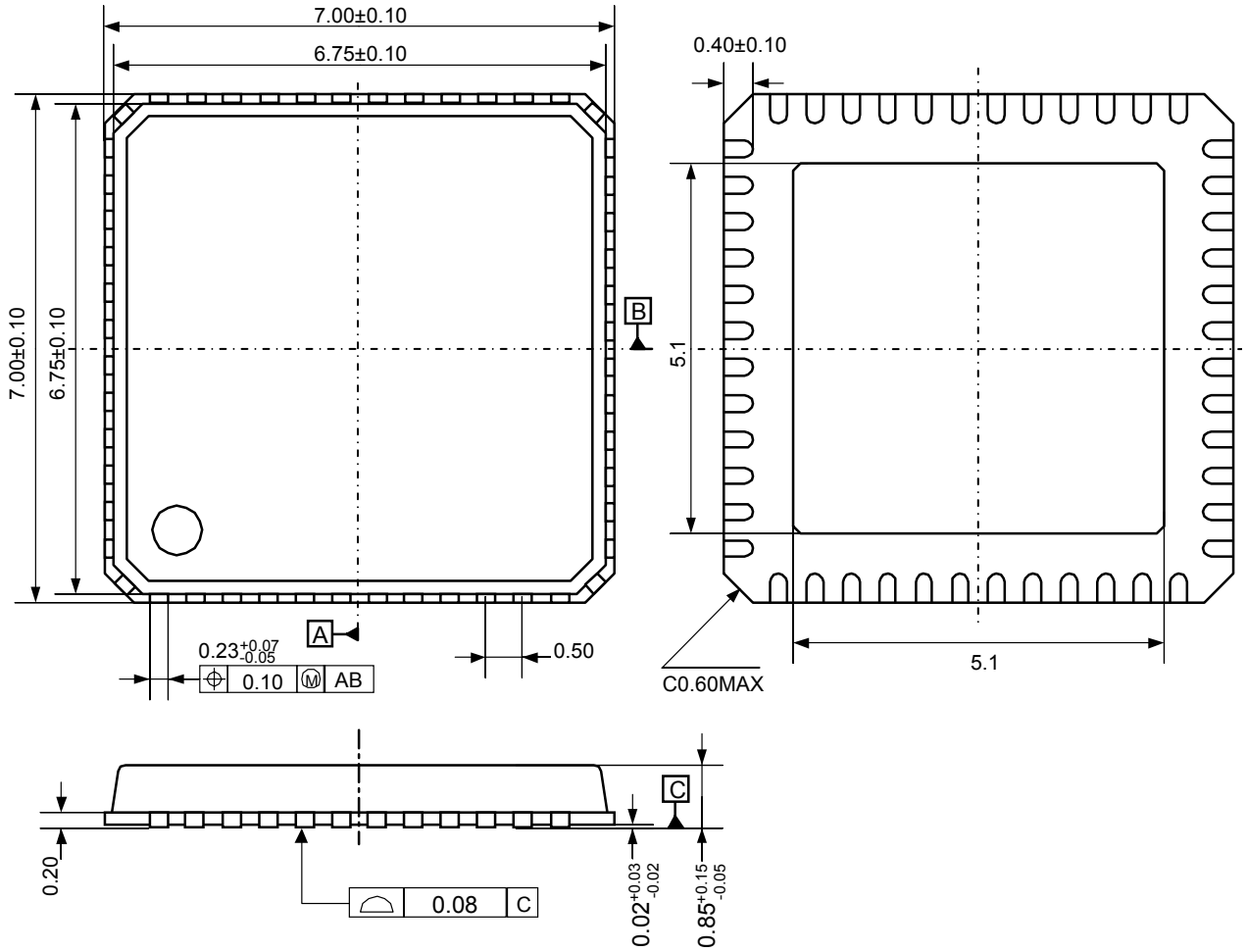


Figure 13. I²C Bus Interface

PACKAGE

48pin QFN (Unit: mm)

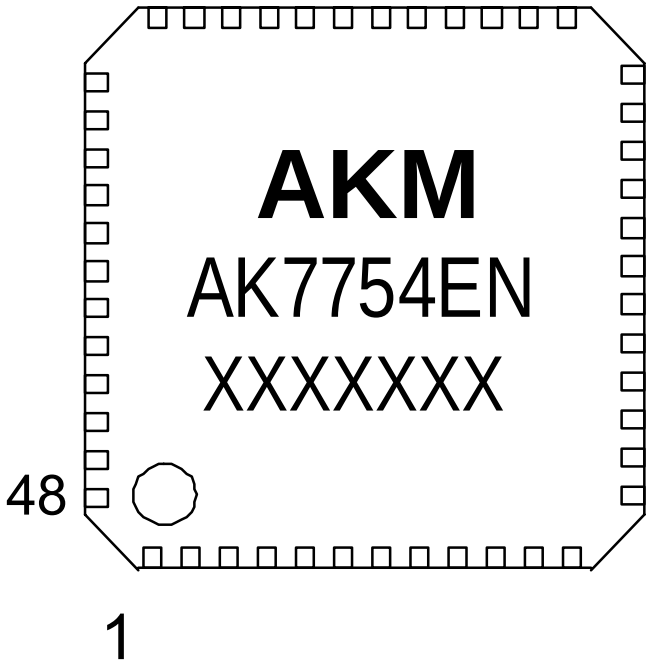


Note: The exposed pad on the bottom surface of the package must be open or connected to the ground.
A support lead on each corner is for mounting the exposed pad. They are tied to the exposed pad electrically.

■ Materials and Lead Specification

Package:	Epoxy, Halogen (bromine and chlorine) free
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

MARKING



XXXXXXX: Date code identifier (7 digits)

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
10/06/01	00	First Edition		
12/03/23	01	Error Correction	8	PIN FUNCTION IN2P (No. 43): MIC Differential Inverted Input Pin2 →MIC Differential Non-Inverted Input Pin2 IN2N (No. 45): MIC Differential Non-Inverted Input Pin2 →MIC Differential Inverted Input Pin2
12/05/18	02	Description Addition	24	PACKAGE The package drawing was changed. A description was added.

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