



Audio Clock Generator AK8128C

Features

- **Output Frequency Range:**
12.288MHz, 24.576MHz
33.8388MHz, 36.864MHz
- **Input Frequency:**
27MHz
- **Low Jitter Performance:**
20 ps (Typ.) Period, 1σ
290ps(Typ.) 1000cycle long term, p-p
- **Low Current Consumption:**
8mA (Typ.)
- **Output Load:**
15pF (max.)
- **Supply Voltage:**
3.0 – 3.6V
- **Operating Temperature Range:**
-20 to +85°C
- **Package:**
10-pin TMSOP (lead-free)

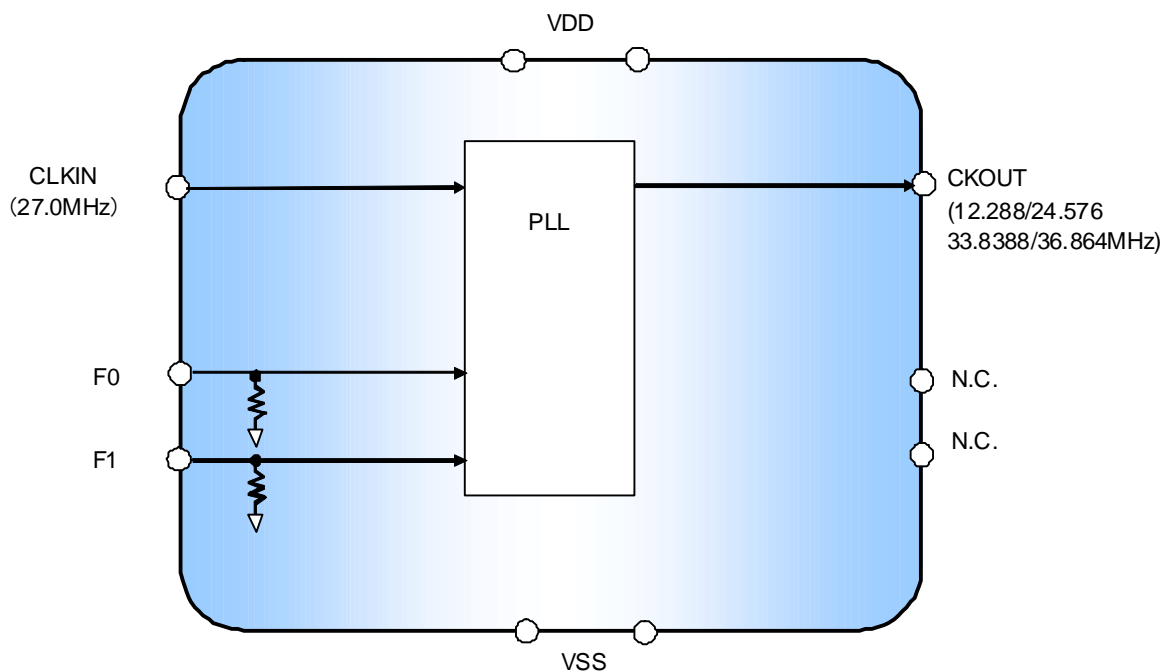
Description

The AK8128C is a single clock generator IC with an integrated PLL. It can generate Audio clock from a 27MHz master clock input frequency. A high performance PLL locks to the master clock input, generating a low jitter, highly accurate clock output without an external crystal.

Applications

- DTV
- PVR
- DVC
- DSC

Block Diagram



AK8128C Single Clock Generator

Pin Descriptions



Package: 10-Pin TMSOP (Top View)

Pin No.	Pin Name	Pin Type	Description
1	VDD	--	Power Supply
2	VSS	--	Ground
3	CLKIN	IN	27MHz External Clock Input
4	VSS	--	Ground
5	VDD	--	Power Supply
6	CKOUT	OUT	Clock Output
7	N.C	--	Connect to VSS
8	F0	IN	Clock Frequency Range Select Pin 0. (1) (2)
9	F1	IN	Clock Frequency Range Select Pin 1. (1) (2)
10	N.C	--	Connect to VSS

- (1) Internal pull down 400kΩ (Typ.)
- (2) See Table1 for output frequency settings.

Table 1: Operation Clock Frequency Setting

Pin Setting		CKOUT (MHz)
F1	F0	
L	L	33.8688
L	H	36.864
H	L	12.288
H	H	24.576

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8128C	128C	Tape and Reel	10-pin TMSOP	-20 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted ⁽¹⁾

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	V _{in}	VSS-0.3 to VDD+0.3	V
Input Current (any pins except supplies)	I _{IN}	±10	mA
Storage Temperature	T _{stg}	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.



ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature	T _a		-20		85	°C
Supply Voltage	VDD		3.0	3.3	3.6	V
Input Clock Frequency	F _{in}			27		MHz
Input Clock Duty Cycle			30	50	70	%
Output Load Capacitance	C _{pl}				15	pF

Note:

(1) Power to VDDs requires to be supplied from a single source. A decoupling capacitor of 0.01μF for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta: -20 to +85°C, Input Frequency: 27MHz, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V _{IH}	Pin: CLKIN, FSEL, OE	0.7VDD			V
Low Level Input Voltage	V _{IL}	Pin: CLKIN, FSEL, OE			0.3VDD	V
Input Current 1	I _{L1}	Pin: CLKIN	-10		+10	μA
Input Current 2	I _{L2}	Pin: F0,F1	-20		+20	μA
High Level Output Voltage	V _{OH}	Pin: CLKOUT I _{OH} =-4mA	0.8VDD			V
Low Level Output Voltage	V _{OL}	Pin: CLKOUT I _{OL} =+4mA			0.2VDD	V
Current Consumption	I _{DD}	No load @36.864MHz (VDD=3.3V, Ta=25°C)		8	10	mA

AC Characteristics

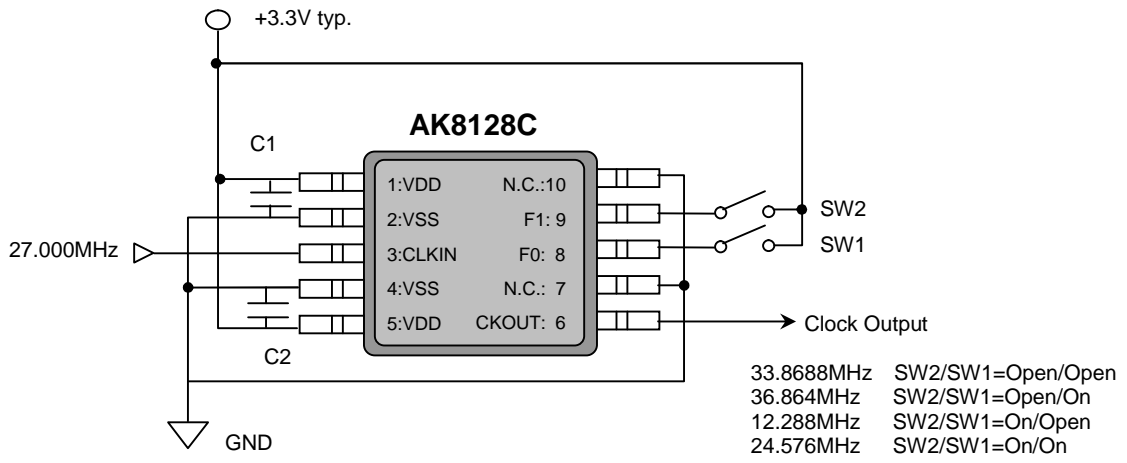
All specifications at VDD: over 3.0 to 3.6V, Ta: -20 to +85°C, Input Frequency: 27MHz, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Frequency		F1/F0="LL" F1/F0="LH" F1/F0="HL" F1/F0="HH"	-	33.8688 36.864 12.288 24.576	-	MHz
Output Clock Duty Cycle			45	50	55	%
Output Clock Rise Time ⁽²⁾	t _{rise}	0.2VDD to 0.8VDD		1.5	2.0	ns
Output Clock Fall Time ⁽²⁾	t _{fall}	0.2VDD to 0.8VDD		1.5	2.0	ns
Output Clock Jitter 1	Jit1	Period, 1σ in 10000 sampling		20	100	ps
Output Clock Jitter 2	Jit2	Long term 1000 cycle p-p ±3σ in 10000 sampling		290	550	ps
Output Lock Time ⁽¹⁾	t _{lock}	Power-up		1	3	ms

(1) The time that output reaches the target frequency within accuracy of ±0.1% from the point that the power supply reaches VDD

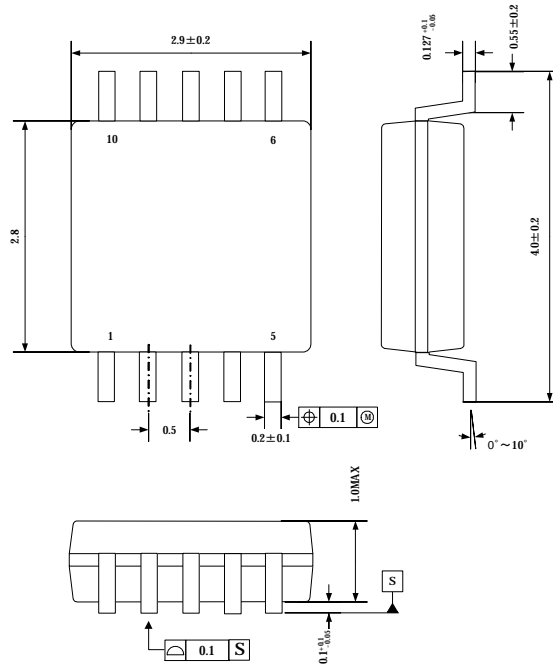
(2) With the load capacitance specified by the recommended operation conditions

Typical Connection Diagram

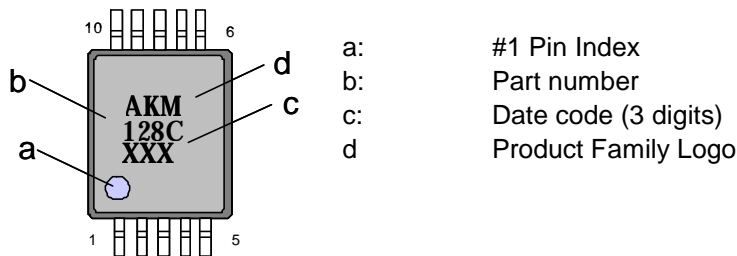


Package Information

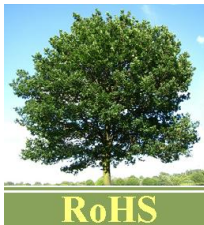
• Mechanical data



• Marking



• RoHS Compliance



All integrated circuits from Asahi Kasei Microdevices Corporation (AKM) assembled in “lead-free” packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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It is noted the documents according to this product, which was released before the date of 1st April 2009, shall include the old company name as Asahi Kasei EMD Corporation (AKEMD). These documents will be continuously valid by interpreting the old company