AK8140A

Programmable Multi Clock Generator with XO

1. General Description

The AK8140A is a member of AKM's High-performance programmable clock generator.
The AK8140A generates up to four output clocks from a single input frequency with two fractional-N PLLs. Each output can be programmed for any frequency up to 230MHz. PLLs in AK8140A are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption.
The AK8140A is available in a 24-pin HTSSOP package.

2. Features

- In-System Programmability
  - Serial Programmable Register via SDA/SCL pin
- High Accuracy Clock Generator
- Flexible Input Clock Source
  - Crystal Unit : 16MHz - 60MHz
  - External Clock : 4MHz - 100MHz
- Free Programmable Clock Frequencies
  - LVCMOS : up to 160MHz (CLK1-4)
  - LVDS : up to 230MHz (CLK4p/n)
- Low Jitter Performance by using PLL2
  - Period Jitter (1σ) : 8.3ps Max.
  - Cycle to Cycle Jitter (1σ) : 12.8ps Max.
  - Long Term Jitter (1000 cycle, 1σ) : 41.7ps Max.
- Supply Voltage
  - Device Power Supply : VDD1-4 : 3.0 – 3.6V
  - Output Buffer Power Supply : VDDO1-2 : 1.7 – 3.6V
- Operating Temperature Range
  - -40 to +85°C
- Package
  - 24-pin HTSSOP (Lead free)
- Application
  - Automotive Ethernet AVB System, Automotive Video System, Car Navigation and Display Audio
  - Audio Amplifier System, AV Receiver, DTV System, STB, IP-STB, DVD Player and DVD Recorder

4. Block Diagram and Functions

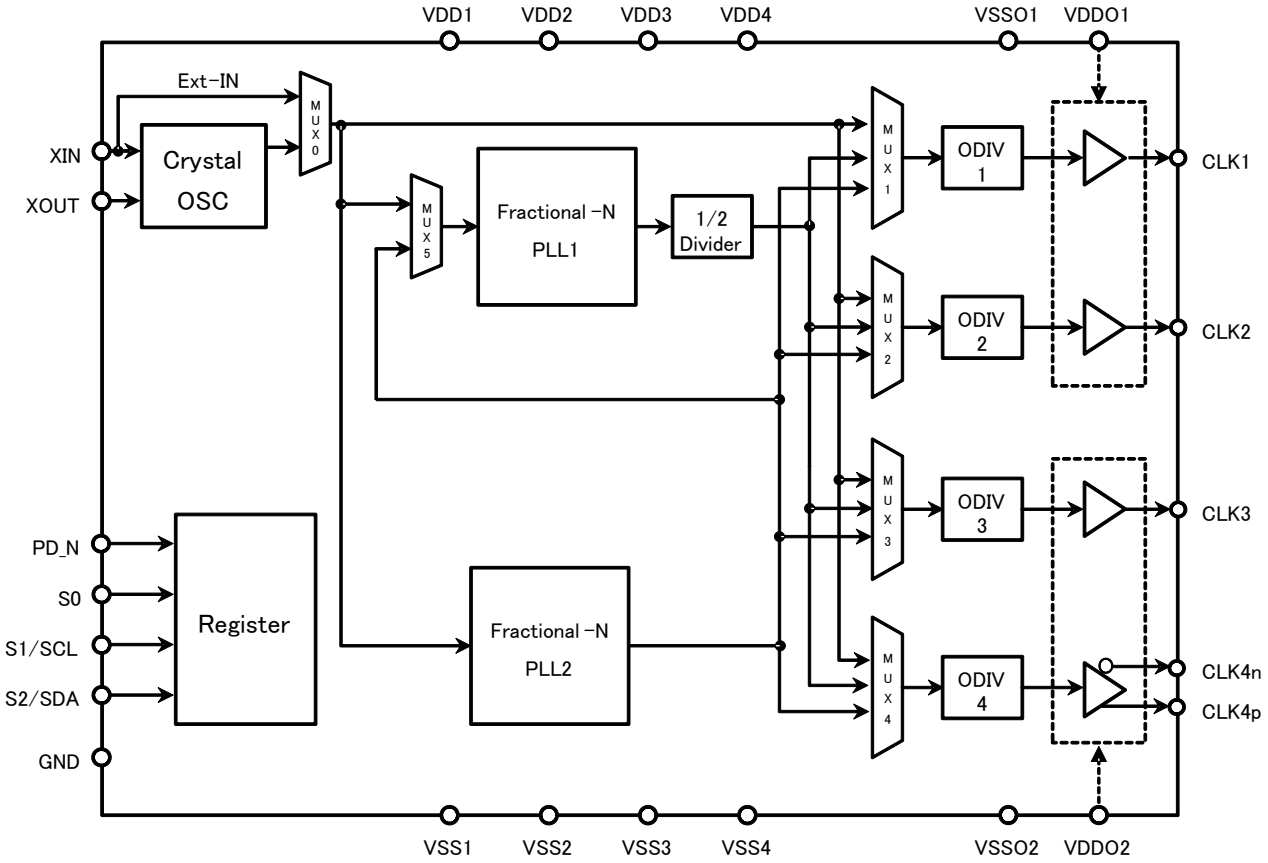


Figure 1. AK8140A Programmable Multi Clock Generator with XO

5. Pin Configurations and Functions

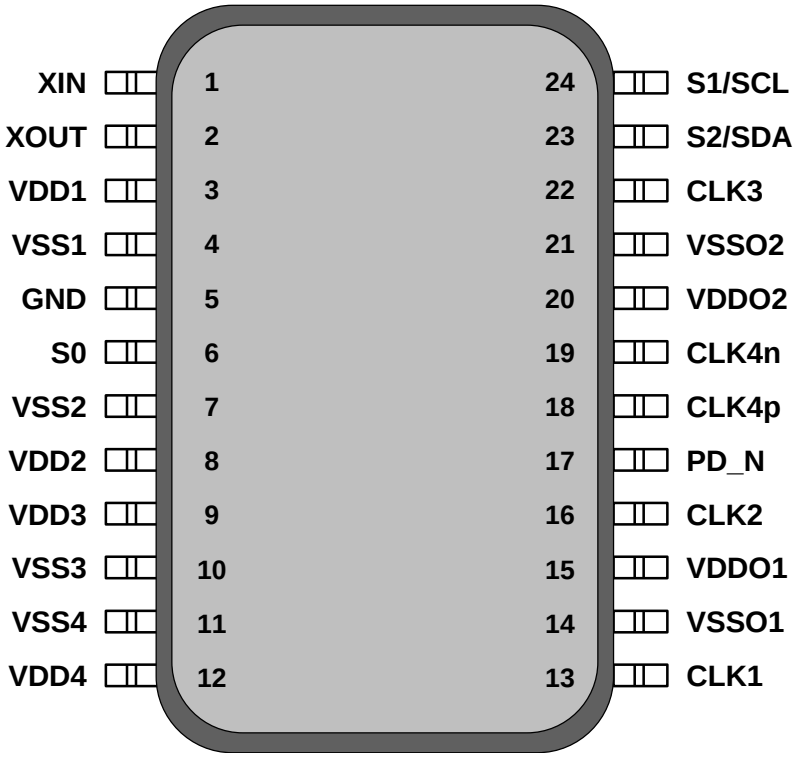


Figure 2. AK8140A Package: 24-Pin HTSSOP (Top View)

Pin No.	Pin Name	Pin Type	Description
1	XIN	AI	Crystal connection (Default) or External clock input When Crystal connection is selected, OSC_DIS bit should be set '0'. When External clock input is selected, OSC_DIS bit should be set '1'.
2	XOUT	AO	Crystal connection Open when an external clock input is used.
3	VDD1	PWR	Device Power Supply 1
4	VSS1	PWR	Connect to Ground
5	GND	AI	Connect to Ground
6	S0	DI	Programmable control pin 0 Connect to Ground when S0 pin isn't used.
7	VSS2	PWR	Connect to Ground
8	VDD2	PWR	Device Power Supply 2
9	VDD3	PWR	Device Power Supply 3
10	VSS3	PWR	Connect to Ground
11	VSS4	PWR	Connect to Ground
12	VDD4	PWR	Device Power Supply 4
13	CLK1	DO	LVCMOS Output pin1 When VDDO1 = 1.8V, CLK1MOD bit should be set '0' (Default). When VDDO1 = 3.3V, CLK1MOD bit should be set '1'.
14	VSSO1	PWR	Connect to Ground for Output Buffer

Pin No.	Pin Name	Pin Type	Description
15	VDDO1	PWR	Power Supply1 for Output Buffer CLK1 and CLK2
16	CLK2	DO	LVCMOS Output pin2 When VDDO1 = 1.8V, CLK1MOD bit should be set '0' (Default). When VDDO1 = 3.3V, CLK1MOD bit should be set '1'.
17	PD_N	DI	Power Down Control pin L : Device is powered down, all outputs are low. H : PLLs and all outputs are normal operation.
18	CLK4p	DO	LVDS (Default) / LVCMOS Output pin4 Output Interface is changed by CLK4_CMOS bit (Address: 03h). When LVDS is selected, CLK4_CMOS bit should be set '0'. When LVCMOS is selected, CLK4_CMOS bit should be set '1'. CLK4p and CLK4n Output is Opposite when LVCMOS Output. When VDDO2 = 1.8V, CLK4MOD bit should be set '0' (Default). When VDDO2 = 3.3V, CLK4MOD bit should be set '1'.
19	CLK4n	DO	
20	VDDO2	PWR	Power Supply2 for Output Buffer CLK3 and CLK4
21	VSSO2	PWR	Connect to Ground for Output Buffer
22	CLK3	DO	LVCMOS Output pin3 When VDDO1 = 1.8V, CLK1MOD bit should be set '0' (Default). When VDDO1 = 3.3V, CLK1MOD bit should be set '1'.
23	S2/SDA	DIO	Dual function pin S2 : Programmable control pin2, SDA : Serial Data Input / Output (Default) Internal Pull Up Resistance : 500 kΩ When SPICON bit = SPICON_SET bit = '1', Pin 23 becomes S2 pin for Programmable control pin. Refer to Page 29.
24	S1/SCL	DI	Dual function pin S1 : Programmable control pin1, SCL : Serial Clock Input (Default) Internal Pull Down Resistance : 500 kΩ When SPICON bit = SPICON_SET bit = '1', Pin 24 becomes S1 pin for Programmable control pin. Refer to Page 29.

Note:

(1) AI : Analog Input pin, AO : Analog Output pin, DI : Digital Input pin, DO : Digital Output pin
DIO : Digital Input and Output pin, PWR : Power Supply pin

(2) The Heat sink pad on the bottom surface of the package is recommended to solder to the PCB.

6. Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	Pin: VDD1-4	3.0	3.3	3.6	V
	VDDO1	Pin: VDDO1 Power Supply for CLK1 and CLK2 Output Buffers	1.7 3.0	1.8 3.3	1.9 3.6	
	VDDO2	Pin: VDDO2 Power Supply for CLK3 and CLK4 Output Buffers	1.7 2.3 3.0	1.8 2.5 3.3	1.9 2.7 3.6	
Output Load Capacitance (2)	Cplclk	Pin: CLK1-3 Output Frequency : up to 50MHz			25	pF
		Pin: CLK1-3 Output Frequency : up to 120MHz			15	
		Pin: CLK1-3 Output Frequency : up to 160MHz			10	
		Pin: CLK4p/n LVCMOS output Output Frequency : up to 160MHz			10	

Note:

(1) Power to VDD1-4 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pins.

(2) Output load for CLK4p/n pins at LVDS output is descripted on page 11 for details.

8. Electrical Characteristics

DC Characteristics

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	Pin: S0, PD_N, S1/SCL, S2/SDL, XIN	0.7*VDD			V
Low Level Input Voltage	V_{IL}	Pin: S0, PD_N, S1/SCL, S2/SDL, XIN			0.3*VDD	V
Input Current 1	I_L1	Pin: S0, PD_N VDD or VSS force	-1		+1	μA
Input Current 2	I_L2	Pin: S1/SCL VDD or VSS force	-1		+20	μA
Input Current 3	I_L3	Pin: S2/SDA VDD or VSS force	-20		+1	μA
Low Level Output Voltage	V_{OL}	Pin: SDA I_{OL} = +3mA, Open Drain			0.2*VDD	V
Current Consumption 1	$I_{DD}1$	All outputs 'ON', No load Input / Output frequency XIN: 100MHz CLK1-3: 160MHz CLK4p/n LVDS: 230MHz		58	70	mA
Current Consumption 2	$I_{DD}2$	All outputs 'OFF' Input / Output frequency XIN: 100MHz CLK1-3: 'L'/ 'H'/'Hi-Z' output CLK4p/n : 'L'/ 'H'/'Hi-Z' output		15	20	mA
Power Down Mode Current Consumption	SI_{DD}	No load, Power Down Mode PD_N = 'L'		0.5	50	μA

AC Characteristics

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Clock Frequency	F_{osc}	Pin: XIN, XOUT	16		60	MHz
External Clock Input Frequency	F_{in}	Pin: XIN When External Input is selected. OSC_DIS = '1'	4		100	MHz
External Clock Input Duty Cycle	F_{indc}	Pin: XIN When External Input is selected Measurement point: 0.5VDD	30	50	70	%
Output Clock Frequency Accuracy (1)(2)	$F_{accuracy}$	Pin: CLK1-3, CLK4p/n	-30		+30	ppm
Output Lock Time (3)	T_{lock}	Pin: CLK1-3, CLK4p/n		0.25	1	ms

Note:

(1) Specification of Frequency Accuracy is measured by connecting the standard crystal unit for DSX321G of DAISHINKU Corp. on page 49.

(2) This Output Clock Frequency Accuracy does not include accuracy of crystal unit. Total output clock frequency accuracy could be up to "Output Clock Frequency Accuracy" + "Crystal unit accuracy".

(3) Settling time that output frequency reaches within the accuracy 0.1 % of the target frequency after registers "20h to 2Bh" or "30h to 38h" are set through SCA/SCL pins.

PLL Characteristics

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PLL1 Characteristics						
VCO Frequency 1	fVCO1	VCO frequency range of PLL1	230		460	MHz
Phase Comparison Frequency 1	fcmp1		6.75		13.5	MHz
Period Jitter 1 (1)(2)(3)(6)	$Jit_{\_period}$	Jitter of Output Clock from PLL1, 1σ		8.3		ps
Cycle to Cycle Jitter 1 (1)(2)(4)(6)	$Jit_{\_c2c}$	Jitter of Output Clock from PLL1, 1σ		12.8		ps
Long Term Jitter 1 (1)(2)(5)(6)	$Jit_{\_long}$	Jitter of Output Clock from PLL1, 1000 cycle delay, 1σ		40		ps
PLL2 Characteristics						
VCO Frequency 2	fVCO2	VCO frequency range of PLL2	80		230	MHz
Phase Comparison Frequency 2	fcmp2		2.5		14.375	MHz
Period Jitter 2 (1)(2)(3)(6)	$Jit_{\_period}$	Jitter of Output Clock from PLL2, 1σ			8.3	ps
Cycle to Cycle Jitter 2 (1)(2)(4)(6)	$Jit_{\_c2c}$	Jitter of Output Clock from PLL2, 1σ			12.8	ps
Long Term Jitter 2 (1)(2)(5)(6)	$Jit_{\_long}$	Jitter of Output Clock from PLL2, 1000 cycle delay, 1σ			41.7	ps

Note:

(1) The load conditions are described on page 6.

(2) CLK1 or CLK2 is enabled or CLK1 and CLK2 output the same frequency. Similarly, CLK3 or CLK4p/n is enabled or CLK3 and CLK4p/n output the same frequency.

(3) Jitter depends on configuration. Jitter data is for input frequency = 48MHz, output frequency = 27MHz/48MHz/50MHz.

(4) Jitter depends on configuration. Jitter data is for input frequency = 25MHz/30MHz/50MHz, output frequency = 27MHz/50MHz.

(5) Jitter depends on configuration. Jitter data is for input frequency = 27MHz, output frequency = 25M/148.5MHz.

(6) 10,000 sampling or more

LVCMOS Characteristics

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Frequency	fout	Pin: CLK1-3, CLK4p/n			160	MHz
High Level Output Voltage	V_{OH}	Pin: CLK1-3, CLK4p/n I_{OH} = -4mA	0.8VDDO1-2			V
Low Level Output Voltage	V_{OL}	Pin: CLK1-3, CLK4p/n I_{OH} = +4mA			0.2VDDO1-2	V
Output Clock Rise Time (1)(2)(3)	$T_{\_rise}$	Pin: CLK1-3 Load Cplclk = 10pF 0.2VDDO1-2 → 0.8VDDO1-2		0.7		ns
		Pin: CLK1-3 Load Cplclk = 25pF 0.2VDDO1-2 → 0.8VDDO1-2		1.2		ns
		Pin: CLK4p/n, VDDO2 = 3.3V Load Cplclk = 10pF 0.2VDDO2 → 0.8VDDO2		0.3		ns
Output Clock Fall Time (1)(2)(3)	$T_{\_fall}$	Pin: CLK1-3 Load Cplclk = 10pF 0.8VDDO1-2 → 0.2VDDO1-2		0.7		ns
		Pin: CLK1-3 Load Cplclk = 25pF 0.8VDDO1-2 → 0.2VDDO1-2		1.2		ns
		Pin: CLK4p/n, VDDO2 = 3.3V Load Cplclk = 10pF 0.8VDDO2 → 0.2VDDO2		0.3		ns
Output Clock Duty Cycle (1)	$T_{\_outdc}$	Pin: CLK1-3, CLK4p/n (4)	45	50	55	%
		Pin: CLK1-3, CLK4p/n (5)	45	50	55	%
		Pin: CLK1-3, CLK4p/n (6)	20		80	%

Note:

(1) The load conditions are described on page 6
(2) When VDDO1-2 = 1.8V: CLKnMOD (n = 1-3) = "0", when VDDO1-2 = 3.3V: CLKnMOD (n = 1-3) = "1".
(3) When VDDO1-2 = 3.3V: CLK4MOD = "1".
(4) When ODIVn divides the PLL1/2 Clock.
(5) When ODIVn divides the Input Bypass Clock by even dividing value.
(6) When ODIVn divides the Input Bypass Clock by odd dividing value.

CLK4p/n LVDS Characteristics

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Frequency	fout				230	MHz
Single Output Voltage (1)	V_{OD}		250	350	450	mVpp
Offset Voltage (1)	V_{OS}	VDDO2 = 2.3 to 3.6V, CLK4MOD = "1"	1.125	1.240	1.375	V
		VDDO2 = 1.7 to 1.9V, CLK4MOD = "0"	0.685	0.800	0.935	V
Output Clock Rise Time (1)	$T_{\_rise}$	0.2VDDO1-2 → 0.8VDDO1-2		0.2		ns
Output Clock Fall Time (1)	$T_{\_fall}$	0.8VDDO1-2 → 0.2VDDO1-2		0.2		ns
Output Clock Duty Cycle (1)	$T_{\_outdc}$	(2)	45	50	55	%
		(3)	45	50	55	%
		(4)	20		80	%

Note:
(1) LVDS clock measured at the circuit shown in Figure 3.
(2) When ODIV4 divides the PLL1/2 Clock.
(3) When ODIV4 divides the Input Bypass Clock by even dividing value.
(4) When ODIV4 divides the Input Bypass Clock by odd dividing value.

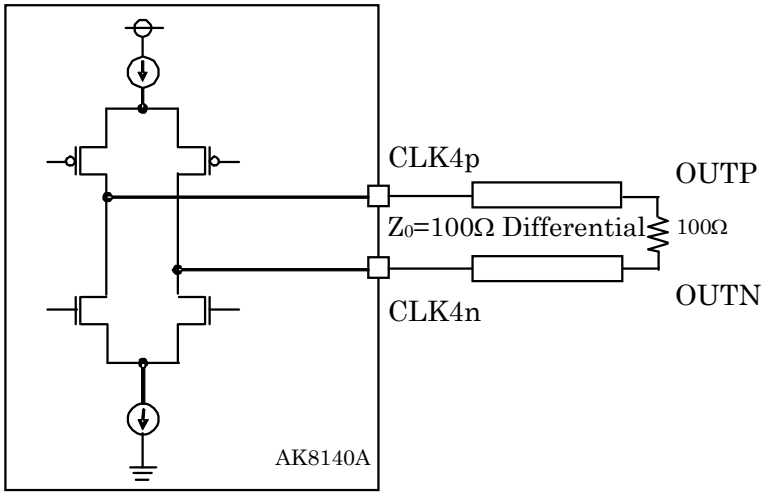


Figure 3. CLK4p/n LVDS Clock measurement circuit

Serial Interface (SDA/SCL pin) AC Characteristics (1)

All specifications at VDD1-4: over 3.0 to 3.6V, VDDO1-2: over 1.7 to 3.6V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	fSCL				400	kHz
SCL Clock Low Period	tLOW		1.3			µs
SCL Clock High Period	tHIGH		0.6			µs
Pulse Width of Spikes which must be suppressed	tI				50	ns
SCL Low to SDA Data Out	tAA		0.3			µs
Bus free time between a STOP and START Condition	tBUF		1.3			µs
Start Condition Hold Time	tHD.SAT		0.6			µs
Start Condition Setup Time (for a Repeated Start Condition)	tSU.SAT		0.6			µs
Data in Hold Time	tHD.DAT		0			µs
Data in Setup Time	tSU.DAT		100			ns
SDA and SCL Rise Time	tR				0.3	µs
SDA and SCL Fall Time	tF				0.3	µs
Stop Condition Setup Time	tSU.STO		0.6			µs
Input Capacitance at SDA/SCL	Cb				200	pF

Note:

(1) The AK8140A operates as a slave device of the 2-wire serial SDA/SCL bus.
This serial interface can be used the I^2C interface timing.
It operates in the standard-mode transfer (up to 100kbit/s) and the fast-mode transfer (up to 400kbit/s).
It doesn't support the Clock Stretching Mode and the High Speed Mode.

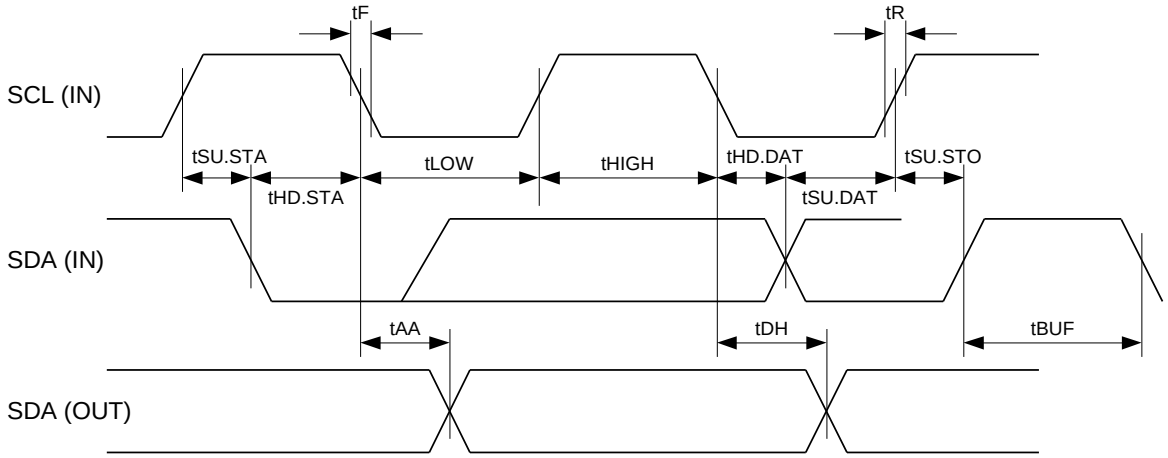


Figure 4. 2-wire Serial Interface AC Timing

9. Functional Descriptions

PLL1 setting procedure

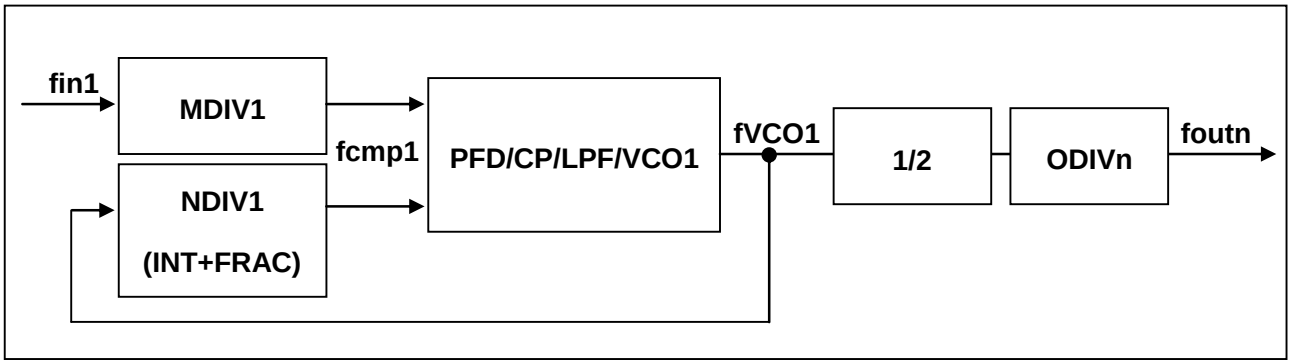


Figure 5. PLL1 Block Diagram

PLL1 is Fractional-N PLL.
Output frequency from PLL1 is determined by PLL1 parameter:
Refclk Dividing Value (MDIV1), Fractional-N1 Dividing Value (INT + FRAC), and Output Dividing Value (ODIVn(n = 1-4)).

These parameters should be set as described below.

Step1. Deciding VCO1 Target Frequency.

VCO1 Frequency (fVCO1) is decided from CLKn Output frequency (foutn) and Output Dividing Value (ODIVn, set by address: 0Dh ~ 13h). Set fVCO1 frequency between 230MHz to 460MHz.

$230\text{MHz} \leq \text{fVCO1} \leq 460\text{MHz}$ (fVCO1 = fount × 2 × ODIVn)

Step2. Deciding Phase Comparison Frequency.

Set MDIV1 Divider (MDIV, set by address: 26h or 2Bh) as fcmp1 becomes the greatest common measure of fin1 and fvco1 between 6.75MHz to 13.5MHz.

$6.75\text{MHz} \leq \text{fcmp1} \leq 13.5\text{MHz}$ (fcmp1 = fin1 / MDIV1)

Step3. Deciding Feedback Dividing Value.

This value is decided by VCO1 frequency (fVCO1) and Phase Comparison Frequency (fcmp1).
7 bits integral part and 18 bits fractional part (signed 2's complement) is necessary to be set.

$$\text{NDIV1} = \frac{\text{fVCO1}}{\text{fcomp1}} = \text{N}_{\text{INT1}} + \frac{\text{N}_{\text{FRAC1}}}{2^{18}}$$

Integral part (N_{INT1}) : N_{INT1} = INT[6:0] = round [fVCO1 / fcmp1]
Fractional part ($N_{FRAC1} / 2^{18}$) : N_{FRAC1} = FRAC[17:0] = round [((fVCO1 / fcmp1) – N_{INT1}) × 2^{18}]

Example1) input frequency = 27MHz, output frequency = 123.75MHz

1. fVCO1
   VCO1 Frequency: 247.5MHz ODIV = 1
   fVCO1 = 123.75MHz × 2 × 1 = 247.5MHz

2. fcmp1
   Phase Comparison Frequency1: 9MHz MDIV = 3
   fcmp1 = 27MHz / 3 = 9MHz

3. NDIV1
   Feedback Dividing Value: NDIV1 = fVCO1 / fcmp1 = 247.5 / 9 = 27.5
   N_{INT1} = round [247.5 / 9] = round [27.5] = 28
   N_{INT1} = 28, N_{FRAC1} / 2^{18} = -0.5

   FRAC[17:0] = round [(27.5 – 28) × 2^{18}] = -131072
   Output Frequency Error: 0ppm

Example2) input frequency = 16MHz, output frequency = 24.576MHz

1. fVCO1
   VCO1 Frequency: 442.368MHz ODIV = 9
   fVCO1 = 24.576MHz × 2 × 9 = 442.368MHz

2. fcmp1
   Phase Comparison Frequency1: 8MHz MDIV = 2
   fcmp1 = 16MHz / 2 = 8MHz

3. NDIV1
   Feedback Dividing Value: NDIV1 = fVCO1 / fcmp1 = 442.368 / 8 = 55.296
   N_{INT1} = round [442.368 / 8] = round [55.296] = 55
   N_{INT1} = 55, N_{FRAC1} / 2^{18} = 0.296

   FRAC[17:0] = round [(55.296 – 55) × 2^{18}] = 77595
   Output Frequency Error: 0.026ppm (0.64Hz)

PLL2 setting procedure

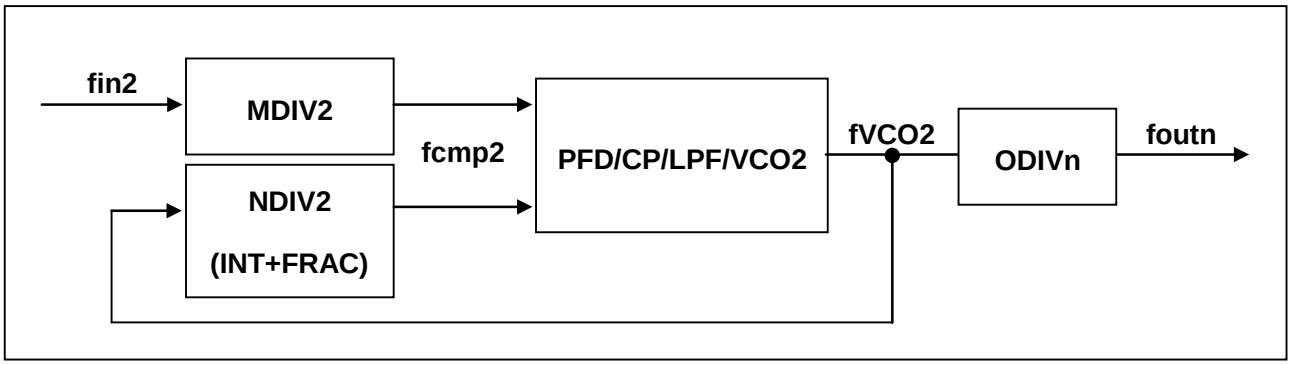


Figure 6. PLL2 Block Diagram

PLL2 is Fractional-N PLL.
Output frequency from PLL2 is determined by PLL2 parameter:
Refclk Dividing Value (MDIV2), Fractional-N2 Dividing Value (INT + FRAC), and Output Dividing Value (ODIVn(n = 1-4)).

These parameters should be set as described below.

Step1. Deciding VCO2 Target Frequency.

VCO2 Frequency (fVCO2) is decided from CLKn Output frequency (foutn) and Output Dividing Value (ODIVn, set by address: 0Dh ~ 13h). Set fVCO2 frequency between 80MHz to 230MHz.

80MHz ≤ fVCO2 ≤ 230MHz (fVCO2 = fount × ODIVn)

Step2. Deciding Phase Comparison Frequency.

Set MDIV2 Divider (MDIV[2:0], set by address: 31h or 35h) as fcmp2 becomes the greatest common measure of fin2 and fvco2 between 2.5MHz to 14.735MHz.

2.5MHz ≤ fcmp2 ≤ 14.735MHz (fcmp2 = fin2 / MDIV2)

Step3. Deciding Feedback Dividing Value.

This value is decided by VCO2 frequency (fVCO2) and Phase Comparison Frequency (fcmp2).
6 bits integral part (NINT[5:0], set by address: 32h or 36h) and 9 bits fractional part (numerator: NUME0[8:0] and denominator: NDENO0[8:0], set by address: 32h ~ 34h or 36h ~ 38h) is necessary to be set.

$$NDIV2 = \frac{fVCO2}{fcomp2} = N_{INT2} + N_{FRAC2} = N_{INT2} + \frac{N_{NUME}}{N_{DENO}}$$

Integral part = N_{INT2} = NINT[5:0] = round [fVCO2 / fcmp2]

Fractional part = $N_{FRAC2} = N_{NUME} / N_{DENO}$ is calculated as below.

First calculate optimum $N_{DENO} = NDENO[8:0]_{OPTIMUM}$.
$NDENO[8:0]_{OPTIMUM}$ can be obtained by substituting from 1 to 511 into the NDENO[8:0] in the following formula.

When min [abs [(round [N_{FRAC2} × NDENO[8:0]]) / NDENO[8:0]) – N_{FRAC2}]]
$NDENO[8:0]_{OPTIMUM}$ = NDENO[8:0]

$NUME[8:0]_{OPTIMUM}$ can be obtained by substituting $NDENO[8:0]_{OPTIMUM}$ in the following formula.

$NUME[8:0]_{OPTIMUM}$ = round [N_{FRAC2} × $NDENO[8:0]_{OPTIMUM}$]

Example1) input frequency = 27MHz, output frequency = 54MHz

1. fVCO2
   VCO2 Frequency: 216MHz ODIV = 4
   fVCO2 = 54MHz × 4 = 216MHz

2. fcmp2
   Phase Comparison Frequency2: 27MHz MDIV = 2
   fcmp2 = 27MHz / 2 = 13.5MHz

3. NDIV2
   Feedback Dividing Value: NDIV2 = fVCO2 / fcmp2 = 216 / 13.5 = 16
   N_{INT2} = round [216 / 13.5] = round [16] = 16
   N_{INT2} = 16, N_{FRAC2} = 0

   N_{FRAC2} = N_{NUME} / N_{DENO} = 0
   Output Frequency Error: 0ppm

Example2) input frequency = 27MHz, output frequency = 24.576MHz

1. fVCO2
   VCO2 Frequency: 221.184MHz ODIV = 9
   fVCO2 = 24.576MHz × 9 = 221.184MHz

2. fcmp2
   Phase Comparison Frequency2: 27MHz MDIV = 2
   fcmp2 = 27MHz / 2 = 13.5MHz

3. NDIV2
   Feedback Dividing Value: NDIV2 = fVCO2 / fcmp2 = 221.184 / 13.5 = 16.384
   N_{INT2} = round [221.184 / 13.5] = round [16.384] = 16
   N_{INT2} = 16, N_{FRAC2} = 0.384

   When min [abs [(round [0.384 × 125]) / 125) – 0.384]]
   $NDENO_{OPTIMUM}$ = 125
   $NUME_{OPTIMUM}$ = round [0.384 × 125] = 48

   N_{FRAC} = N_{NUME} / N_{DENO} = 48 / 125 = 0.384
   Output Frequency Error: 0ppm

Programmable control setting

AK8140A has programmable control settings which can be controlled by “Serial programming interface mode (refer to page. 26)” and “Programmable control pin mode (refer to page. 29)”. In the default setting, programmable control settings can be controlled by “Serial programming interface mode”. “Programmable control pin mode” is selected when SPICON bit = SPICON_SET bit = ‘1’.

Eight user-definable configurations are shown in following table by setting registers for address : 04h ~ 0Bh, 20h, 30h. These settings can be controlled by S0, S1, and S2 which are register setting or external control pins.

They can be programmed to any of the following functions:

- PLL1/2 frequency:
  select from two variation of fVCO frequency set by the applicable register.

- CLK1-4 output state:
  select from four states: enable/Hi-z/disable to L/ disable to H.

Table 1. Programmable Control Setting by S[2:0]

Programmable Control			PLL1 frequency	PLL2 frequency	Output State			
S2	S1	S0			CLK1	CLK2	CLK3	CLK4
0	0	0	FS1_0	FS2_0	CLK1_0[1:0]	CLK2_0[1:0]	CLK3_0[1:0]	CLK4_0[1:0]
0	0	1	FS1_1	FS2_1	CLK1_1[1:0]	CLK2_1[1:0]	CLK3_1[1:0]	CLK4_1[1:0]
0	1	0	FS1_2	FS2_2	CLK1_2[1:0]	CLK2_2[1:0]	CLK3_2[1:0]	CLK4_2[1:0]
0	1	1	FS1_3	FS2_3	CLK1_3[1:0]	CLK2_3[1:0]	CLK3_3[1:0]	CLK4_3[1:0]
1	0	0	FS1_4	FS2_4	CLK1_4[1:0]	CLK2_4[1:0]	CLK3_4[1:0]	CLK4_4[1:0]
1	0	1	FS1_5	FS2_5	CLK1_5[1:0]	CLK2_5[1:0]	CLK3_5[1:0]	CLK4_5[1:0]
1	1	0	FS1_6	FS2_6	CLK1_6[1:0]	CLK2_6[1:0]	CLK3_6[1:0]	CLK4_6[1:0]
1	1	1	FS1_7	FS2_7	CLK1_7[1:0]	CLK2_7[1:0]	CLK3_7[1:0]	CLK4_7[1:0]
Address			20h	30h	04h, 05h	06h, 07h	08h, 09h	0Ah, 0Bh

The output frequency of PLL1 is chosen from two setups, PLL1_0 or PLL1_1.

Table 2. PLL1 Output Frequency Selection (Address: 20h)

FS1_x	PLL1 Frequency
0	PLL1_0 Predefined by address: 21h, 22h ~ 26h (Default)
1	PLL1_1 Predefined by address: 21h, 27h ~ 2Bh

(x=0-7)

The output frequency of PLL2 is chosen from two setups, PLL2_0 or PLL2_1.

Table 3. PLL2 Output Frequency Selection (Address: 30h)

FS2_x	PLL2 Frequency
0	PLL2_0 Predefined by address: 31h ~ 34h (Default)
1	PLL2_1 Predefined by address: 35h ~ 38h

(x = 0-7)

CLKn_x [1:0] bit set output state(CLKn_x) defined in the Table 1. on page 18 can be set up.

Table 4. CLK1-4 Output State Definition (Address: 04h ~ 0Bh)

CLKn_x [1:0]	CLKn Output State
00	CLK Enabled (Default)
01	Disable to Low
10	Disable to High
11	Disable to Hi-z

(n = 1-4, x = 0-7)

Power up sequence

Step1 : Supplying proper voltage to the power pins with PD_N pin = 'L'.
*Note: VDD1-4 must be supplied simultaneously.
The assumption power start time to reach 90 % of VDD is within 20 ms.
Step2 : Set the PD_N pin to 'H' 1 μs after the point that the power supply reaches 90% of VDD.
Step3 : SCL / SDA are acceptable min 2ms later.

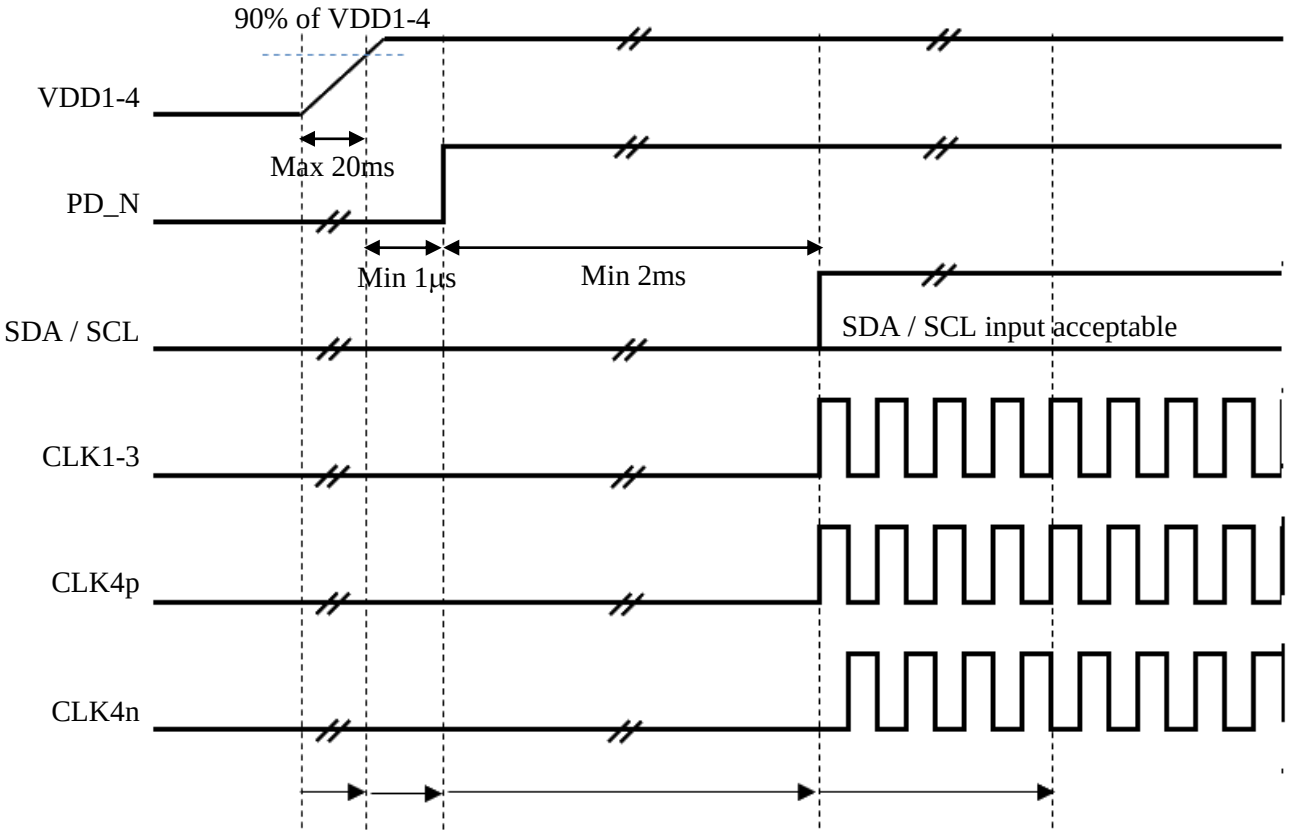


Figure 7. Power up sequence

Serial interface

Read/Write performance of serial interface is explained as below. The device address of AK8140A is Device Address#1:1100, Device Address#2:1 A1 0. A1 is set by the register 'SLV_ADD1' bit (Address: 03h).

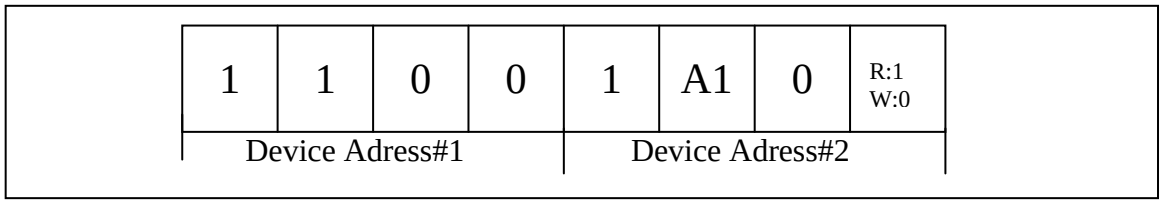


Figure 8. The Device Address of AK8140A

Write operation

Write operation is described below. Data must be sent after sending 8 bits address and receiving ACK. It is possible to write next address sequentially by sending next data instead of stop condition.
The address which is written after "13h/2Bh/38h" becomes "00h/20h/30h".

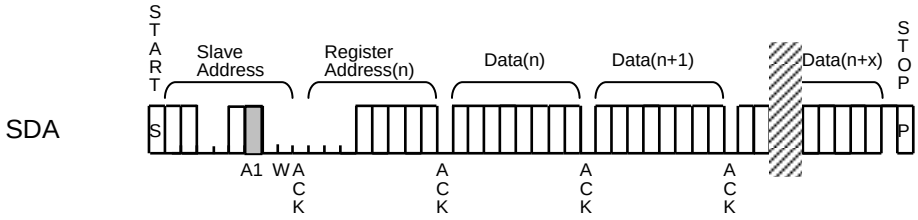


Figure 9. Write operation

Current address read

Current address read operation is described below. The data that is read by this operation is obtained as "last accessed address + 1". Therefore, it is consequent to return "13h/2Bh/38h" after accessing the address "00h/20h/30h".

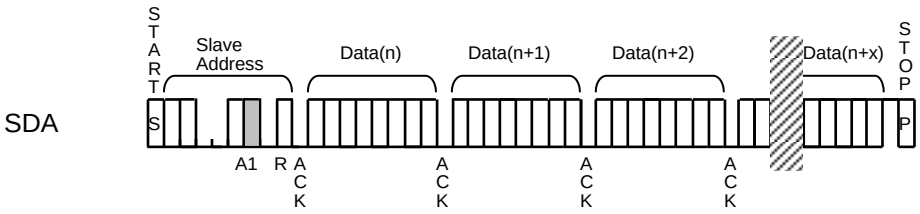


Figure 10. Current address read

Random read

Random read operation is described below. It is necessary to operate “dummy write” before sending read command. Dummy write is to send the address to read. It is possible to read next address sequentially by sending ACK instead of stop condition.

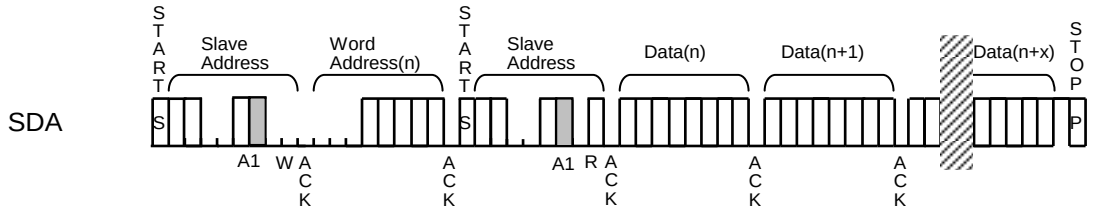


Figure 11. Random read

Change data

Change data operation is described below. It is available when SCL is Low.

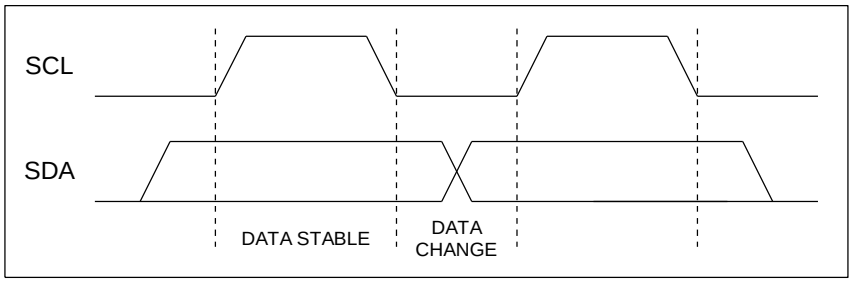


Figure 12. Change data

Start / Stop timing

Start / Stop timing is described below. The sequence is started when SDA goes from high to low during SCL is high. The sequence is stopped when SDA goes from low to high during SCL is high.

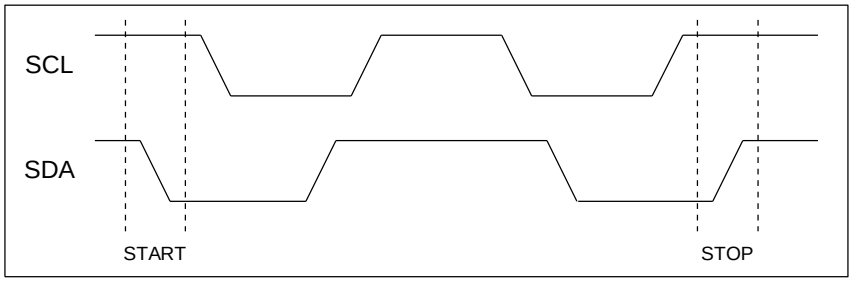


Figure 13. Start / Stop timing

Register Configuration

AK8140A has Register can be programmed via the serial SDA/SCL interface.
The following table and explanations describe the programmable functions of AK8140A.

- Default register state is all '0'.
  The default setting appears after power is supplied or after power-down/up sequence until it is reprogrammed to a different setting.

- All data transferred with the MSB first.

- When a Certain Setting is set by three Address, write the data to all Address.
  22h ~ 24h, 27h ~ 29h, 32h ~ 34h, 36h ~ 38h
  FRACn[17:0] settings are updated after writing register 24h / 29h.
  Setting procedure should be (1)22h / 27h , (2)23h / 28h, and then (3)24h / 29h.

  NDIV2 Dividing Value settings are updated after writing register 34h / 38h.
  Setting procedure should be (1)32h / 36h , (2)33h / 37h, and then (3)34h / 38h.

- Write '0' to Reserved bits.

- **The AK8140A prohibits to write '1' to address 16h ~ 1Fh, 2Ch ~ 2Fh and 39h ~ FFh.**

Table 5. AK8140A Register Configuration

Address	Register	Remarks	Page
00h to 13h	Generic Configuration Register	**Device Setting** · Device Setting (S0/S1/S2) for Serial Programming mode · Device Input clock (Crystal or Ext-in) · Slave Address A1 **CLK1 to 4 Setting** · CLK1 to 4 Output State （CLK enabled / Disabled to L / Disabled to H / Hi-Z） · MUX1 to 4 (PLL1 fVCO1/ PLL2 fVCO2 / Input Bypass) · ODIV1 to 4 Parameter · CLK1 to 4 Output Buffer Drivability · CLK4 Output Interface LVDS or CMOS	**p. 24 to p. 34**
14h to 15h	Reserved Bits	Reserved Bits	**p. 35**
20h to 2Bh	PLL1 Configuration Register	**PLL1 Setting** （Input CLK for PLL1, MDIV1, NDIV1, fVCO1 range）	**p. 36 to p. 42**
30h to 38h	PLL2 Configuration Register	**PLL2 Setting** （MDIV2, NDIV2, fVCO2 range）	**p. 43 to p. 47**

Generic Configuration Register (Address: 00h ~ 13h)

Addr	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
00h	Reserved	Reserved	Reserved	Reserved	Reserved	S[2]	S[1]	S[0]	Device Control Setting for SDA/SCL Mode
	0	0	0	0	0	0	0	0	
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	0	0	0	0	0	0	0	0	
02h	RID[1]	RID[0]	OSC_DIS	Reserved	R / W	R / W	R / W	R / W	Device Overall Setting
	0	0	0	0	0	0	0	0	
03h	Reserved	Reserved	PWDN	SLV _ADD1	Reserved	CLK4 _CMOS	SPICON	SPICON _SET	
	0	0	0	0	0	0	0	0	
04h	CLK1_0 [1]	CLK1_0 [0]	CLK1_1 [1]	CLK1_1 [0]	CLK1_2 [1]	CLK1_2 [0]	CLK1_3 [1]	CLK1_3 [0]	CLK1 Output State Setting
	0	0	0	0	0	0	0	0	
05h	CLK1_4 [1]	CLK1_4 [0]	CLK1_5 [1]	CLK1_5 [0]	CLK1_6 [1]	CLK1_6 [0]	CLK1_7 [1]	CLK1_7 [0]	
	0	0	0	0	0	0	0	0	
06h	CLK2_0 [1]	CLK2_0 [0]	CLK2_1 [1]	CLK2_1 [0]	CLK2_2 [1]	CLK2_2 [0]	CLK2_3 [1]	CLK2_3 [0]	CLK2 Output State Setting
	0	0	0	0	0	0	0	0	
07h	CLK2_4 [1]	CLK2_4 [0]	CLK2_5 [1]	CLK2_5 [0]	CLK2_6 [1]	CLK2_6 [0]	CLK2_7 [1]	CLK2_7 [0]	
	0	0	0	0	0	0	0	0	
08h	CLK3_0 [1]	CLK3_0 [0]	CLK3_1 [1]	CLK3_1 [0]	CLK3_2 [1]	CLK3_2 [0]	CLK3_3 [1]	CLK3_3 [0]	CLK3 Output State Setting
	0	0	0	0	0	0	0	0	
09h	CLK3_4 [1]	CLK3_4 [0]	CLK3_5 [1]	CLK3_5 [0]	CLK3_6 [1]	CLK3_6 [0]	CLK3_7 [1]	CLK3_7 [0]	
	0	0	0	0	0	0	0	0	
0Ah	CLK4_0 [1]	CLK4_0 [0]	CLK4_1 [1]	CLK4_1 [0]	CLK4_2 [1]	CLK4_2 [0]	CLK4_3 [1]	CLK4_3 [0]	CLK4 Output State Setting
	0	0	0	0	0	0	0	0	
0Bh	CLK4_4 [1]	CLK4_4 [0]	CLK4_5 [1]	CLK4_5 [0]	CLK4_6 [1]	CLK4_6 [0]	CLK4_7 [1]	CLK4_7 [0]	
	0	0	0	0	0	0	0	0	
0Ch	MUX1[1]	MUX1[0]	MUX2[1]	MUX2[0]	MUX3[1]	MUX3[0]	MUX4[1]	MUX4[0]	MUX1-4 Selection
	0	0	0	0	0	0	0	0	

Addr	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
0Dh	Reserved	Reserved	Reserved	Reserved	CLK1 MOD	DIV2_ BYPASS1	ODIV_1 [9]	ODIV_1 [8]	Output Buffer1 Drivability
	0	0	0	0	0	0	0	0	
0Eh	ODIV_1 [7]	ODIV_1 [6]	ODIV_1 [5]	ODIV_1 [4]	ODIV_1 [3]	ODIV_1 [2]	ODIV_1 [1]	ODIV_1 [0]	ODIV1 Setting
	0	0	0	0	0	0	0	0	
0Fh	Reserved	Reserved	CLK3 MOD	CLK2 MOD	DIV2_ BYPASS3	DIV2_ BYPASS2	ODIV_2 [9]	ODIV_2 [8]	Output Buffer2/3 Drivability
	0	0	0	0	0	0	0	0	
10h	ODIV_2 [7]	ODIV_2 [6]	ODIV_2 [5]	ODIV_2 [4]	ODIV_2 [3]	ODIV_2 [2]	ODIV_2 [1]	ODIV_1 [0]	ODIV2 Setting
	0	0	0	0	0	0	0	0	
11h	ODIV_3 [7]	ODIV_3 [6]	ODIV_3 [5]	ODIV_3 [4]	ODIV_3 [3]	ODIV_3 [2]	ODIV_3 [1]	ODIV_3 [0]	ODIV3 Setting
	0	0	0	0	0	0	0	0	
12h	Reserved	Reserved	Reserved	Reserved	CLK4 MOD	DIV2_ BYPASS4	ODIV_4 [9]	ODIV_4 [8]	Output Buffer4 Drivability
	0	0	0	0	0	0	0	0	
13h	ODIV_4 [7]	ODIV_4 [6]	ODIV_4 [5]	ODIV_4 [4]	ODIV_4 [3]	ODIV_4 [2]	ODIV_4 [1]	ODIV_4 [0]	ODIV4 Setting
	0	0	0	0	0	0	0	0	

Generic Configuration Register

Address: 00h Device Control Setting for Serial Programming Mode*
*Valid only when Serial Programming Mode (Address: 03h SPICON = "0")

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reserved	Reserved	Reserved	Reserved	Reserved	S[2]	S[1]	S[0]

S[2:0]: Device Control Setting for Serial Programming Mode

When SPICON bit is set to "0", pin23 / 24 has SDA / SCL function and S[2:0] bits select the Device Control Setting predefined as the Table 1. on page 18.

Table 6. S[2:0]: Device Control Setting for Serial Programming Mode

S[2:0]	Device Control Setting (see on page 18)
000	[S2:S0]=000 (Default)
001	[S2:S0]=001
010	[S2:S0]=010
011	[S2:S0]=011
100	[S2:S0]=100
101	[S2:S0]=101
110	[S2:S0]=110
111	[S2:S0]=111

Address: 01h Reserved

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Address: 02h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
02h	RID[1]*	RID[0]*	OSC_DIS	Reserved	R / W	R / W	R / W	R / W

RID[1:0]: Device Identification *read only

Table 7. RID[1:0]: Device Identification

RID[1:0]	Device Identification
00	AK8140A (Default)
01	
10	
11	

OSC_DIS: Crystal Oscillator Circuit Enable/Disable Setting (MUX0)

Set the register followed by clock source, as explained in the following table.

Table 8. OSC_DIS: Crystal Oscillator Circuit Enable/Disable Setting

OSC_DIS	Crystal Oscillator Circuit State
0	Enable (Crystal Connection) (Default)
1	Disable (Ext-in : External Clock Signal Input)

R/W: User arbitrarily programmable bits (D3 ~ D0)

User can freely program these bits if necessary.

Address: 03h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
03h	Reserved	Reserved	PWDN	SLV _ADD1	Reserved	CLK4 _CMOS	SPICON	SPICON _SET

PWDN: Device Power Down control

When set PWDN bit to "1", only PLL1/2, ODIVn and Output Buffers is powered down. Register settings are unchanged.
CLKn output state is followed by CLKn output state selection (Address: 04h ~ 0Bh, CLKn_x[1:0]) when the device is powered down by this bit. *1

Table 9. PWDN: Device Power Down control

PWDN	Device Setting
0	Device Active (Default)
1	Device Powered down*1

*1 It becomes CLKn = 'L', when CLKn output state is set to CLKn_x[1:0] = "00" as "CLK enabled".

SLV_ADD1: Slave Address Bits A1 Selection

SLV_ADD1 sets the A1 of the Slave Receiver Address.
The default setting SLV_ADD1= '0' appears after power is supplied or after power-down/up sequence until it is reprogrammed to a different setting.
See page 21 for more information about Slave Address setting.

Table 10. SLV_ADD1: Slave Address Bits A1 Selection

SLV_ADD1	Device Setting
0	A1 of Slave Address : 0 (Default)
1	A1 of Slave Address : 1

CLK4_CMOS: CLK4 Output Interface Selection LVDS/CMOS

CLK4_CMOS bit sets CLK4 output Interface, LVDS or LVCMOS.

Table 11. CLK4_CMOS: CLK4 Output Interface Selection LVDS/CMOS

CLK4_CMOS	CLK4 Output Setting
0	LVDS output (Default)
1	LVCMOS output

SPICON: Operation mode selection for pin 23/24

SPICON bit selects the operational mode of a dual functional pin 23/24.
When SPICON = “1”, pin 23/24 become S1/S2 pin for “Programmable Control pin”. The setup of SPICON = "1" becomes effective by writing ’1’ to “SPICON_SET” bit additionally, and impossible to use it as “Serial programming interface”. However, Once pin 23/24 play the role of S1/S2 pin, S1/S2 pin can be temporarily used as SDA/SCL pin for “Serial programming interface” to change the register setting by shorting VDDO1 to VSS.
The user can predefine up to eight device control settings by setting registers for address: 04h ~ 0Bh, 20h, 30h. These settings then can be selected by the external control pins, S0, S1, and S2.

Table 12. SPICON: Operation mode selection for pin 23/24

SPICON	Pin 23/24 operation
0	Serial programming interface*1 (Default) Pin 23:SDA Pin 24:SCL
1	Programmable control pin*2 Pin 23:S2 Pin 24:S1

*1 Address：00h becomes effective.
*2 S0/S1/S2 pin can control the Device Setting defined in the table on page 18.

SPICON_SET: SPICON Validation

“SPICON_SET” validates a setup of “SPICON” bit.
A setup written in SPICON by writing ‘1’ in this bit becomes effective.
When Set “SPICON_SET” = ‘1’, “SPICON_SET” bit should be written last.

Table 13. SPICON_SET: SPICON Validation

SPICON_SET	SPICON Setting
0	- (Default)
1	SPICON bit is Effective *1

*1 “SPICON_SET” bit should be written last.
Setup of “SPICON” bit is validated by the rising edge of a “SPICON_SET” bit.

Address: 04h ~ 0Bh

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
04h	CLK1_0 [1]	CLK1_0 [0]	CLK1_1 [1]	CLK1_1 [0]	CLK1_2 [1]	CLK1_2 [0]	CLK1_3 [1]	CLK1_3 [0]
05h	CLK1_4 [1]	CLK1_4 [0]	CLK1_5 [1]	CLK1_5 [0]	CLK1_6 [1]	CLK1_6 [0]	CLK1_7 [1]	CLK1_7 [0]
06h	CLK2_0 [1]	CLK2_0 [0]	CLK2_1 [1]	CLK2_1 [0]	CLK2_2 [1]	CLK2_2 [0]	CLK2_3 [1]	CLK2_3 [0]
07h	CLK2_4 [1]	CLK2_4 [0]	CLK2_5 [1]	CLK2_5 [0]	CLK2_6 [1]	CLK2_6 [0]	CLK2_7 [1]	CLK2_7 [0]
08h	CLK3_0 [1]	CLK3_0 [0]	CLK3_1 [1]	CLK3_1 [0]	CLK3_2 [1]	CLK3_2 [0]	CLK3_3 [1]	CLK3_3 [0]
09h	CLK3_4 [1]	CLK3_4 [0]	CLK3_5 [1]	CLK3_5 [0]	CLK3_6 [1]	CLK3_6 [0]	CLK3_7 [1]	CLK3_7 [0]
0Ah	CLK4_0 [1]	CLK4_0 [0]	CLK4_1 [1]	CLK4_1 [0]	CLK4_2 [1]	CLK4_2 [0]	CLK4_3 [1]	CLK4_3 [0]
0Bh	CLK4_4 [1]	CLK4_4 [0]	CLK4_5 [1]	CLK4_5 [0]	CLK4_6 [1]	CLK4_6 [0]	CLK4_7 [1]	CLK4_7 [0]

CLKn_x[1:0] : CLK1-4 Output State Definition

CLKn_x[1:0] bit set output state (CLKn_x) defined in the Table 1. on page 18 can be set up.

ODIVn function is stopped, when CLKn state is set to Disable (CLKn_x[1:0] = “01” / “10” / “11”).
When CLK4 state is set to Disable, CLK4p/4n each pin will be the following state.
CLK4_x[1:0] = “01” / “10” / “11” : CLK4p / 4n = ‘L’ / ‘L’, ‘H’ / ‘H’, ‘Hi-Z’ / ‘Hi-Z’

Table 14. CLK1-4 Output State Definition

CLKn_x[1:0]	CLKn Output State
00	CLK Enabled (Default)
01	Disable to Low
10	Disable to High
11	Disable to Hi-z

(n = 1-4, x = 0-7)

Address: 0Ch

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	MUX1[1]	MUX1[0]	MUX2[1]	MUX2[0]	MUX3[1]	MUX3[0]	MUX4[1]	MUX4[0]

MUXn[1:0]: CLK1-4 Output Clock Source Selection

Select Output Clock Signal Source of CLK1-4.

Table 15. CLK1-4 Output Clock Source Selection

MUXn[1:0]	CLKn Output Clock Source
00	"L" Output (Default)
01	Input Bypass
10	PLL1 output (fvco1)
11	PLL2 output (fvco2)

(n = 1-4)

Address: 0Dh ~ 13h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	Reserved	Reserved	Reserved	Reserved	CLK1 MOD	DIV2_ BYPASS1	ODIV_1 [9]	ODIV_1 [8]
0Eh	ODIV_1 [7]	ODIV_1 [6]	ODIV_1 [5]	ODIV_1 [4]	ODIV_1 [3]	ODIV_1 [2]	ODIV_1 [1]	ODIV_1 [0]
0Fh	Reserved	Reserved	CLK3 MOD	CLK2 MOD	DIV2_ BYPASS3	DIV2_ BYPASS2	ODIV_2 [9]	ODIV_2 [8]
10h	ODIV_2 [7]	ODIV_2 [6]	ODIV_2 [5]	ODIV_2 [4]	ODIV_2 [3]	ODIV_2 [2]	ODIV_2 [1]	ODIV_2 [0]
11h	ODIV_3 [7]	ODIV_3 [6]	ODIV_3 [5]	ODIV_3 [4]	ODIV_3 [3]	ODIV_3 [2]	ODIV_3 [1]	ODIV_3 [0]
12h	Reserved	Reserved	Reserved	Reserved	CLK4 MOD	DIV2_ BYPASS4	ODIV_4 [9]	ODIV_4 [8]
13h	ODIV_4 [7]	ODIV_4 [6]	ODIV_4 [5]	ODIV_4 [4]	ODIV_4 [3]	ODIV_4 [2]	ODIV_4 [1]	ODIV_4 [0]

ODIVn Dividing Value Setting (ODIV_n / DIV2_BYPASSn)

The Dividing value of ODIVn is decided by “Frequency setting procedure” on page 14.

(1) The case ODIVn divides the clock signal of Input Bypass. (MUXn = “01”)

Set ODIVn dividing value according to explanation below, when ODIVn divides a clock signal of Input Bypass.
ODIVn configuration is as the following Figure. ODIVn is calculated number by “Frequency setting procedure” on page 14.

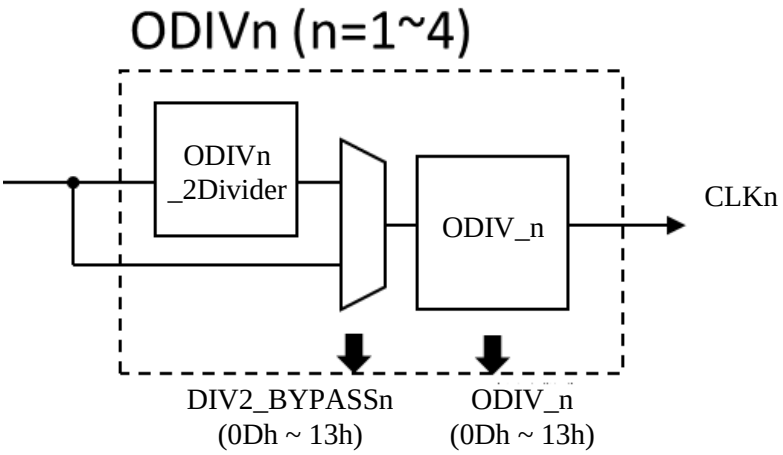


Figure 14. ODIVn configuration

When set ODIVn dividing Value = 2 or odd number:
→ Bypass ODIVn_2 Divider, ODIV_n is the same number as ODIVn

Example1: ODIVn = 3
Bypass ODIVn_2 Divider (DIV2_BYPASSn = '1')
ODIV_n = ODIVn = 3

When set ODIVn dividing Value even number beyond 4:
→ Using ODIVn_2 Divider, ODIV_n = ODIVn / 2

Example1: ODIVn = 10
Using ODIVn_2 Divider (DIV2_BYPASSn = "0")
ODIV_n = ODIVn / 2 = 5

(2) The case ODIVn divides clock signal of PLL1 or PLL2 (MUXn = "10" or "11")

Set ODIVn dividing value according to explanation below, when ODIVn divides clock signal of PLL1 or PLL2

When ODIVn divides fvco1 (MUXn = "10"):
→ ODIVn = ODIVn (calculated value) / 2

When ODIVn divides fvco2 (MUXn = "11"):
→ ODIVn = ODIVn (calculated value)

ODIV_n[9:0]: ODIV_n dividing value Control (n = 1, 2, 4)

Set ODIV_n (n = 1, 2, 4) dividing value of ODIV1, 2, 4 as blow.

Table 16. ODIV_n dividing value Control (n = 1, 2, 4)

ODIV_n[9:0] (n=1,2,4)	Dividing Value
00 0000 0000	1 (Default)
00 0000 0001	2
00 0000 0010	3
:	:
11 1111 1111	1024

ODIV_3[7:0]: ODIV_3 dividing value Control

Set ODIV_3 dividing value of ODIV3 as blow

Table 17. ODIV_3 dividing value Control

ODIV_3[7:0]	Dividing Value
0000 0000	1 (Default)
0000 0001	2
0000 0010	3
:	:
1111 1111	256

DIV2_BYPASSn (n = 1-4)

DIV2_BYPASSn selects whether ODIVn_2divider used. (n = 1-4)

Table 18. DIV2_BYPASSn (n = 1-4)

DIV2_BYPASSn	ODIVn_2Divider
0	Use the 2divider (Default)
1	Bypass the 2 divider

Effective only when MUXn (n = 1-4) = “00” / “01”

CLKnMOD: CLKn (n = 1-3) Output Buffer Drivability Setting

“CLKnMOD” set the drivability of Output Buffer of CLKn as the following table. (n = 1-3)

Table 19. CLKn (n = 1-3) Output Buffer Drivability Setting

CLKnMOD	CLKn Drivability
0	High when VDDO1, 2 = 1.8V (Default)
1	Low when VDDO1, 2 = 3.3V

(n = 1-3)

CLK4MOD: CLK4 Output Buffer Drivability Setting

“CLK4MOD” set the drivability of Output Buffer of CLK4 as the following table.

Table 20. CLK4 Output Buffer Drivability Setting

CLK4MOD	CLK4 Drivability
0	High when VDDO2=1.8V (Default)
1	Low when VDDO2=3.3V

Reserved Bits (Address: 14h ~ 15h)

Addr	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
14h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	0	0	0	0	0	0	0	0	
15h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
	0	0	0	0	0	0	0	0	

Reserved Bits

Address: 14h ~ 15h Reserved Bits

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
14h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
15h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

・Write ‘0’ to Reserved bits.

PLL1 Configuration Register (Address: 20h ~ 2Bh)

Addr	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
20h	FS1_0	FS1_1	FS1_2	FS1_3	FS1_4	FS1_5	FS1_6	FS1_7	PLL1 Frequency Selection
	0	0	0	0	0	0	0	0	
21h	INPUT _CK1	VCO1_ RANGE0 [1]	VCO1_ RANGE0 [0]	VCO1_ RANGE1 [1]	VCO1_ RANGE1 [0]	Reserved	Reserved	Reserved	PLL1 Input Clock Selection fVCO1_ Range
	0	0	0	0	0	0	0	0	
22h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC0 [17]	FRAC0 [16]	PLL1_0 NDIV1 Fractional Part Setting
	0	0	0	0	0	0	0	0	
23h	FRAC0 [15]	FRAC0 [14]	FRAC0 [13]	FRAC0 [12]	FRAC0 [11]	FRAC0 [10]	FRAC0 [9]	FRAC0 [8]	
	0	0	0	0	0	0	0	0	
24h	FRAC0 [7]	FRAC0 [6]	FRAC0 [5]	FRAC0 [4]	FRAC0 [3]	FRAC0 [2]	FRAC0 [1]	FRAC0 [0]	
	0	0	0	0	0	0	0	0	
25h	Reserved	INT0[6]	INT0[5]	INT0[4]	INT0[3]	INT0[2]	INT0[1]	INT0[0]	PLL1_0 NDIV1 Integral Part Setting
	0	0	0	0	0	0	0	0	
26h	MDIVC0 [3]	MDIVC0 [2]	MDIVC0 [1]	MDIVC0 [0]	MDIVP0 [3]	MDIVP0 [2]	MDIVP0 [1]	MDIVP0 [0]	PLL1_0 MDIV1 Setting
	0	0	0	0	0	0	0	0	
27h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC1 [17]	FRAC1 [16]	PLL1_1 NDIV1 Fractional Part Setting
	0	0	0	0	0	0	0	0	
28h	FRAC1 [15]	FRAC1 [14]	FRAC1 [13]	FRAC1 [12]	FRAC1 [11]	FRAC1 [10]	FRAC1 [9]	FRAC1 [8]	
	0	0	0	0	0	0	0	0	
29h	FRAC1 [7]	FRAC1 [6]	FRAC1 [5]	FRAC1 [4]	FRAC1 [3]	FRAC1 [2]	FRAC1 [1]	FRAC1 [0]	
	0	0	0	0	0	0	0	0	
2Ah	Reserved	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]	PLL1_1 NDIV1 Integral Part Setting
	0	0	0	0	0	0	0	0	
2Bh	MDIVC1 [3]	MDIVC1 [2]	MDIVC1 [1]	MDIVC1 [0]	MDIVP1 [3]	MDIVP1 [2]	MDIVP1 [1]	MDIVP1 [0]	PLL1_1 MDIV1 Setting
	0	0	0	0	0	0	0	0	

PLL1 Configuration Register

PLL1 Block Diagram is as the following Figure.
Set PLL1 parameter according to Frequency Setting Procedure on page 14.
PLL1 has two Frequency mode predefined as PLL1_0 or PLL1_1 and selected by S[2:0] bits (Address: 00h) or S0/S1/S2 pin.
Refer to Programmable Control pin setting on page 18 for more information about Frequency selection.

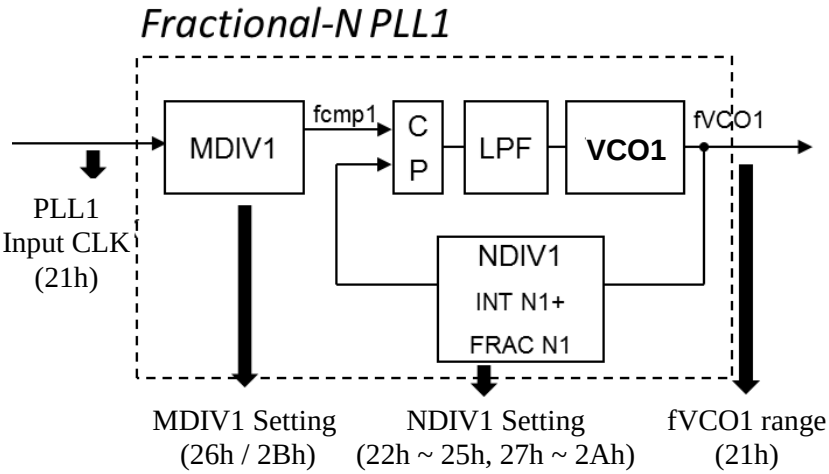


Figure 15. PLL1 Block Diagram

Address: 20h PLL1 Output Frequency selection

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	FS1_0	FS1_1	FS1_2	FS1_3	FS1_4	FS1_5	FS1_6	FS1_7

FS1_x (x = 0-7): PLL1 Output Frequency selection

The output frequency of PLL1 is chosen from two setups, PLL1_0 and PLL1_1.

Table 21. PLL1 Output Frequency selection

FS1_x	PLL1 Frequency
0	PLL1_0 Predefined by address:21h, 22h ~ 26h (Default)
1	PLL1_1 Predefined by address:21h, 27h ~ 2Bh

(x=0-7)

Address: 21h PLL1 Input Clock Selection / fVCO1 range

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
21h	INPUT_CK1	VCO1_RANGE0 [1]	VCO1_RANGE0 [0]	VCO1_RANGE1 [1]	VCO1_RANGE1 [0]	Reserved	Reserved	Reserved

INPUT_CK1: PLL1Input Clock Selection (MUX5)

Table 22. PLL1Input Clock Selection (MUX5)

INPUT_CK1	PLL1Input Clock
0	Input Clock (Crystal Oscillation or External Clock Signal Input) (Default)
1	fvco2 PLL2 output clock

VCO1_RANGEn[1:0]: fVCO1 range selection (n = 0, 1)

"VCO1_RANGEn[1:0]" selects the fVCO1 frequency range. fVCO1 frequency can be set according to Frequency Setting Procedure on page 14.

Table 23. fVCO1 range selection (n = 0, 1)

VCO1_RANGEn[1:0]	fVCO1 range
00	fVCO1 < 300MHz (Default)
01	300MHz ≤ fvco1 < 370MHz
10	370MHz ≤ fvco1
11	370MHz ≤ fvco1

Address: 22h ~ 24h, 27h ~ 29h NDIV1 fractional part setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
22h 27h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRACn [17]	FRACn [16]
23h 28h	FRACn [15]	FRACn [14]	FRACn [13]	FRACn [12]	FRACn [11]	FRACn [10]	FRACn [9]	FRACn [8]
24h 29h	FRACn [7]	FRACn [6]	FRACn [5]	FRACn [4]	FRACn [3]	FRACn [2]	FRACn [1]	FRACn [0]

(n = 0, 1)

FRACn [17:0] : NDIV1 fractional part setting (n = 0, 1)

When a Certain Setting is set by three Address, write the data to all Address.
FRACn[17:0] settings are updated after writing register 24h / 29h.
Setting procedure should be (1)22h / 27h , (2)23h / 28h, and then (3)24h / 29h.

NDIV1 fractional part can be set according to Frequency Setting Procedure on page 14.
Fractional part of N is expressed by $A/2^{18}$. Here, the numerator A is defined by FRAC bits. FRAC is treated as 2's Complement which is able to set from -2^{17} up to $+2^{17}$. Consequently, it is possible to set from -0.5 to +0.5 for fractional part of N.

Table 24. NDIV1 fractional part setting (n = 0, 1)

FRACn [17:0]	A	Fractional Part
01 1111 1111 1111 1111	+131071	0.49999619..
01 1111 1111 1111 1110	+131070	0.49999237..
: 01 0000 0000 0000 0000 :	: +65536 :	: 0.25 :
00 0000 0000 0000 0001	+1	0.00000381..
00 0000 0000 0000 0000	0 (Default)	0 (Default)
11 1111 1111 1111 1111	-1	-0.00000381..
11 1111 1111 1111 1110	-2	
: 11 0000 0000 0000 0000 :	: -65536 :	: -0.25 :
10 0000 0000 0000 0001	-131071	-0.49999619..
10 0000 0000 0000 0000	-131072	-0.5

Address: 25h / 2Ah NDIV1 integral part settings

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
25h 2Ah	Reserved	INTn[6]	INTn[5]	INTn[4]	INTn[3]	INTn[2]	INTn[1]	INTn[0]

(n = 0, 1)

INTn [6:0]: NDIV1 integral part setting (n = 0, 1)

NDIV1 Integral part can be set according to Frequency Setting Procedure on page 14.
INTn[6:0] must be set from “0010001” to “1000100”, when PLL1 is used.

Table 25. NDIV1 integral part setting (n = 0, 1)

INTn [6:0]	integral part
000 0000	(Default)
000 0001 ~ 001 0000	Prohibited
001 0001	17
001 0010	18
:	:
100 0011	67
100 0100	68
100 0101 ~ 111 1111	Prohibited

Address: 26h / 2B MDIV1 Setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
26h 2Bh	MDIVCn [3]	MDIVCn [2]	MDIVCn [1]	MDIVCn [0]	MDIVPn [3]	MDIVPn [2]	MDIVPn [1]	MDIVPn [0]

(n = 0, 1)

MDIV1 Dividing Value Settings (MDIVCn, MDIVPn)
MDIV1Configuration is as the following Figure.
MDIV1 Dividing Value can be set according to Frequency Setting Procedure on page 14.

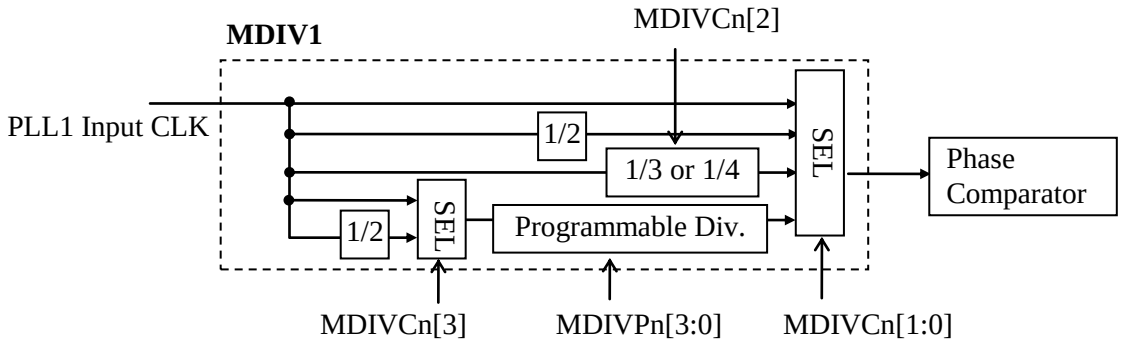


Figure 16. MDIV1 Configuration

MDIVCn[3]: Programmable divider input selection (n = 0, 1)

Table 26. Programmable divider input selection (n = 0, 1)

MDIVCn[3]	Input of Programmable divide
0	PLL1 Input CLK (Default)
1	PLL1 Input CLK 1/2

MDIVCn[2]: 3 or 4 divider selection (n = 0, 1)

Table 27. 3 or 4 divider selection (n = 0, 1)

MDIVCn[2]	Selected divider
0	3 divider (Default)
1	4 divider

MDIVCn[1:0]: Input of Phase comparator selection (n = 0, 1)

Set MDIVCn[1:0] = "11", when INPUT_CK1 is set to "1" (Address = 21h).

Table 28. Input of Phase comparator selection (n = 0, 1)

MDIVCn[1:0]	Input of Phase comparator
0 0	PLL1 Input CLK (Default)
0 1	PLL1 Input CLK 1/2
1 0	3 or4 divider output
1 1	Programmable divider Output

MDIVPn[3:0]: Programmable divider control (n = 0, 1)

MDIVPn[3:0] must be set from "0001" to "1111", when PLL1 is used.

Table 29. MDIVPn Programmable divider control (n = 0, 1)

MDIVPn[3:0]	Programmable Divider dividing value
0 0 0 0	(Default)
0 0 0 1	2
0 0 1 0	3
0 0 1 1	4
0 1 0 0	5
0 1 0 1	6
0 1 1 0	7
0 1 1 1	8
1 0 0 0	9
1 0 0 1	10
1 0 1 0	11
1 0 1 1	12
1 1 0 0	13
1 1 0 1	14
1 1 1 0	15
1 1 1 1	16

PLL2 Configuration Register (Address: 30h ~ 38h)

Addr	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
30h	FS2_0	FS2_1	FS2_2	FS2_3	FS2_4	FS2_5	FS2_6	FS2_7	PLL2 Frequency Selection
	0	0	0	0	0	0	0	0	
31h	Reserved	Reserved	MDIV0[2]	MDIV0[1]	MDIV0[0]	VCO2_ RANGE0 [1]	VCO2_ RANGE0 [0]	Reserved	PLL2_0 MDIV2 Setting
	0	0	0	0	0	0	0	0	fVCO2_ Range0
32h	NINT0 [5]	NINT0 [4]	NINT0 [3]	NINT0 [2]	NINT0 [1]	NINT0 [0]	NUME0 [8]	NUME0 [7]	PLL2_0 NDIV2 Setting
	0	0	0	0	0	0	0	0	
33h	NUME0 [6]	NUME0 [5]	NUME0 [4]	NUME0 [3]	NUME0 [2]	NUME0 [1]	NUME0 [0]	DENO0 [8]	
	0	0	0	0	0	0	0	0	
34h	DENO0 [7]	DENO0 [6]	DENO0 [5]	DENO0 [4]	DENO0 [3]	DENO0 [2]	DENO0 [1]	DENO0 [0]	
	0	0	0	0	0	0	0	0	
35h	Reserved	Reserved	MDIV1[2]	MDIV1[1]	MDIV1[0]	VCO2_ RANGE1 [1]	VCO2_ RANGE1 [0]	Reserved	PLL2_1 MDIV2 Setting
	0	0	0	0	0	0	0	0	fVCO2_ Range1
36h	NINT1 [5]	NINT1 [4]	NINT1 [3]	NINT1 [2]	NINT1 [1]	NINT1 [0]	NUME1 [8]	NUME1 [7]	PLL2_1 NDIV2 Setting
	0	0	0	0	0	0	0	0	
37h	NUME1 [6]	NUME1 [5]	NUME1 [4]	NUME1 [3]	NUME1 [2]	NUME1 [1]	NUME1 [0]	DENO1 [8]	
	0	0	0	0	0	0	0	0	
38h	DENO1 [7]	DENO1 [6]	DENO1 [5]	DENO1 [4]	DENO1 [3]	DENO1 [2]	DENO1 [1]	DENO1 [0]	
	0	0	0	0	0	0	0	0	

PLL2 Configuration Register

PLL2 Block Diagram is as the following Figure.
Set PLL2 parameter according to. Frequency Setting Procedure on page 16.
PLL2 has two Frequency mode predefined as PLL2_0 or PLL2_1 and selected by S[2:0] bits (Address: 00h) or S0/S1/S2 pin.
Refer to Programmable Control pin setting on page 18 for more information about Frequency selection.

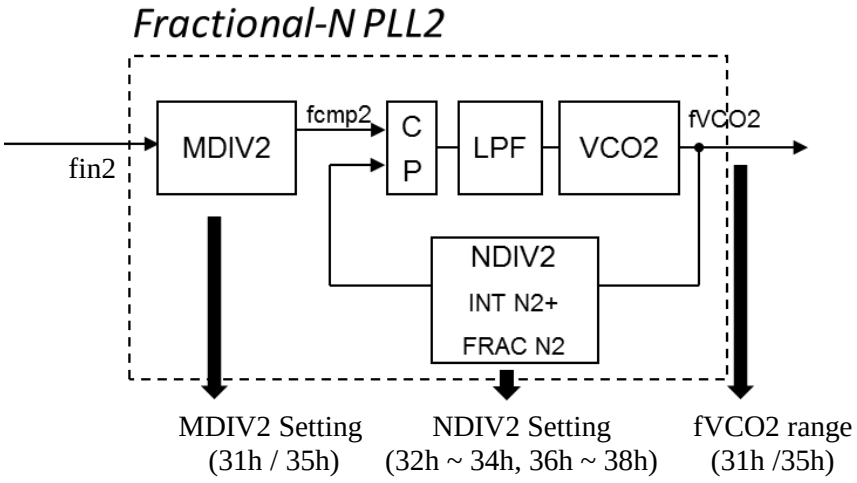


Figure 17. PLL2 Block Diagram

Address: 30h PLL2 Output Frequency selection

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	FS2_0	FS2_1	FS2_2	FS2_3	FS2_4	FS2_5	FS2_6	FS2_7

FS2_x (x = 0-7): PLL2 Output Frequency selection

The output frequency of PLL2 is chosen from two setups, PLL2_0 or PLL2_1.

Table 30. PLL2 Output Frequency selection

FS2_x	PLL2 Frequency
0	PLL2_0 Predefined by address: 31h ~ 34h (Default)
1	PLL2_1 Predefined by address: 35h ~ 38h

(x=0-7)

Address: 31h / 35h MDIV2 and fVCO2 frequency range Setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
31h 35h	Reserved	Reserved	MDIVn[2]	MDIVn[1]	MDIVn[0]	VCO2_ RANGEn [1]	VCO2_ RANGEn [0]	Reserved

(n = 0, 1)

MDIVn[2:0]: MDIV2 Dividing Value Setting (n = 0, 1)

MDIV2Configuration is as the following Figure.
MDIV2 Dividing Value can be set according to Frequency Setting Procedure on page 16.

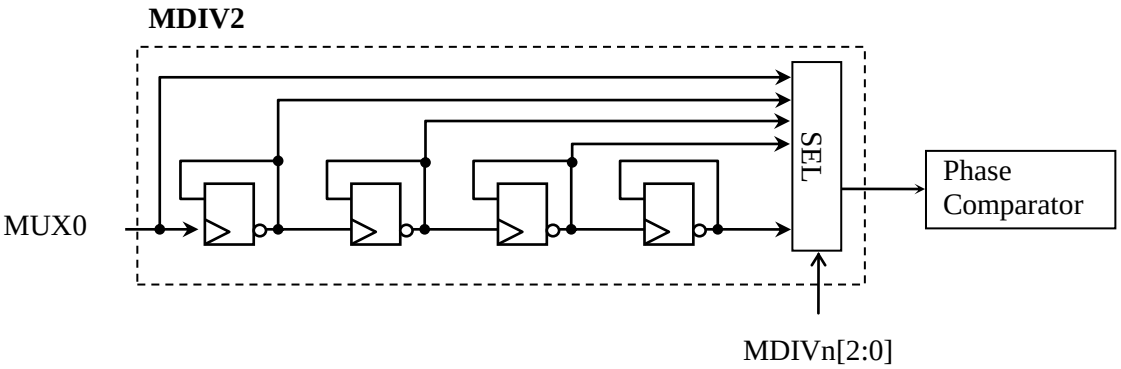


Figure 18. MDIV2 configuration

Table 31. MDIVn Programmable divider control (n = 0, 1)

MDIVn[2:0]	MDIV2 Dividing Value
000	1 (Default)
001	2
010	4
011	8
100	16
Except the above	Prohibited (Device is Reset)

VCO2_RANGEn[1:0]: fVCO2 range selection (n = 0, 1)

"VCO2_RANGEn[1:0]" selects the fVCO2 frequency range. fVCO2 frequency can be set according to Frequency Setting Procedure on page 16.

Table 32. fVCO2 range selection (n = 0, 1)

VCO2_RANGEn[1:0]	fVCO2 range
00	fVCO2 < 117.5MHz (Default)
01	117.5MHz ≤ fVCO2 < 155MHz
10	155MHz ≤ fVCO2 < 192.5MHz
11	192.5MHz ≤ fVCO2

Address: 32h ~ 34h, 36h ~ 38h NDIV2 Dividing Value (n = 0, 1)

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
32h 36h	NINTn [5]	NINTn [4]	NINTn [3]	NINTn [2]	NINTn [1]	NINTn [0]	NUMEn [8]	NUMEn [7]
33h 37h	NUMEn [6]	NUMEn [5]	NUMEn [4]	NUMEn [3]	NUMEn [2]	NUMEn [1]	NUMEn [0]	DENOn [8]
34h 38h	DENOn [7]	DENOn [6]	DENOn [5]	DENOn [4]	DENOn [3]	DENOn [2]	DENOn [1]	DENOn [0]

(n = 0, 1)

When a Certain Setting is set by three Address, write the data to all Address.
NDIV2 Dividing Value settings are updated after writing register 34h / 38h.
Setting procedure should be (1)32h / 36h , (2)33h / 37h, and then (3)34h / 38h.

NDIV2 dividing value can be set according to Frequency Setting Procedure on page 16.
NDIV2 Dividing Value is decided by setting NINTn, NUMEn and DENOn.

NINTn[5:0]: NDIV2 integral part setting (n = 0, 1)

NINTn[5:0] must be set from "010000" to "111001", when PLL2 is used.

Table 33. NDIV2 integral part setting (n = 0, 1)

NINTn[5:0]	NDIV2 Integral Part
000000	(Default)
000001 ~ 001111	prohibited
010000	16
:	:
100011	35
100100	36
100101	37
:	:
111001	57
111010 ~ 111111	prohibited

NUMEn[8:0]: NDIV2 Numerator of fractional part setting (n = 0, 1)

Table 34. NDIV2 Numerator of fractional part setting (n = 0, 1)

NUMEn[8:0]	NDIV2 Numerator of fractional part setting
000000000	0 (Default) (Integer-N Mode)
000000001	1
:	:
111111110	510
111111111	511

DENOn[8:0]: NDIV2 Denominator of fractional part setting (n = 0, 1)

DENOn[8:0] must be set from “000000001” to “111111111”, when PLL2 is used.

Table 35. NDIV2 Denominator of fractional part setting (n = 0, 1)

DENOn[8:0]	NDIV2 Denominator of fractional part setting
000000000	(Default)
000000001	1
:	:
111111110	510
111111111	511

10. Recommended External Circuits

Typical Connection Diagram

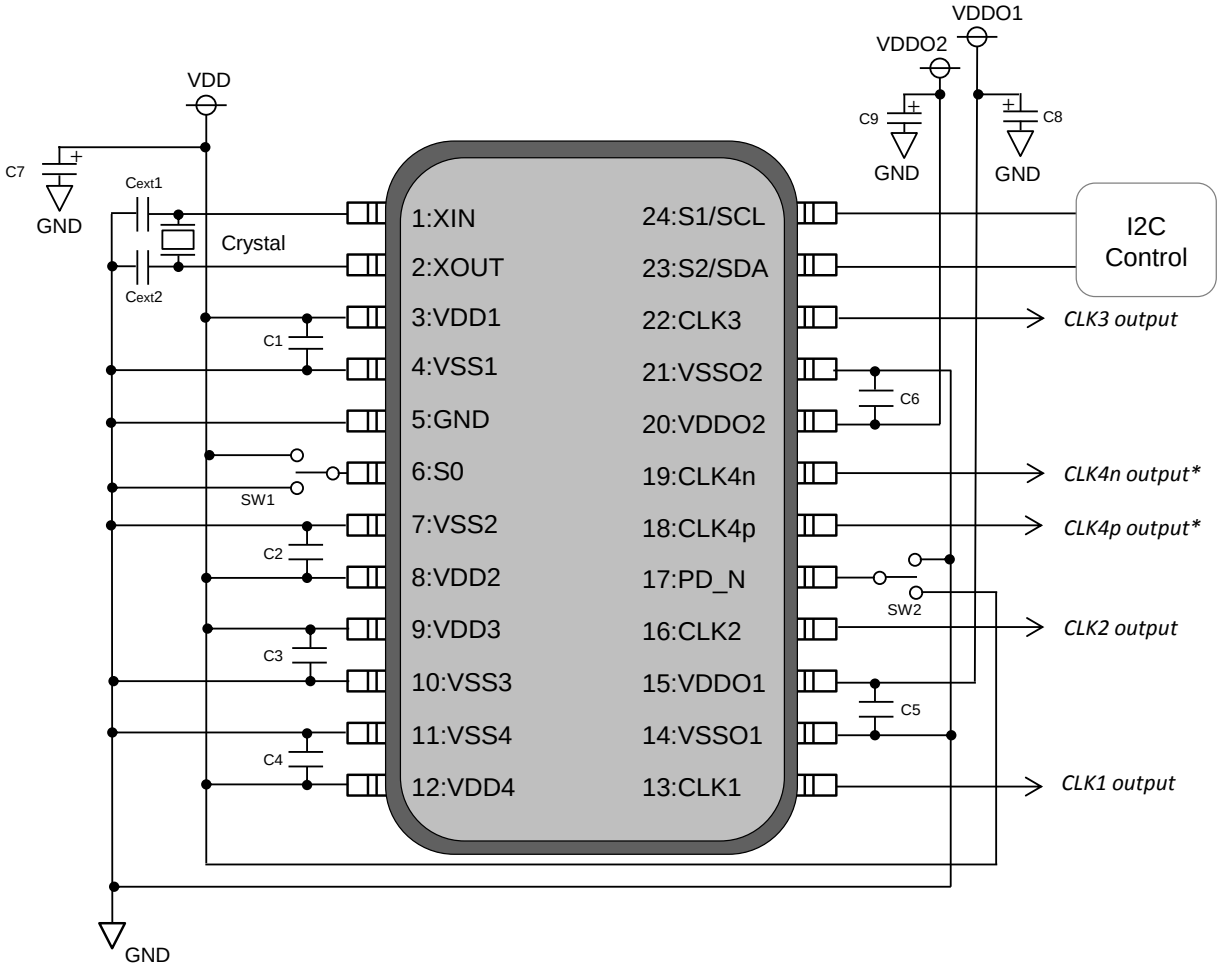


Figure 19. Typical Connection Diagram

C1, C2, C3, C4, C5, C6:	0.1μF Ceramic Capacitor
C7, C8, C9:	Electrolytic capacitor
Cext1, Cext2:	Depends on crystal characteristics. Refer to the specification of the crystal.
SW1:	This switch controls 'H' and 'L' of S0 control pin. Refer to the datasheet about S0 control.
SW2:	This switch that controls 'H' and 'L' of PD_N pin. Refer to the datasheet about PD_N control.

*1: When CLK4n and CLK4p pin output LVDS clock, refer to the LVDS Clock measurement circuit shown on this datasheet page 11.
*2: No. 23 SDA/S2 pin has the internal pull-up 500kΩ resister.
*3: No. 24 SCL/S1 pin has the internal pull-down 500kΩ resister.

Crystal Unit

Table 36. DAISHINKU Corp. DSX321G

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Nominal frequency	f0		25.000		MHz	CL = 8pF
Equivalent resistance	R1		18.2	60	Ω	
Shunt capacitance	C0		1.22		pF	
Motional capacitance	C1		4.724		fF	
Motional inductance	L1		8.585		mH	
Drive Level			30		μW	±2 μW

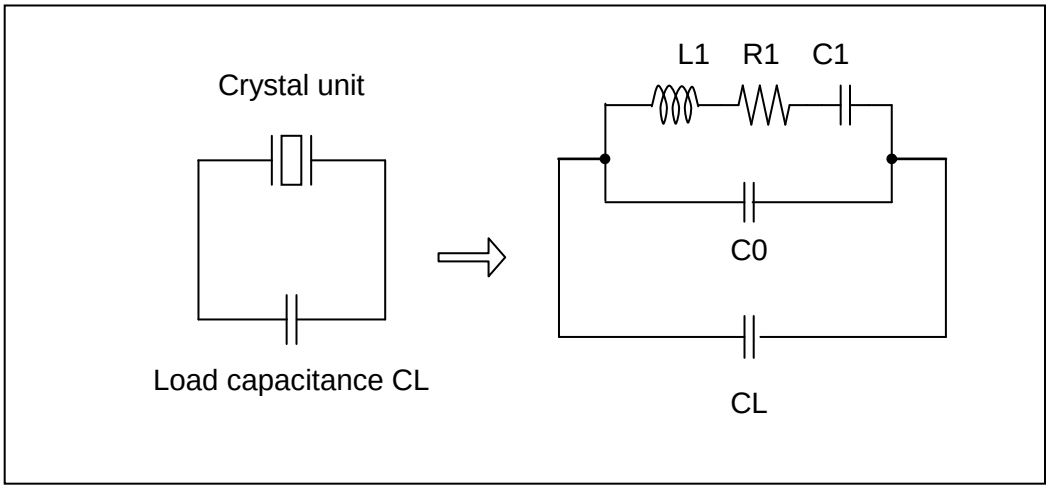
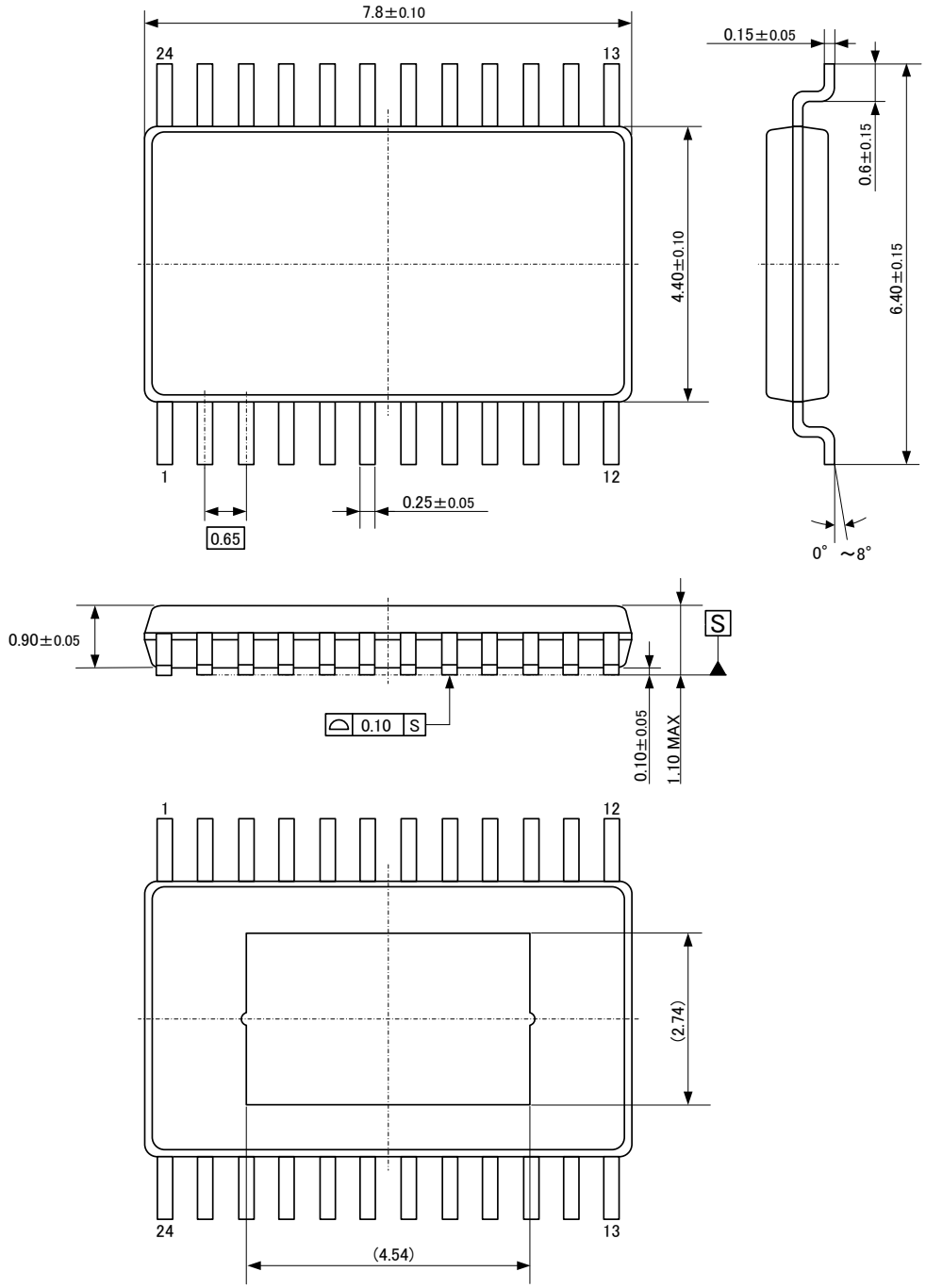


Figure 20. Equivalent parameter and load

11. Package

Outline Dimensions

24pin HTSSOP (Unit : mm)

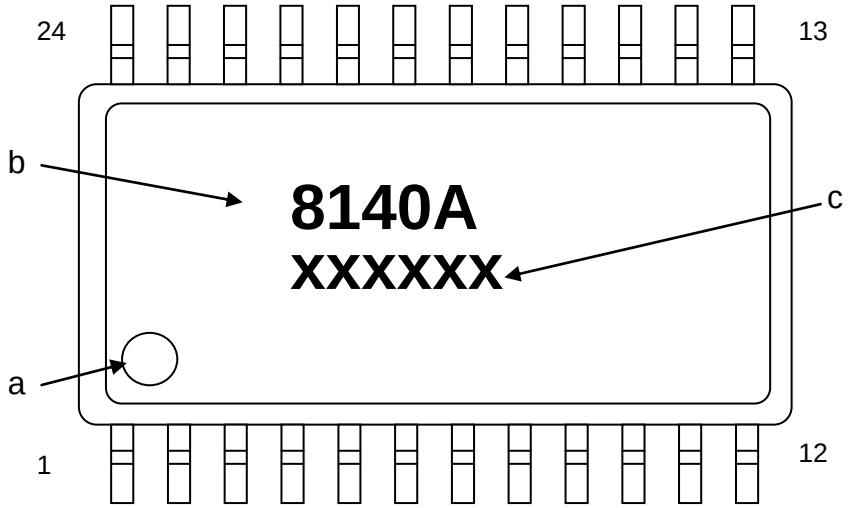


Note:

(1) The Heat sink pad on the bottom surface of the package is recommended to solder to the PCB.

Marking

a: #1 Pin Index
b: Part number
c: Date code (6 digits)



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