AK8147DV2
Programmable Multi Clock Generator with XO

1. General Description

The AK8147DV2 is a member of AKM's High-performance programmable clock generator. The AK8147DV2 generates up to six output clocks from a single input frequency with four fractional-N PLLs. Each output can be programmed for any frequency up to 148.5MHz. PLLs in AK8147DV2 are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. In addition, enables 'Dynamic Frequency Control'. The AK8147DV2 is available in a 32-pin QFN package.

2. Features

- In-System Programmability
  - Serial Programmable Register via SDA/SCL pin
- High Accuracy Clock Generator
- Flexible Input Clock Source
  - Crystal Unit : 8MHz - 50MHz
  - External Clock : 2.8224MHz - 100MHz
- Free Programmable Clock Frequencies
  - LVCMOS : 187.5Hz - 148.5MHz (CLK1-6)
- Low Jitter Performance by using PLL2-4
  - Period Jitter (1σ) : 6.7ps typ.
  - Cycle to Cycle Jitter (1σ) : 9.0ps typ.
  - Long Term Jitter (1000 cycle, 1σ) : 20.0ps typ.
- Supply Voltage
  - Device Power Supply : VDD : 3.0 - 3.6V
  - Output Buffer Power Supply : VDDO1-6 : 1.7 - 3.6V
- Operating Temperature Range
  - -40 to +105°C
- Package
  - 32-pin QFN (Lead free)
- Dynamic Frequency Control by using PLL1 only
  - Configurable output tuning
- Application
  - Car Navigation, Display Audio, Automotive Video System, AVB Ethernet and VCXO replacement
  - Audio Amplifier System, AV Receiver, DTV System, STB, IP-STB, DVD Player and DVD Recorder

3. Table of Contents

4. Block Diagram and Functions

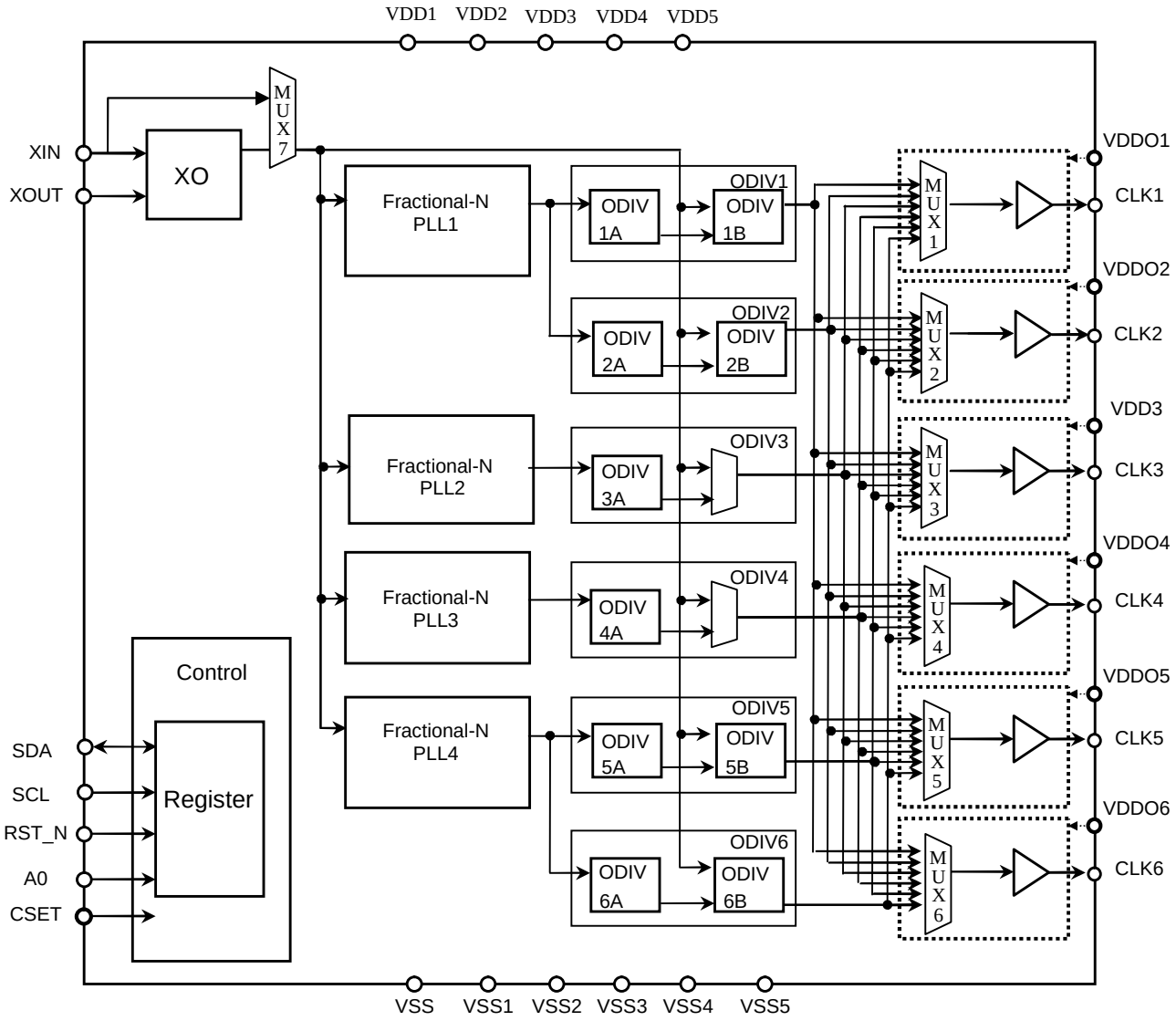


Figure 1. AK8147DV2 Programmable Multi Clock Generator with XO

5. Pin Configurations and Functions

■ Pin Layout

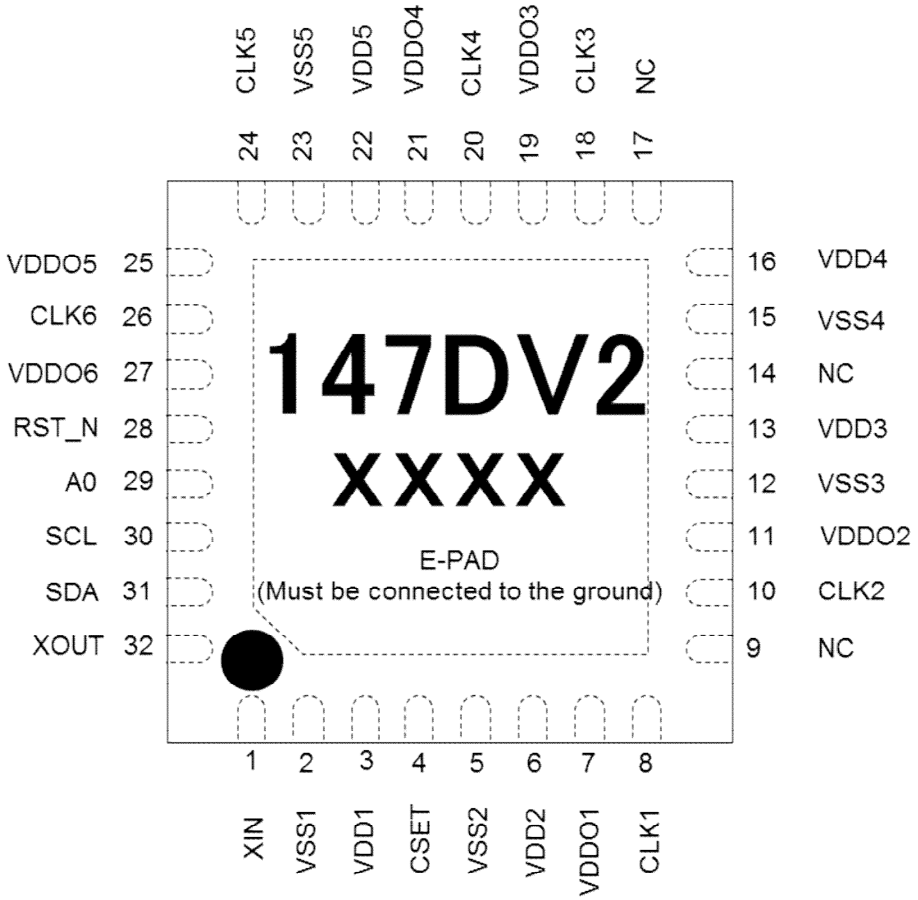


Figure 2. AK8147DV2 Package: 32-Pin QFN (Top View)

■ Pin Functions

Pin No.	Pin Name	Pin Type	Description
1	XIN	AI/DI	Crystal connection or External clock input
2	VSS1	PWR	Connect to Ground
3	VDD1	PWR	Device Power Supply 1
4	CSET	DI	Register default value control pin *Table.
5	VSS2	PWR	Connect to Ground
6	VDD2	PWR	Device Power Supply 2
7	VDDO1	PWR	Power Supply1 for Output Buffer CLK1
8	CLK1	DO	LVCMOS Output pin1
9,14,17	NC	PWR	Connect to Ground
10	CLK2	DO	LVCMOS Output pin2
11	VDDO2	PWR	Power Supply2 for Output Buffer CLK2
12	VSS3	PWR	Connect to Ground
13	VDD3	PWR	Device Power Supply 3
15	VSS4	PWR	Connect to Ground
16	VDD4	PWR	Device Power Supply 4
18	CLK3	DO	LVCMOS Output pin3
19	VDDO3	PWR	Power Supply3 for Output Buffer CLK3
20	CLK4	DO	LVCMOS Output pin4
21	VDDO4	PWR	Power Supply4 for Output Buffer CLK4
22	VDD5	PWR	Device Power Supply 5
23	VSS5	PWR	Connect to Ground
24	CLK5	DO	LVCMOS Output pin5
25	VDDO5	PWR	Power Supply5 for Output Buffer CLK5
26	CLK6	DO	LVCMOS Output pin6
27	VDDO6	PWR	Power Supply6 for Output Buffer CLK6
28	RST_N	DI	Reset control ''L'': Reset ''H'': Reset Release
29	A0	DI	Slave Receiver Address control
30	SCL	DI	Serial Clock Input
31	SDA	DIO	Serial Data Input / Output
32	XOUT	AO	Crystal connection Open when an external clock input is used
E-PAD	VSS	PWR	The exposed pad on the bottom surface of the package must be connected to the ground.

Note:
(1) AI : Analog Input pin
AO : Analog Output pin
DI : Digital Input pin
DO : Digital Output pin
DIO : Digital Input and Output pin
PWR : Power Supply pin

6. Absolute Maximum Ratings

VSS=VSS1=VSS2=VSS3=VSS4=VSS5=0V
Over operating free-air temperature range unless otherwise noted (2)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3* (min VDD-4.6) (max 4.6)	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-65 to 150	°C

Note
(2) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		105	°C
Supply voltage (3)	VDD	Pin: VDD1-5	3.0	3.3	3.6	V
	VDDO	Pin: VDDO1-6 Power Supply for CLK1 and CLK2 Output Buffers	1.7	1.8 3.3	3.6	
Output Load Capacitance (4)	Cplclk	Pin: CLK1-6 Output Frequency : up to 75MHz (VDDOn=1.8V) up to 120MHz (VDDOn=3.3V)			25	pF
		Pin: CLK1-6 Output Frequency : up to 100MHz (VDDOn=1.8V) up to 140MHz (VDDOn=3.3V)			15	
		Pin: CLK1-6 Output Frequency : up to 148.5MHz up to 148.5MHz (VDDOn=1.8V) up to 148.5MHz (VDDOn=3.3V)			10	

Note:
(3) Power to VDD1-6 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pins.
(4) Refer to Table18 (p.25).

8. Electrical Characteristics

■ DC Characteristics

All specifications at VDD1-5: 3.0 to 3.6V, VDDO1-6: 1.7 to 3.6V, Ta: -40 to +105°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	Pin: RST_N, SCL, SDA, XIN CSET, A0	0.7*VDD		VDD	V
Low Level Input Voltage	V_{IL}	Pin: RST_N, SCL, SDA, XIN CSET, A0	VSS		0.3*VDD	V
Input Current	I_L	Pin: RST_N, SCL, SDA CSET, A0 VDD or VSS force	-1		+1	μA
Low Level Output Voltage	V_{OL}	Pin: SDA I_{OL} = +3mA, Open Drain			0.2*VDD	V
Current Consumption 1(5)	$I_{DD}1$	All outputs 'ON', No load Input / Output frequency XIN: 26MHz CLK1: 24.576MHz CLK2/3: 27MHz CLK4: 37.007MHz CLK5: 48MHz CLK6: 26MHz CLKnDL [1:0] bit = ''00''		52	65	mA
Current Consumption 2(5)	$I_{DD}2$	All outputs 'OFF' Input / Output frequency XIN: 26MHz CLK1: 24.576MHz CLK2/3: 27MHz CLK4: 37.007MHz CLK5: 48MHz CLK6: 26MHz CLKnOE [1:0] bit =''01'' / ''10'' / ''11''		46	58	mA
Power Down Mode Current Consumption(6)	SI_{DD}	No load, Power Down Mode PWDN = '1', CLKnOE [1:0] bit = except''00''		0.5	50	μA

Note:

(5) Typ : VDDO1/2=3.3V , VDDO3-6=1.8V, Max : VDDO1/2=3.6V , VDDO3-6=1.9V

(6) VDD1-5 = VDDO1-6 = 3.6V

■ AC Characteristics

All specifications at VDD1-5: 3.0 to 3.6V, VDDO1-6: 1.7 to 3.6V, Ta: -40 to +105°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Clock Frequency	F_{osc}	Pin: XIN, XOUT	8		50	MHz
External Clock Input Frequency	F_{in}	Pin: XIN When External Input is selected. OSC_DIS = '1'	2.8224		100	MHz
External Clock Input Duty Cycle	F_{indc}	Pin: XIN When External Input is selected Measurement point: 0.5*VDD	30	50	70	%
Output Clock Frequency Accuracy (7)(8)	$F_{accuracy}$	Pin: XIN, XOUT	-30		+30	ppm
Output Lock Time (9)	T_{lock}	Pin: CLK1-5 PLL1		1	2	ms
		Pin: CLK1-5 PLL2-4		0.1	0.3	ms
		Pin: CLK6 Input frequency = 8 – 11MHz		2	5	ms
		Pin: CLK6 Input frequency = 11 – 50MHz	Crystal /Ext-	1	2	ms

Note:

(7) Specification of Frequency Accuracy is measured by connecting the standard crystal unit.

(8) This Output Clock Frequency Accuracy does not include accuracy of crystal unit.
Total output clock frequency accuracy could be up to "Output Clock Frequency Accuracy" + "Crystal unit accuracy".

(9) Settling time that output frequency reaches within the accuracy 0.1 % of the target frequency after registers ''01h'', ''20h to 24h'', ''30h to 34h'', ''40h to 44h'', or ''50h to 54h'' are set through SCA/SCL pins.

■ PLL Characteristics

All specifications at VDD1-5: 3.0 to 3.6V, VDDO1-6: 1.7 to 3.6V, Ta: -40 to +105°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PLL1 Characteristics						
VCO Frequency 1	fVCOA	VCO frequency range of PLL1	216		432	MHz
Phase Comparison Frequency 1	fcmpA		2.8224		14.375	MHz
Period Jitter 1 (10)(11)(13)	Jit_period	Jitter of Output Clock from PLL1, 1σ		6.7		ps
Cycle to Cycle Jitter 1 (10)(11)(13)	Jit_c2c	Jitter of Output Clock from PLL1, 1σ		9.0		ps
Long Term Jitter 1 (10)(12)(13)	Jit_long	Jitter of Output Clock from PLL1, 1000 cycle delay, 1σ		50.0		ps
PLL2-4 Characteristics						
VCO Frequency 2-4	fVCOB	VCO frequency range of PLL2-4	216		432	MHz
Phase Comparison Frequency 2-4	fcmpB		2.8224		14.375	MHz
Period Jitter 2-4 (10)(12)(13)	Jit_period	Jitter of Output Clock from PLL2-4, 1σ		6.7		ps
Cycle to Cycle Jitter 2-4 (10)(12)(13)	Jit_c2c	Jitter of Output Clock from PLL2-4, 1σ		9.0		ps
Long Term Jitter 2-4 (10)(12)(13)	Jit_long	Jitter of Output Clock from PLL2-4, 1000 cycle delay, 1σ		20.0		ps

Note:

(10) The load conditions are described on page 6.

(11) Jitter depends on configuration.
Jitter data is for input frequency = 26MHz, output frequency = 37.007MHz

(12) Jitter depends on configuration.
Jitter data is for input frequency = 26MHz, output frequency = 24.576MHz

(13) 10,000 sampling or more

■ LVCMOS Characteristics

All specifications at VDD1-5: 3.0 to 3.6V, VDDO1-6: 1.7 to 3.6V, Ta: -40 to +105°C, unless otherwise noted

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Output Frequency	fout	Pin: CLK1-6			0.0001875		148.5	MHz
High Level Output Voltage	VOH	Pin: CLK1-6 IOH = -0.5mA			0.8*VDDOn (n=1-6)			V
Low Level Output Voltage	VOL	Pin: CLK1-6 IOH = +0.5mA					0.2*VDDOn (n=1-6)	V
Output Clock Rise Time (14) (15) (16)	T_rise	CLKnDL [1:0] = "00"	Load Cplclk	10pF		0.7 / 0.3 (24)		ns
				15pF		0.9 / 0.4 (24)		
				25pF		1.2 / 0.6 (24)		
		CLKnDL [1:0] = "01"		10pF		1.9 / 0.9 (24)		ns
				15pF		2.5 / 1.3 (24)		
				25pF		3.7 / 1.9 (24)		
		CLKnDL [1:0] = "10"		10pF		2.9 / 1.4 (24)		ns
				15pF		3.8 / 1.9 (24)		
				25pF		5.5 / 2.8 (24)		
		CLKnDL [1:0] = "11"		10pF		5.8 / 2.9 (24)		ns
				15pF		7.5 / 3.8 (24)		
				25pF		11.0 / 5.7 (24)		
Output Clock Fall Time (14) (15) (17)	T_fall	CLKnDL [1:0] = "00"	Load Cplclk	10pF		0.6 / 0.3 (24)		ns
				15pF		0.7 / 0.4 (24)		
				25pF		1.1 / 0.7 (24)		
		CLKnDL [1:0] = "01"		10pF		1.8 / 1.2 (24)		ns
				15pF		2.3 / 1.6 (24)		
				25pF		3.3 / 2.3 (24)		
		CLKnDL [1:0] = "10"		10pF		2.7 / 1.9 (24)		ns
				15pF		3.6 / 2.5 (24)		
				25pF		5.2 / 3.7 (24)		
		CLKnDL [1:0] = "11"		10pF		5.0 / 3.2 (24)		ns
				15pF		6.5 / 4.3 (24)		
				25pF		9.6 / 6.3 (24)		
Output Clock Duty Cycle (14)	T_outdc	Pin: CLK1-6 (18)			45	50	55	%
		Pin: CLK1-6 (19)			40	50	60	%
		Pin: CLK1-6 (20)			45	50	55	%
		Pin: CLK1-6 (21)			40	50	60	%
		Pin: CLK1-6 (22)			45	50	55	%
		Pin: CLK1-6 (23)			45	50	55	%

Note:

(14) The load conditions are described on page 6
(15) Pin : CLK1-6
(16) 0.2VDDO1-6 → 0.8VDDO1-6
(17) 0.8VDDO1-6 → 0.2VDDO1-6
(18) ODIVn divides the Input Bypass Clock or PLL Clock by even dividing value.
(19) ODIVn divides the Input Bypass Clock or PLL Clock by odd dividing value. Fout>60MHzh
(20) ODIVn divides the Input Bypass Clock or PLL Clock by odd dividing value. Fout<60MHz
(21) External input, no divide, INSEL= '0'. Fout<33MHz
(22) External input, no divide, INSEL= '1',
(23) XO CLK, no divide,
(24) VDDO1-6=1.8V/3.3V

■ Serial Interface (SDA/SCL pin) AC Characteristics(25)

All specifications at VDD1-5: 3.0 to 3.6V, VDDO1-6: 1.7 to 3.6V, Ta: -40 to +105°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	fSCL				400	kHz
SCL Clock Low Period	tLOW		1.3			μs
SCL Clock High Period	tHIGH		0.6			μs
Pulse Width of Spikes which must be suppressed	tI				50	ns
SCL Low to SDA Data Out	tAA		0.3			μs
Bus free time between a STOP and START Condition	tBUF		1.3			μs
Start Condition Hold Time	tHD.SAT		0.6			μs
Start Condition Setup Time (for a Repeated Start Condition)	tSU.SAT		0.6			μs
Data in Hold Time	tHD.DAT		0			μs
Data in Setup Time	tSU.DAT		100			ns
SDA and SCL Rise Time	tR				0.3	μs
SDA and SCL Fall Time	tF				0.3	μs
Stop Condition Setup Time	tSU.STO		0.6			μs
Input Capacitance at SDA/SCL	Cb				200	pF

Note:

(25) The AK8147DV2 operates as a slave device of the 2-wire serial SDA/SCL bus.
This serial interface can be used the I2C interface timing.
It operates in the standard-mode transfer (up to 100kbit/s) and the fast-mode transfer (up to 400kbit/s).
It doesn't support the Clock Stretching Mode and the High Speed Mode.

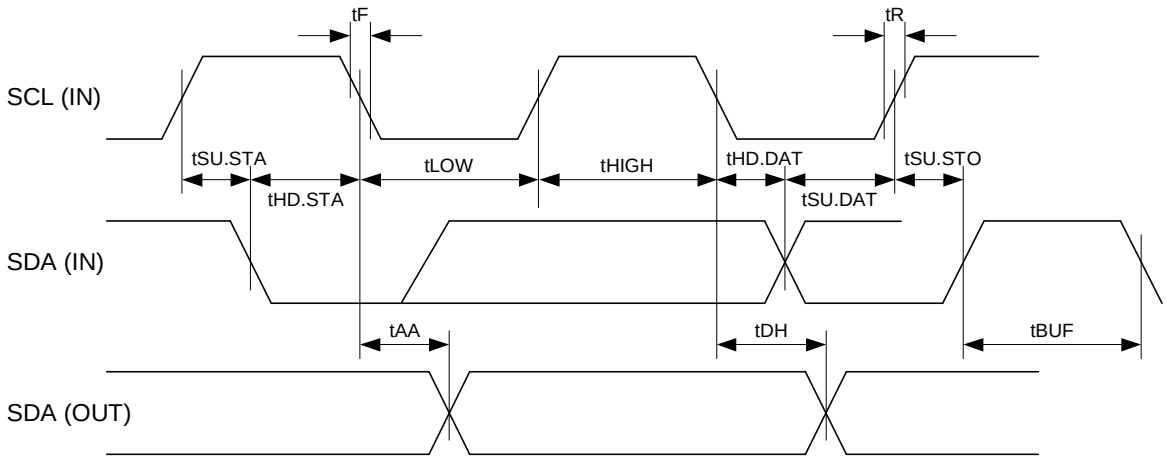


Figure 3. 2-wire Serial Interface AC Timing

9. Functional Descriptions

■ PLL1 setting procedure

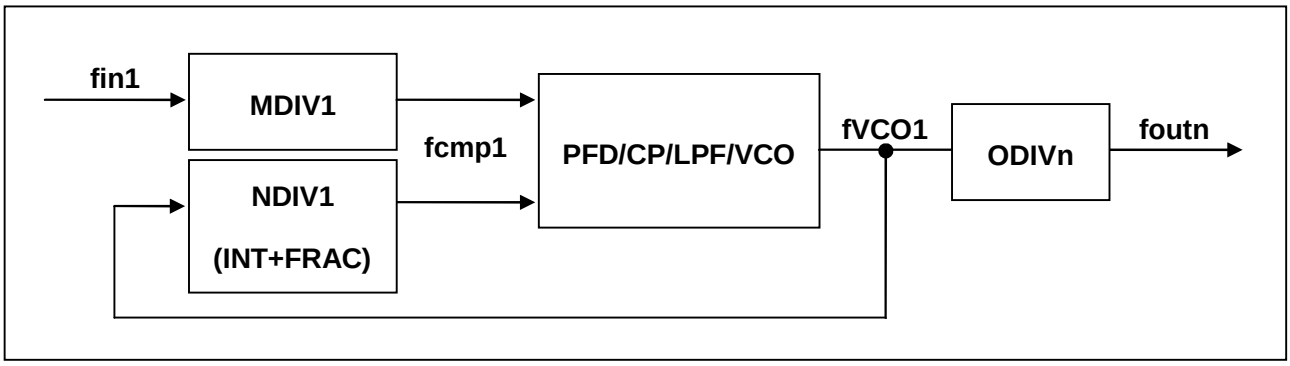


Figure 4. PLL1 Block Diagram

PLL1 is Fractional-N PLL. Output frequency is determined by parameters as follows:
Refclk Divider (MDIV1), Fractional-N1 Divider (INT + FRAC), and Output Divider (ODIVn(n = 1-6)).

These parameters should be set as described below.

Step1. VCO1 Target Frequency setting

VCO1 Frequency (fVCO1) is calculated from CLKn Output frequency (foutn) and Output Divider (ODIVn : 09h-10h). Set fVCO1 frequency between 216MHz to 432MHz.

216MHz ≤ fVCO1 ≤ 432MHz (fVCO1 = foutn × ODIVn)

Step2. Phase Comparison Frequency setting

Set MDIV1 (MDIV1 [1:0] : 20h) as fcmp1 becomes the greatest common measure of fin1 and fvco1 between 2.8224MHz to 14.375MHz .

2.8224MHz ≤ fcmp1 ≤ 14.375MHz (fcmp1 = fin1 / MDIV1)

Step3. Feedback Divider setting

This value is determined by VCO1 frequency (fVCO1) and Phase Comparison Frequency (fcmp1).
8 bits integral part and 18 bits fractional part (signed 2's complement) are necessary to be set.

$$NDIV1 = \frac{fVCO1}{fcomp1} = N_{INT1} + \frac{N_{FRAC1}}{2^{18}}$$

Integral part (NINT1) : NINT1 = INT1[7:0] = round [fVCO1 / fcmp1]
Fractional part (NFRAC1 / 218) : NFRAC1 = FRAC1[17:0] = round [((fVCO1 / fcmp1) – NINT1) × 218]

Dynamic frequency control

PLL1 enables configurable output frequency tuning during operation by FRAC1 [17:0] register setting.
FRAC1 [17:0] register must be executed under condition as follows,
- XIN input frequency is stable

After completion of 24h address setting, 18bits data in 22h – 24h will be updated.

Please avoid the frequency setting in below condition.
1. Over 500ppm range
2. Fractional part doesn't satisfied with the condition [-131070< FRAC < +131071], or
   16 conditions as follows

No.	FRAC1[17:0] (BIN)	(DEC)	Fractional value
1	01 1100 0000 0000 0000	+114688	0.4375
2	01 1000 0000 0000 0000	+98304	0.375
3	01 0100 0000 0000 0000	+81920	0.3125
4	01 0000 0000 0000 0000	+65536	0.25
5	00 1100 0000 0000 0000	+49152	0.1875
6	00 1000 0000 0000 0000	+32768	0.125
7	00 0100 0000 0000 0000	+16384	0.0625
8	00 0000 0000 0000 0000	0	0
9	11 1100 0000 0000 0000	+16384	-0.0625
10	11 1000 0000 0000 0000	+32768	-0.125
11	11 0100 0000 0000 0000	+49152	-0.1875
12	11 0000 0000 0000 0000	+65536	-0.25
13	10 1100 0000 0000 0000	+81920	-0.3125
14	10 1000 0000 0000 0000	+98304	-0.375
15	10 0100 0000 0000 0000	+114688	-0.4375
16	10 0000 0000 0000 0000	+131072	-0.5

■ PLL2-4 setting procedure

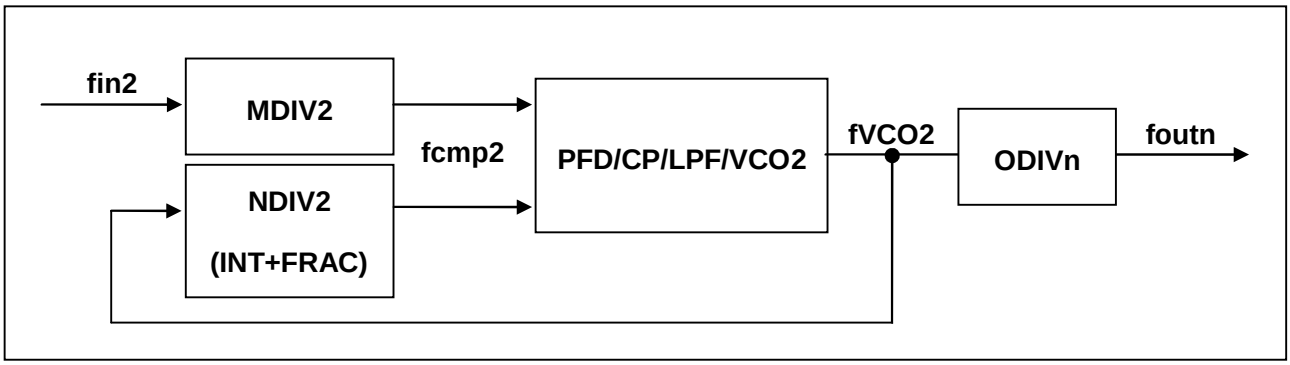


Figure 5. PLL2 Block Diagram

PLL2-4 are Fractional-N PLL. Output frequency is determined by parameters as follows:
Refclk Divider (MDIV2-4), Fractional-N2-4 Divider (INT + FRAC), and Output Divider (ODIVn(n = 1-6)).

These parameters should be set as described below.

Step1. VCO2-4 Target Frequency setting

VCO2-4 Frequency (fVCO2-4) is calculated from CLKn Output frequency (foutn) and Output Divider (ODIVn : 9h-10h). Set fVCO2-4 frequency between 216MHz to 432MHz.

216MHz ≤ fVCO2-4 ≤ 432MHz (fVCO2-4 = foutn × ODIVn)

Step2. Phase Comparison Frequency setting

Set MDIV2-4 Divider (MDIV[1:0], set by address: 30h/40h/50h) as fcmp2 becomes the greatest common measure of fin2 and fvco2 between 2.8224MHz to 14.735MHz.

2.8224MHz ≤ fcmp2 ≤ 14.735MHz (fcmp2 = fin2 / MDIV2)

Step3. Feedback Divider setting

This value is determined by VCO2-4 frequency (fVCO2-4) and Phase Comparison Frequency (fcmp2-4).
8 bits integral part (INT2-4[7:0], set by address: 31h/41h/51h) and 9 bits x2 fractional part (numerator: NUMEn[8:0] and denominator: DENOn[8:0], set by address: 32h-34h/42h-44h/52h-54h) are necessary to be set.

$$NDIV2 = \frac{fVCO2}{fcomp2} = N_{INT2} + N_{FRAC2} = N_{INT2} + \frac{N_{NUME}}{N_{DENO}}$$

Integral part = NINT2 = INTn[7:0] = rounddown [fVCO2 / fcmp2]
Fractional part = NFRAC2 = NNUME / NDENO is calculated as below.

First calculate optimum NDENO = DENOn[8:0]OPTIMUM.
DENOn[8:0]OPTIMUM can be obtained by substituting from 1 to 511 into the DENOn[8:0] in the following formula.

When min [abs [(round [NFRAC2 × DENO2[8:0]]) / DENO2[8:0]) – NFRAC2]]
DENO2[8:0]OPTIMUM = DENO2[8:0]

NUME2[8:0]OPTIMUM can be obtained by substituting DENO2[8:0]OPTIMUM in the following formula.
NUME2[8:0]OPTIMUM = round [NFRAC2 × DENO2[8:0]OPTIMUM]

■ Power up sequence

Step1 : Supply proper voltage to the power pins under RST_N pin = 'L' condition.
*Note : VDD1-5 must be supplied simultaneously.

Step2 : Set the RST_N pin to 'H' at least after 10µs from the point that the power supply reaches 90% of VDD.

Step3 : Setting Register.

Step4 : PLL output will be stable (±0.1%) within 2ms.

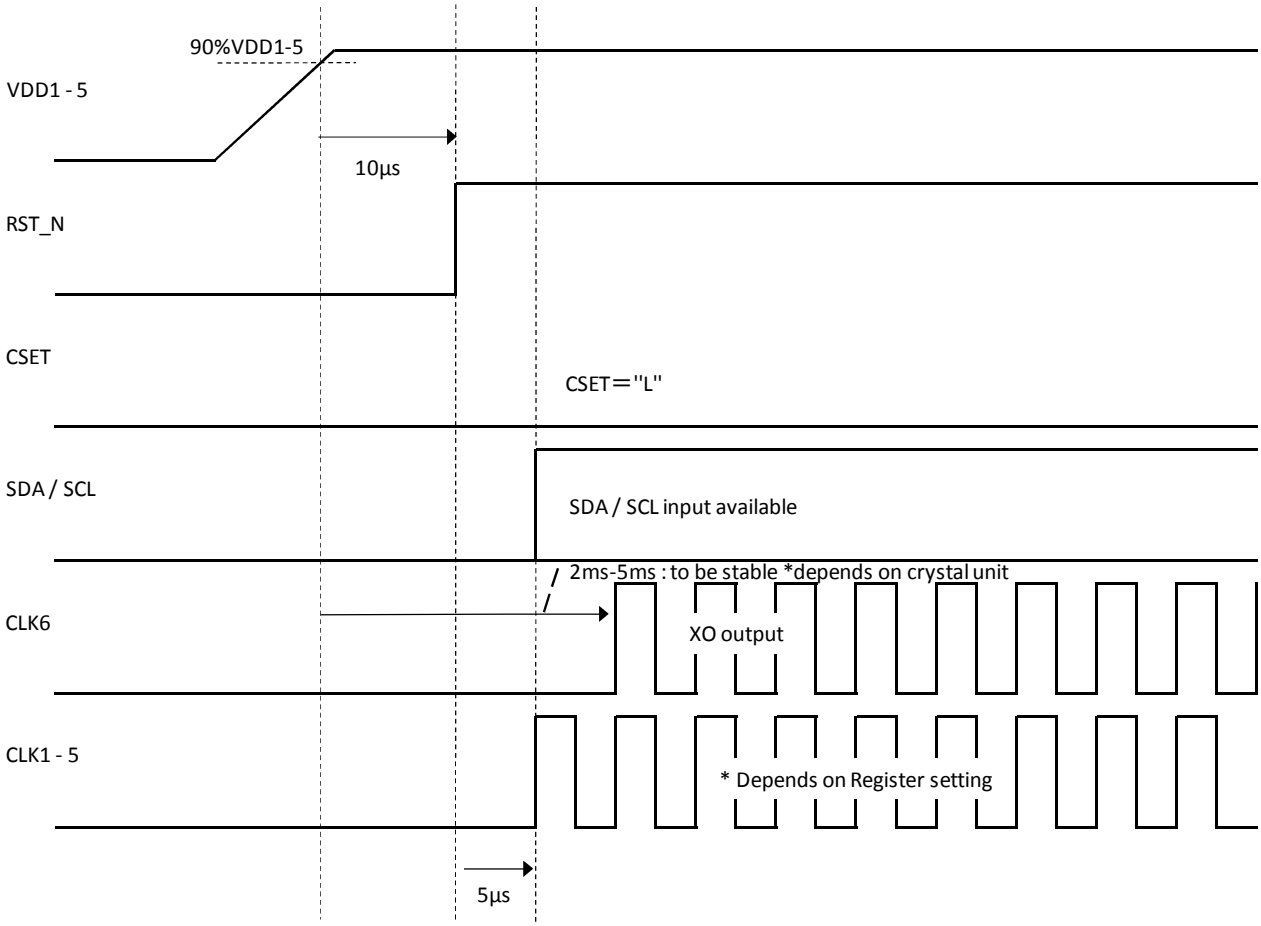


Figure 6. Power up sequence

Serial interface

Read/Write performance of serial interface is explained as below. The device address of AK8147DV2 is Device Address#1:1011, Device Address#2:01 A0. A0 is set by A0 pin.

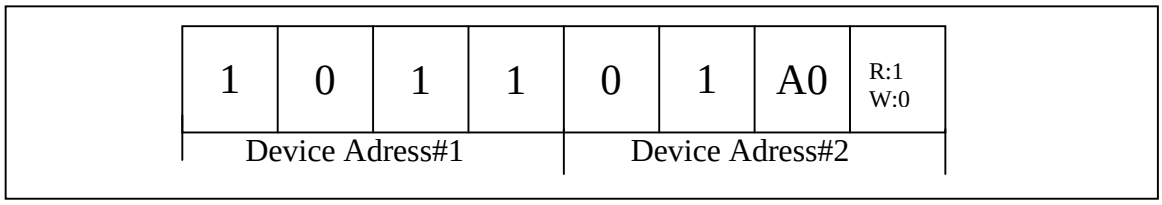


Figure 7. The Device Address of AK8147DV2

Write operation

Write operation is described below. Data must be sent after sending 8 bits address and receiving ACK. It is possible to write next address sequentially by sending next data instead of stop condition.
The address which is written after “12h/24h/34h/44h/54h” becomes “00h/20h/30h/40h/50h”.

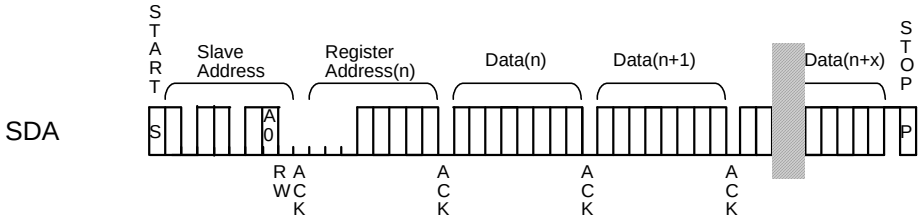


Figure 8. Write operation

Current address read

Current address read operation is described below. The data that is read by this operation is obtained as “last accessed address + 1”. Therefore, it is consequent to return “12h/24h/34h/44h/54h” after accessing the address “00h/20h/30h/40h/50h”.

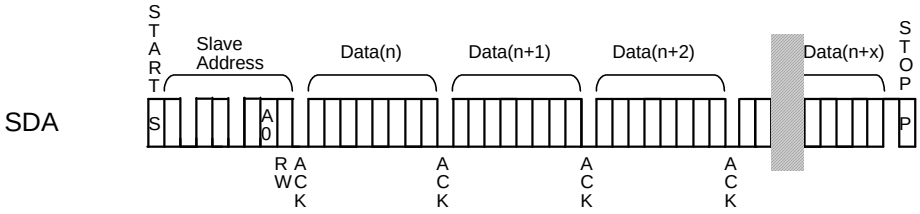


Figure 9. Current address read

Random read

Random read operation is described below. It is necessary to operate “dummy write” before sending read command. Dummy write is to send the address to read. It is possible to read next address sequentially by sending ACK instead of stop condition.

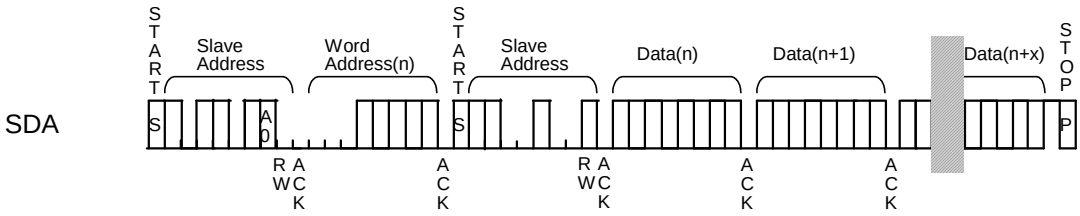


Figure 10. Random read

Change data

Change data operation is described below. It is available when SCL is Low.

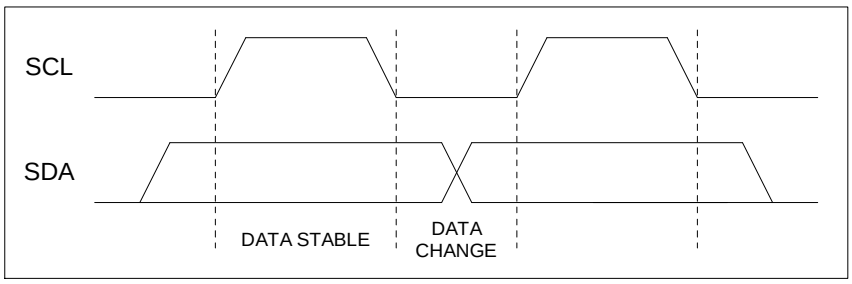


Figure 11. Change data

Start / Stop timing

Start / Stop timing is described below. The sequence is started when SDA goes from high to low during SCL is high. The sequence is stopped when SDA goes from low to high during SCL is high.

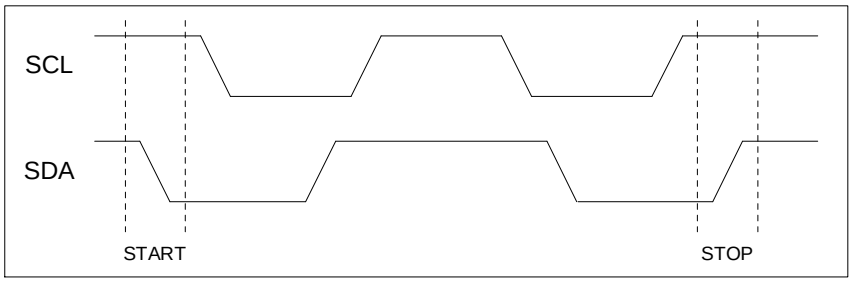


Figure 12. Start / Stop timing

■ Register Configuration

AK8147DV2 has Registers can be programmed via the serial SDA/SCL interface.
The following table and explanations describe the programmable functions of AK8147DV2.

- The default setting appears after power is supplied or after power-down/up sequence until it is reprogrammed to a different setting.
- All data transferred with the MSB first.
- When a Certain Setting is set by three Address, write the data to all Address.
  22h ~ 24h, 32h ~ 34h, 42h ~ 44h, 52h~54h
  FRACn[17:0] settings are updated after writing register 24h as last step.
  Setting procedure should be (1st) 22h , (2nd) 23h, and then (3rd) 24h.
- NDIV2 Divider settings are updated after writing register 34h / 44h /54h.
  Setting procedure should be (1st) 32h / 42h /52h , (2nd) 33h / 43h/ 53h, and then (3rd) 34h / 44h/ 54h.
- The other register except describing in Table 1 must be prohibited .

Table 1. AK8147DV2 Register Configuration

Address	Register	Remarks	Page
00h to 12h	Generic Configuration Register	CLK1 to 6 Setting · CLK1 to 6 Output State （CLK enabled / Disabled to L / Disabled to H / Hi-Z） · MUX1 to 6 (PLL1 fVCO1/ PLL2 fVCO2/ PLL3 fVCO3/ PLL4 fVCO4 / Input Bypass) · ODIV1 to 6 Parameter · CLK1 to 6 Output Buffer Drivability	p. 19 to p. 25
20h to 24h	PLL1 Configuration Register	PLL1 Setting （MDIV1, NDIV1, fVCO1 range）	p. 36 to p. 42
30h to 34h	PLL2 Configuration Register	PLL2 Setting （MDIV2, NDIV2, fVCO2 range）	p. 43 to p. 47
40h to 44h	PLL3 Configuration Register	PLL3 Setting （MDIV3, NDIV3, fVCO3 range）	p. 43 to p. 47
50h to 54h	PLL4 Configuration Register	PLL4 Setting （MDIV4, NDIV4, fVCO4 range）	p. 43 to p. 47

■ **Generic Configuration Register (Address: 00h ~ 12h)**

Address	Data								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
00h	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	00
Device Setting									
01h	Reserved	RID[1]	RID[0]	PWDN	PLL1PD	PLL2PD	PLL3PD	PLL4PD	0F 00(26)
02h	INSEL	PDIOSC	ODIV1 RST	ODIV2 RST	ODIV3 RST	ODIV4 RST	ODIV5 RST	ODIV6 RST	3E 10(26)
CLK1-6 Output State Setting									
03h	ODIV1 OE[1]	ODIV1 OE[0]	ODIV2 OE[1]	ODIV2 OE[0]	ODIV5 OE[1]	ODIV5 OE[0]	ODIV6 OE[1]	ODIV6 OE[0]	54 10(26)
04h	CLK1 OE[1]	CLK1 OE[0]	CLK2 OE[1]	CLK2 OE[0]	CLK5 OE[1]	CLK5 OE[0]	CLK6 OE[1]	CLK6 OE[0]	00
05h	ODIV3 OE[1]	ODIV3 OE[0]	ODIV4 OE[1]	ODIV4 OE[0]	CLK3 OE[1]	CLK3 OE[0]	CLK4 OE[1]	CLK4 OE[0]	50 00(26)
MUX1-6 State Setting									
06h	Reserved	Reserved	MUX1[2]	MUX1[1]	MUX1[0]	MUX2[2]	MUX2[1]	MUX2[0]	13
07h	Reserved	Reserved	MUX3[2]	MUX3[1]	MUX3[0]	MUX4[2]	MUX4[1]	MUX4[0]	18
08h	Reserved	Reserved	MUX5[2]	MUX5[1]	MUX5[0]	MUX6[2]	MUX6[1]	MUX6[0]	25
ODIV1-6 State Setting									
09h	ODIV1IN	ODIV1 RPLSEL	ODIV1 CNT64[5]	ODIV1 CNT64[4]	ODIV1 CNT64[3]	ODIV1 CNT64[2]	ODIV1 CNT64[1]	ODIV1 CNT64[0]	0A
0Ah	ODIV2IN	ODIV2 RPLSEL	ODIV2 CNT64[5]	ODIV2 CNT64[4]	ODIV2 CNT64[3]	ODIV2 CNT64[2]	ODIV2 CNT64[1]	ODIV2 CNT64[0]	0A
0Bh	Reserved	ODIV1 RPL[3]	ODIV1 RPL[2]	ODIV1 RPL[1]	ODIV1 RPL[0]	ODIV2 RPL[2]	ODIV2 RPL[1]	ODIV2 RPL[0]	00
0Ch	Reserved	ODIV3IN	ODIV3 CNT64[5]	ODIV3 CNT64[4]	ODIV3 CNT64[3]	ODIV3 CNT64[2]	ODIV3 CNT64[1]	ODIV3 CNT64[0]	09
0Dh	Reserved	ODIV4IN	ODIV4 CNT64[5]	ODIV4 CNT64[4]	ODIV4 CNT64[3]	ODIV4 CNT64[2]	ODIV4 CNT64[1]	ODIV4 CNT64[0]	0F
0Eh	ODIV5IN	ODIV5 RPLSEL	ODIV5 CNT64[5]	ODIV5 CNT64[4]	ODIV5 CNT64[3]	ODIV5 CNT64[2]	ODIV5 CNT64[1]	ODIV5 CNT64[0]	07
0Fh	ODIV6IN	ODIV6 RPLSEL	ODIV6 CNT64[5]	ODIV6 CNT64[4]	ODIV6 CNT64[3]	ODIV6 CNT64[2]	ODIV6 CNT64[1]	ODIV6 CNT64[0]	80
10h	Reserved	Reserved	Reserved	Reserved	ODIV5 RPL	ODIV6 RPL[2]	ODIV6 RPL[1]	ODIV6 RPL[0]	00
CLK1-6 Output State Setting									
11h	Reserved	Reserved	Reserved	Reserved	CLK1DL[1]	CLK1DL[0]	CLK2DL[1]	CLK2DL[0]	00
12h	CLK3DL[1]	CLK3DL[0]	CLK4DL[1]	CLK4DL[0]	CLK5DL[1]	CLK5DL[0]	CLK6DL[1]	CLK6DL[0]	00

Note
(26) CSET **pin** = ‘‘H’’

Generic Configuration Register

Address: 00h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Default	0	0	0	0	0	0	0	0

R/W: User arbitrarily programmable bits (D7 ~ D0)
User can freely program these bits if necessary.

Address: 01h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
01h	Reserved	RID[1]	RID[0]	PWDN	PLL1PD	PLL2PD	PLL3PD	PLL4PD
Default	0	0	0	0	1	1	1	1
CSET **pin** = ‘‘H’’	0	0	0	0	0	0	0	0

RID[1:0]: Device Identification *read only

Table 2. RID[1:0]: Device Identification

RID[1:0]	Device Identification
00	AK8147DV2 (Default)
01	N/A
10	N/A
11	N/A

PWDN: Device Power Down control

When set PWDN bit to “1”, only register can be controlled via I2C in the device. Register settings are not initialized at this moment.

Table 3. PWDN: Device Power Down control

PWDN	Device Setting
0	Device Active
1	Device Power down *1

*1 CLKnOE[1:0] (Address: 04h ~ 05h) is set to except ‘‘00’’.

PLLnPD : PLL1-4 Power Down control

Table 4. PWDN: Device Power Down control

PLLnPD	PLLn Setting
0	Power down release
1	Power down

Address: 02h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
02h	INSEL	PDIOSC	ODIV1RST	ODIV2RST	ODIV3RST	ODIV4RST	ODIV5RST	ODIV6RST
Default	0	0	1	1	1	1	1	0
CSET **pin** = "H"	0	0	0	1	0	0	0	0

INSEL : Input Clock Select

Table 5. INSEL: Input Clock Select

INSEL	Device Setting
0	Normal （XO circuit）
1	XO Power down（MUX7）

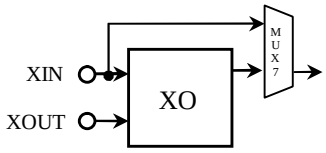


Figure 13 input clock select

PDIOSC: Crystal Oscillator Circuit Enable/Disable Setting

Table 6. PDIOSC: Crystal Oscillator Circuit Enable/Disable Setting

OSC_DIS	Crystal Oscillator Circuit State
0	Enable (Crystal Connection)
1	Disable (Ext-in : External Clock Signal Input)

ODIVnRST: ODIVn Reset Control

Table 7. ODIVnRST: ODIVn Reset Control

ODIVnRST	ODIVn Reset Control
0	Reset release
1	Reset

(n = 1-6)

Address: 03h – 05h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
03h	ODIV1 OE[1]	ODIV1 OE[0]	ODIV2 OE[1]	ODIV2 OE[0]	ODIV5 OE[1]	ODIV5 OE[0]	ODIV6 OE[1]	ODIV6 OE[0]
Default	0	1	0	1	0	1	0	0
CSET **pin** = "H"	0	0	0	1	0	0	0	0
04h	CLK1 OE[1]	CLK1 OE[0]	CLK2 OE[1]	CLK2 OE[0]	CLK5 OE[1]	CLK5 OE[0]	CLK6 OE[1]	CLK6 OE[0]
Default	0	0	0	0	0	0	0	0
05h	ODIV3 OE[1]	ODIV3 OE[0]	ODIV4 OE[1]	ODIV4 OE[0]	CLK3 OE[1]	CLK3 OE[0]	CLK4 OE[1]	CLK4 OE[0]
Default	0	1	0	1	0	0	0	0
CSET **pin** = "H"	0	0	0	0	0	0	0	0

CLKnOE [1:0]：CLKn Output State Setting

CLKnOE [1:0] bits setting is prior to ODIVnOE [1:0] setting for output state definition.

Table 8. CLK1-6 Output State Definition

CLKnOE [1:0]	CLKn Output State
00	CLK Enable
01	Disable to Low
10	Disable to High
11	Disable to Hi-z

(n = 1-6)

ODIVnOE [1:0]：ODIVn Output State Setting

Glitch free control function is enabled when CLKnOE [1:0] = "00"

Table 9. ODIVn Output State Definition

ODIVnOE [1:0]	ODIVn Output State
00	ODIVn output Enable
01	Disable to Low
10	Disable to High
11	Prohibited

(n = 1-6)

Address: 06h – 08h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
06h	Reserved	Reserved	MUX1[2]	MUX1[1]	MUX1[0]	MUX2[2]	MUX2[1]	MUX2[0]
Default	0	0	0	1	0	0	1	1
07h	Reserved	Reserved	MUX3[2]	MUX3[1]	MUX3[0]	MUX4[2]	MUX4[1]	MUX4[0]
Default	0	0	0	1	1	0	0	0
08h	Reserved	Reserved	MUX5[2]	MUX5[1]	MUX5[0]	MUX6[2]	MUX6[1]	MUX6[0]
Default	0	0	1	0	0	1	0	1

MUXn[2:0]: ODIV1-6 Select

Unselected ODIVn is recommended to be set ODIVnRST = “1” (n=1-6)

Table 10. ODIV1-6 Select

MUXn[2:0]	ODIVn
000	ODIV1
001	ODIV2
010	ODIV3
011	ODIV4
100	ODIV5
101	ODIV6
110	Prohibited
111	Prohibited

(n = 1-6)

Address: 09h ~ 10h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
09h	ODIV1IN	ODIV1 RPLSEL	ODIV1 CNT64[5]	ODIV1 CNT64[4]	ODIV1 CNT64[3]	ODIV1 CNT64[2]	ODIV1 CNT64[1]	ODIV1 CNT64[0]
Default	0	0	0	0	1	0	1	0
0Ah	ODIV2IN	ODIV2 RPLSEL	ODIV2 CNT64[5]	ODIV2 CNT64[4]	ODIV2 CNT64[3]	ODIV2 CNT64[2]	ODIV2 CNT64[1]	ODIV2 CNT64[0]
Default	0	0	0	0	1	0	1	0
0Bh	Reserved	ODIV1 RPL[3]	ODIV1 RPL[2]	ODIV1 RPL[1]	ODIV1 RPL[0]	ODIV2 RPL[2]	ODIV2 RPL[1]	ODIV2 RPL[0]
Default	0	0	0	0	0	0	0	0
0Ch	Reserved	ODIV3IN	ODIV3 CNT64[5]	ODIV3 CNT64[4]	ODIV3 CNT64[3]	ODIV3 CNT64[2]	ODIV3 CNT64[1]	ODIV3 CNT64[0]
Default	0	0	0	0	1	0	0	1
0Dh	Reserved	ODIV4IN	ODIV4 CNT64[5]	ODIV4 CNT64[4]	ODIV4 CNT64[3]	ODIV4 CNT64[2]	ODIV4 CNT64[1]	ODIV4 CNT64[0]
Default	0	0	0	0	1	1	1	1
0Eh	ODIV5IN	ODIV5 RPLSEL	ODIV5 CNT64[5]	ODIV5 CNT64[4]	ODIV5 CNT64[3]	ODIV5 CNT64[2]	ODIV5 CNT64[1]	ODIV5 CNT64[0]
Default	0	0	0	0	0	1	1	1
0Fh	ODIV6IN	ODIV6 RPLSEL	ODIV6 CNT64[5]	ODIV6 CNT64[4]	ODIV6 CNT64[3]	ODIV6 CNT64[2]	ODIV6 CNT64[1]	ODIV6 CNT64[0]
Default	1	0	0	0	0	0	0	0
10h	Reserved	Reserved	Reserved	Reserved	ODIV5 RPL	ODIV6 RPL[2]	ODIV6 RPL[1]	ODIV6 RPL[0]
Default	0	0	0	0	0	0	0	0

ODIVnIN : ODIVn Input Clock Select

Table 11. ODIVn Input Clock Select

ODIVnIN	ODIVn Input Clock Select
0	PLL Output
1	XO output or External Input

(n = 1-6)

ODIVnCNT64 [5:0] : ODIVn Divider A control / setting

Table 12. ODIVn Divider A setting

ODIVnCNT64 [5:0]	ODIVn Divider A value
000000	2
000001	
000010	3
000011	4
:	:
000111	64

(n = 1-6)

ODIVnRPLSEL : ODIVn Divider B control

Table 13. ODIVn Divider B control

ODIVnRPLSEL	ODIVn Divider B control
0	Bypass
1	Select

(n = 1, 2, 5, 6)

ODIV1RPL [3:0] : ODIV1 Divider B

Table 14. ODIV1 Divider B value

ODIV1RPL [3:0]	ODIV1 Divider B
0000	2
0001	4
0010	8
:	:
1111	65536

ODIVnRPL [2:0] : ODIVn Divider B

Table 15. ODIV2,6 Divider B value

ODIV2, 6RPL [2:0]	ODIVn Divider B
000	2
001	4
010	8
:	:
111	256

(n = 2, 6)

ODIV5RPL [3:0] : ODIV5 Divider B

Table 16. ODIV5 Divider B value

ODIV5RPL [3:0]	ODIV5 Divider B
0	2
1	4

Address: 11h – 12h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
11h	Reserved	Reserved	Reserved	Reserved	CLK1 DL[1]	CLK1 DL[0]	CLK2 DL[1]	CLK2 DL[0]
Default	0	0	0	0	0	0	0	0
12h	CLK3 DL[1]	CLK3 DL[0]	CLK4 DL[1]	CLK4 DL[0]	CLK5 DL[1]	CLK5 DL[0]	CLK6 DL[1]	CLK6 DL[0]
Default	0	0	0	0	0	0	0	0

CLKnDL [1:0] : CLKn Drive Level Setting

Table 17. CLK1-6 Drive Level Setting

CLKnDL [1:0]	Device condition
00	High Drive
01	Middle High Drive
10	Middle Low Drive
11	Low Drive

(n = 1-6)

Table 18. Output Frequency @ Drive Level Setting

Parameter	Output Load Cap	Drive Level Setting				note
		00	01	10	11	
Output Frequency	10pF	148.5MHz	50MHz	30MHz	16MHz	VDDOn =1.8V
	15pF	100MHz	40MHz	27MHz	13MHz	
	25pF	75MHz	20MHz	18MHz	8MHz	
	10pF	148.5MHz	80MHz	50MHz	30MHz	VDDOn =3.3V
	15pF	140MHz	70MHz	40MHz	27MHz	
	25pF	120MHz	40MHz	27MHz	16MHz	

■ **PLL1 Configuration Register (Address: 20h ~ 24h)**

Address	Data								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
PLL1 Frequency Selection									
20h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO1 _RANGE	MDIV1[1]	MDIV1[0]	05
PLL1_0 NDIV1 Integral Part Setting									
21h	INT1[7]	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]	1F
PLL1_0 NDIV1 Fractional Part Setting									
22h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC1[17]	FRAC1[16]	01
23h	FRAC1[15]	FRAC1[14]	FRAC1[13]	FRAC1[12]	FRAC1[11]	FRAC1[10]	FRAC1[9]	FRAC1[8]	41
24h	FRAC1[7]	FRAC1[6]	FRAC1[5]	FRAC1[4]	FRAC1[3]	FRAC1[2]	FRAC1[1]	FRAC1[0]	24

PLL1 Configuration Register

PLL1 Block Diagram is as the following Figure.
Set PLL1 parameter according to Frequency Setting Procedure on page 12.

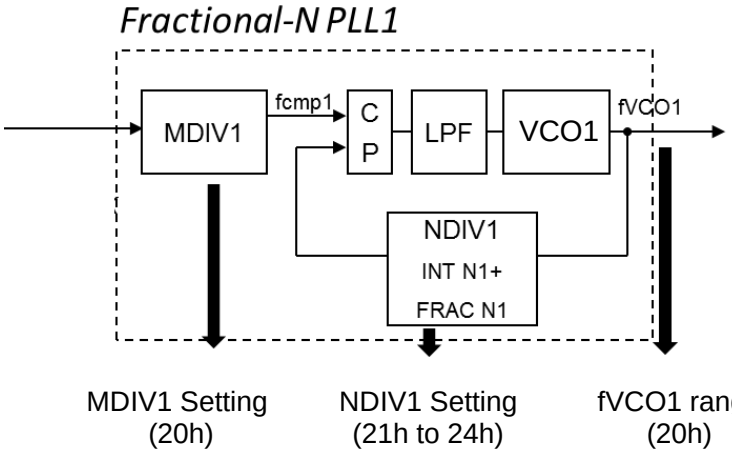


Figure 14. PLL1 Block Diagram

Address: 20h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO1 _RANGE	MDIV1[1]	MDIV1[0]
Default	0	0	0	0	0	1	0	1

VCO1_RANGE: fVCO1 range select

"VCO1_RANGEn[1:0]" selects the fVCO1 frequency range. fVCO1 frequency can be set according to Frequency Setting Procedure on page 14.

Table 19. fVCO1 range setting

VCO1_RANGEn[1:0]	fVCO1 range
0	216MHz ≤ fvco < 324MHz
1	324MHz ≤ fvco ≤ 432MHz

MDIV1 [1:0] : MDIV1 Divider

Table 20. MDIV1 Divider

ODIV1RPL [3:0]	MDIV1 Divider
00	1
01	2
10	4
11	8

Address: 21h PLL1 Input Clock Selection / fVCO1 range

Address [Hex]	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
21	INT1[7]	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]
Default	0	0	0	1	1	1	1	1

INT1 [7:0]: NDIV1 integral part setting

NDIV1 Integral part can be set according to Frequency Setting Procedure on page 14.
INT1[7:0] must be set from "00001111" to "10011001", when PLL1 is used.

Table 21. NDIV1 integral part setting

INTn [6:0]	integral part
0000 0000 ~ 0000 1110	Prohibited
0000 1111	15
0001 0000	16
:	:
1001 1000	152
1001 1001	153
1001 1010 ~ 1111 1111	Prohibited

Address: 22h ~ 24h, NDIV1 fractional part setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
22h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC1[17]	FRAC1[16]
Default	0	0	0	0	0	0	0	1
23h	FRAC1[15]	FRAC1[14]	FRAC1[13]	FRAC1[12]	FRAC1[11]	FRAC1[10]	FRAC1[9]	FRAC1[8]
Default	0	1	0	0	0	0	0	1
24h	FRAC1[7]	FRAC1[6]	FRAC1[5]	FRAC1[4]	FRAC1[3]	FRAC1[2]	FRAC1[1]	FRAC1[0]
Default	0	0	1	0	0	1	0	0

FRAC1 [17:0]: NDIV1 fractional part setting

When a Certain Setting is set by three Address, write the data to all Address.
FRACn[17:0] settings are updated after writing register 24h.
Setting procedure should be (1)22h , (2)23h, and then (3)24h.

NDIV1 fractional part can be set according to Frequency Setting Procedure on page 14.
Fractional part of N is expressed by A/218. Here, the numerator A is defined by FRAC bits. FRAC is treated as 2's Complement which is able to set from -217 up to +217. Consequently, it is possible to set from -0.5 to +0.5 for fractional part of N.

Table 22. NDIV1 fractional part setting (n = 0, 1)

FRACn [17:0]	A	Fractional Part
01 1111 1111 1111 1111	+131071	0.49999619..
01 1111 1111 1111 1110	+131070	0.49999237..
: 01 0000 0000 0000 0000 :	: +65536 :	: 0.25 :
00 0000 0000 0000 0001	+1	0.00000381..
00 0000 0000 0000 0000	0	0
11 1111 1111 1111 1111	-1	-0.00000381..
11 1111 1111 1111 1110	-2	
: 11 0000 0000 0000 0000 :	: -65536 :	: -0.25 :
10 0000 0000 0000 0001	-131071	-0.49999619..
10 0000 0000 0000 0000	-131072	-0.5

■ **PLL2-4 Configuration Register (Address: 30h ~ 34h, 40h ~ 44h, 50h ~ 54h,)**

Address	Data								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
PLL2 VCO Range, MDIV2									
30h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO2 _RANGE	MDIV2[1]	MDIV2[0]	01
PLL2 NDIV Integral Part Setting									
31h	INT2[7]	INT2[6]	INT2[5]	INT2[4]	INT2[3]	INT2[2]	INT2[1]	INT2[0]	12
PLL2 NDIV Fractional Part Setting									
32h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME2[8]	NUME2[7]	02
33h	NUME2[6]	NUME2[5]	NUME2[4]	NUME2[3]	NUME2[2]	NUME2[1]	NUME2[0]	DENO2[8]	4D
34h	DENO2[7]	DENO2[6]	DENO2[5]	DENO2[4]	DENO2[3]	DENO2[2]	DENO2[1]	DENO2[0]	45
PLL3 VCO Range, MDIV3									
40h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO3 _RANGE	MDIV3[1]	MDIV3[0]	05
PLL3 NDIV Integral Part Setting									
41h	INT3[7]	INT3[6]	INT3[5]	INT3[4]	INT3[3]	INT3[2]	INT3[1]	INT3[0]	21
PLL3 NDIV Fractional Part Setting									
42h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME3[8]	NUME3[7]	00
43h	NUME3[6]	NUME3[5]	NUME3[4]	NUME3[3]	NUME3[2]	NUME3[1]	NUME3[0]	DENO3[8]	06
44h	DENO3[7]	DENO3[6]	DENO3[5]	DENO3[4]	DENO3[3]	DENO3[2]	DENO3[1]	DENO3[0]	0D
PLL VCO Range, MDIV4									
50h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO4 _RANGE	MDIV4[1]	MDIV4[0]	05
PLL4 NDIV Integral Part Setting									
51h	INT4[7]	INT4[6]	INT4[5]	INT4[4]	INT4[3]	INT4[2]	INT4[1]	INT4[0]	1D
PLL4 NDIV Fractional Part Setting									
52h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME4[8]	NUME4[7]	00
53h	NUME4[6]	NUME4[5]	NUME4[4]	NUME4[3]	NUME4[2]	NUME4[1]	NUME4[0]	DENO4[8]	0E
54h	DENO4[7]	DENO4[6]	DENO4[5]	DENO4[4]	DENO4[3]	DENO4[2]	DENO4[1]	DENO4[0]	0D

PLL2-4 Configuration Register

PLL2-4 Block Diagram is as the following Figure.
Set PLL2-4 parameter according to. Frequency Setting Procedure on page 13.

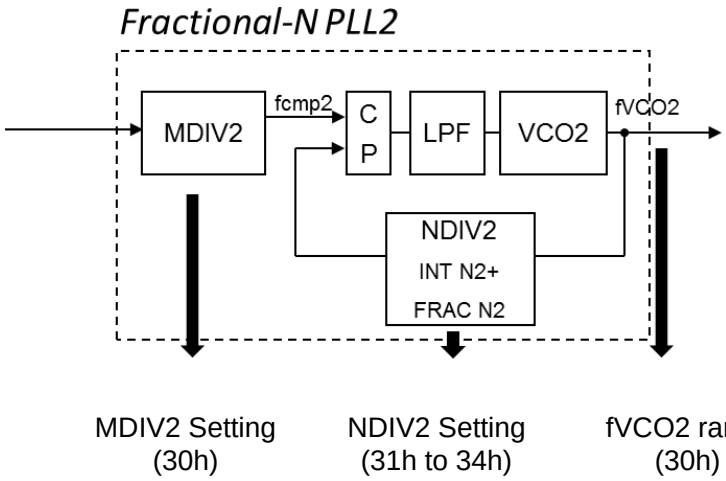


Figure 15. PLL2 Block Diagram

Address: 30h, 40h, 50h, PLL2-4 Output Frequency selection

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO2 _RANGE	MDIV2[1]	MDIV2[0]
Default	0	0	0	0	0	0	0	1
40h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO3 _RANGE	MDIV3[1]	MDIV3[0]
Default	0	0	0	0	0	1	0	1
50h	Reserved	Reserved	Reserved	Reserved	Reserved	VCO4 _RANGE	MDIV4[1]	MDIV4[0]
Default	0	0	0	0	0	1	0	1

VCOn_RANGE [1:0]: PLLn VCO range setting (n = 2-4)

"VCO2_RANGEn[1:0]" selects the fVCO2 frequency range. fVCO2 frequency can be set according to Frequency Setting Procedure on page 16.

Table 23. fVCO2 range selection (n = 0, 1)

VCOn_RANGE[1:0]	fVCO1 range
0	216MHz ≤ fvco < 324MHz
1	324MHz ≤ fvco ≤ 432MHz

MDIVn [1:0] : MDIVn Divider

Table 24. MDIVn Divider

MDIVn [1:0]	MDIVn Divider
00	1
01	2
10	4
11	8

Address: 31h, 41h, 51h, NDIVn Divider

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
31h	INT2[7]	INT2[6]	INT2[5]	INT2[4]	INT2[3]	INT2[2]	INT2[1]	INT2[0]
Default	0	0	0	1	0	0	1	0
41h	INT3[7]	INT3[6]	INT3[5]	INT3[4]	INT3[3]	INT3[2]	INT3[1]	INT3[0]
Default	0	0	1	0	0	0	0	1
51h	INT4[7]	INT4[6]	INT4[5]	INT4[4]	INT4[3]	INT4[2]	INT4[1]	INT4[0]
Default	0	0	0	1	1	1	0	1

(n = 0, 1)

NDIVn divider can be set according to Frequency Setting Procedure on page 16.
NDIVn Divider is decided by setting NINTn, NUMEn and DENOn.

INTn [7:0]: NDIV1 integral part setting

NDIV1 Integral part can be set according to Frequency Setting Procedure on page 14.
INTn [7:0] must be set from “00001111” to “10011001”, when PLLn is used.

Table 25. NDIVn integral part setting

INTn [7:0]	Integral part
0000 0000 ~ 0000 1110	Prohibited
0000 1111	15
0001 0000	16
:	:
1001 1000	152
1001 1001	153
1001 1010 ~ 1111 1111	Prohibited

Address: 32h ~ 34h, 42h ~ 44h, 52h ~ 54h, NDIVn fractional part setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
32h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME2[8]	NUME2[7]
Default	0	0	0	0	0	0	1	0
33h	NUME2[6]	NUME2[5]	NUME2[4]	NUME2[3]	NUME2[2]	NUME2[1]	NUME2[0]	DENO2[8]
Default	0	1	0	0	1	1	0	1
34h	DENO2[7]	DENO2[6]	DENO2[5]	DENO2[4]	DENO2[3]	DENO2[2]	DENO2[1]	DENO2[0]
Default	0	1	0	0	0	1	0	1
42h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME3[8]	NUME3[7]
Default	0	0	0	0	0	0	0	0
43h	NUME3[6]	NUME3[5]	NUME3[4]	NUME3[3]	NUME3[2]	NUME3[1]	NUME3[0]	DENO3[8]
Default	0	0	0	0	0	1	1	0
44h	DENO3[7]	DENO3[6]	DENO3[5]	DENO3[4]	DENO3[3]	DENO3[2]	DENO3[1]	DENO3[0]
Default	0	0	0	0	1	1	0	1
52h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUME4[8]	NUME4[7]
Default	0	0	0	0	0	0	0	0
53h	NUME4 [6]	NUME4 [5]	NUME4 [4]	NUME4 [3]	NUME4 [2]	NUME4 [1]	NUME4 [0]	DENO4 [8]
Default	0	0	0	0	1	1	1	0
54h	DENO4 [7]	DENO4 [6]	DENO4 [5]	DENO4 [4]	DENO4 [3]	DENO4 [2]	DENO4 [1]	DENO4 [0]
Default	0	0	0	0	1	1	0	1

NUMEn[8:0]: NDIVn Numerator of fractional part setting (n = 2, 3, 4)

Table 26. NDIVn Numerator of fractional part setting (n = 2, 3, 4)

NUMEn[8:0]	NDIVn Numerator of fractional part setting
000000000	0 (Integer-N Mode)
000000001	1
:	:
111111110	510
111111111	511

DENOn[8:0]: NDIVn Denominator of fractional part setting (n = 2, 3, 4)

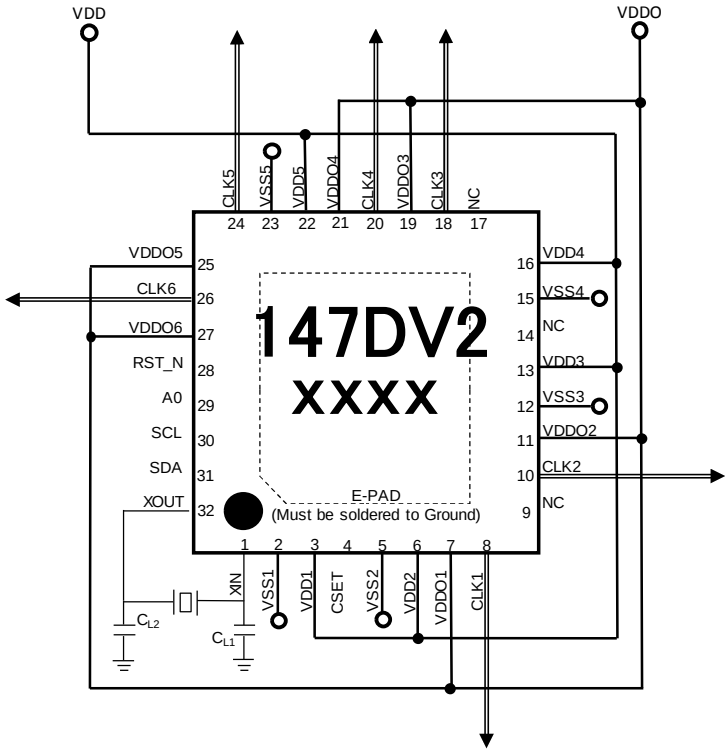
DENOn[8:0] must be set from “000000001” to “111111111”, when PLL2 is used.

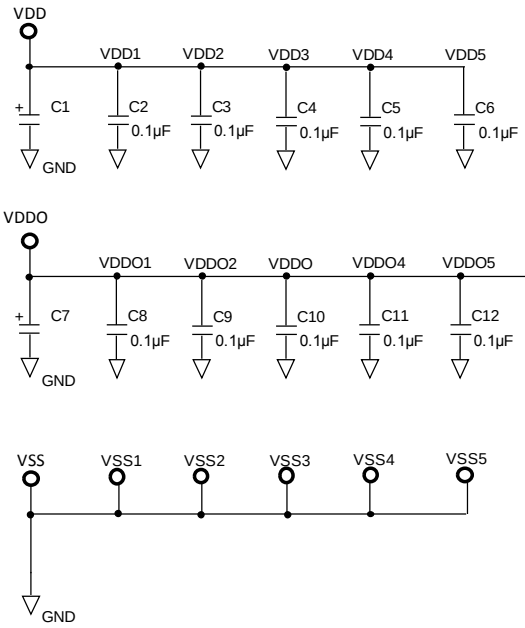
Table 27. NDIVn Denominator of fractional part setting (n = 2, 3, 4)

DENOn[8:0]	NDIVn Denominator of fractional part setting
000000000	Prohibited
000000001	1
:	:
111111110	510
111111111	511

10. Recommended External Circuits

Typical Connection Diagram





Crystal Unit

Recommends the following device or its equivalents

Table 29. Parameter List

NIHON DEMPA KOGYO CO., LTD
NX3225GA 26.000MHz / CHP-CRG-13

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Nominal frequency	f0		26.000		MHz	
Package Size (L x W x H)	-		3.2 x 2.5 x 0.75		mm	
Overtone order	-		Fundamental			at 25°C
Frequency tolerance	-	-20	-	+20	ppm	
Frequency versus Temperature Characteristics	-	-30	-	+30	ppm	with reference to 25°C
Operating Temperature Range	-	-40	-	+85	°C	
Equivalent Series Resistance	R1	-	-	50	Ω	
Level of Drive	-	-	10	200	μW	
Load Capacitance	C_L	-	8	-	pF	

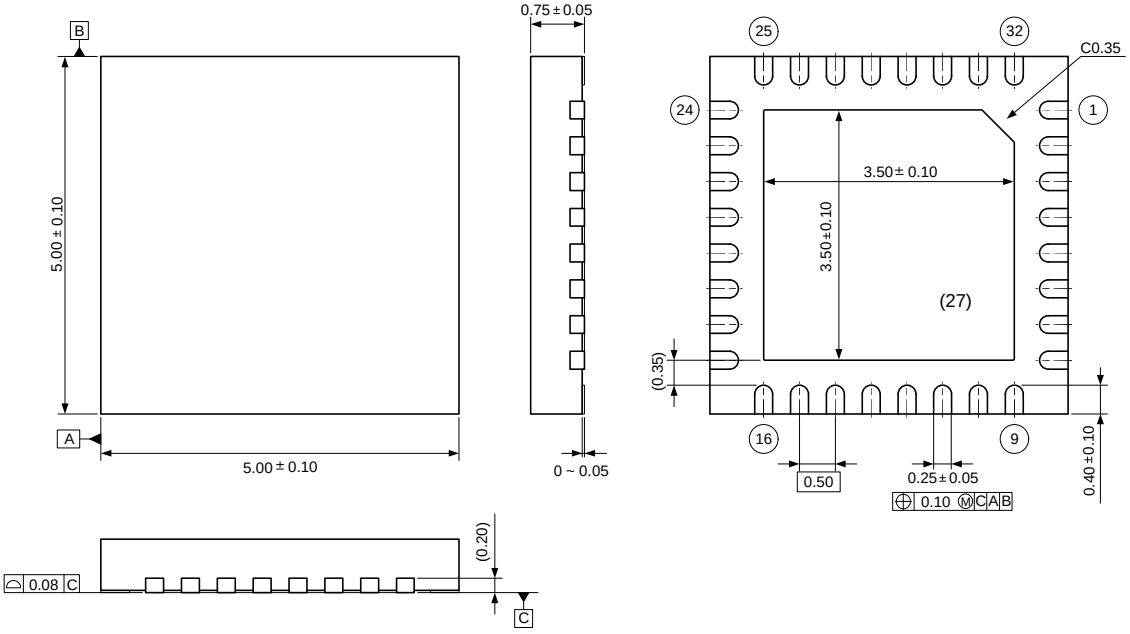
NIHON DEMPA KOGYO CO., LTD
NX3225GA 20.000MHz / CHP-CRG-14

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Nominal frequency	f0		20.000		MHz	
Package Size (L x W x H)	-		3.2 x 2.5 x 0.75		mm	
Overtone order	-		Fundamental			at 25°C
Frequency tolerance	-	-20	-	+20	ppm	
Frequency versus Temperature Characteristics	-	-30	-	+30	ppm	with reference to 25°C
Operating Temperature Range	-	-40	-	+85	°C	
Equivalent Series Resistance	R1	-	-	50	Ω	
Level of Drive	-	-	10	200	μW	
Load Capacitance	C_L	-	8	-	pF	

11. Package

■ Outline Dimensions

32-pin QFN (Unit : mm)



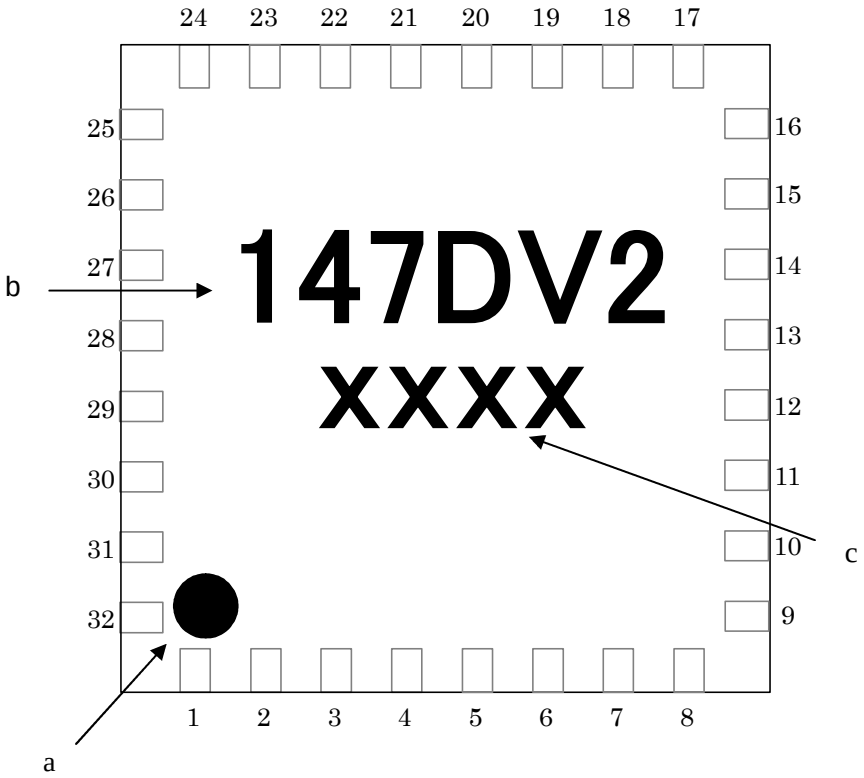
Note:
(27) The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material

Package molding compound : Epoxy (Halogen – free)
Lead Frame : Copper Alloy
Pin surface treatment : 100% Sn

■ **Marking**

a: #1 Pin Index
b: Part number : 147DV2
c: Date code (4 digits)



12. Ordering Guide

■ **Ordering Guide**

AK8147DV2	–40 ~ +105°C	32-pin HLQFN (0.5mm pitch)
AKD8147DV2	Evaluation Board for the AK8147DV2	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/11/21	00	First Edition		

Important Notice

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