AK8157A

Multiclock Generator for Premium Audio Device

1. General Description

The AK8157A is a member of AKM's low power multi clock generator family designed for a high quality premium audio clock with high performance C/N. For example, The AK8157A is recommended to use with a premium DAC, the AK4490. The PLL circuits of the AK8157A are developed by AKM's long-term-experienced clock device technology, enabling low jitter clock outputs while achieving very low current consumption. The AK8157A generates different frequency clocks (Master Clock, Bit Clock, L/R Clock) from external clock input, providing up to three outputs configured by register-setting. The AK8157A is available in a 16-pin WLCSP package.

Application: Smart Cellular Phones, USB DACs, USB Headphones, Bluetooth Headphones

2. Features

- **External Clock Input Frequency: 9.6MHz**
- **Three Frequency Selectable Clock Outputs**
- **Selectable Clock Output Frequencies:**
  - **MCLK: 16.384, 22.5792, 24.576MHz**
  - **BCLK: 2.048MHz ~ 24.576MHz**
  - **LRCK: 32kHz ~ 384kHz**
- **Selectable Clock Output Enable / Disable Control**
- **Low Jitter Performance**
  - **RMS Jitter: 45ps (10Hz ~ 5MHz)**
- **Low Current Consumption: 8mA (VDD1-4 = 1.8V)**
- **Output Load: 80pF**
- **Power Supply: VDD1-4 = 1.7 ~ 2.0V**
- **Digital Input Level: CMOS**
- **Package: 16-pin WLCSP**

3. Table of Contents

4. Block Diagram

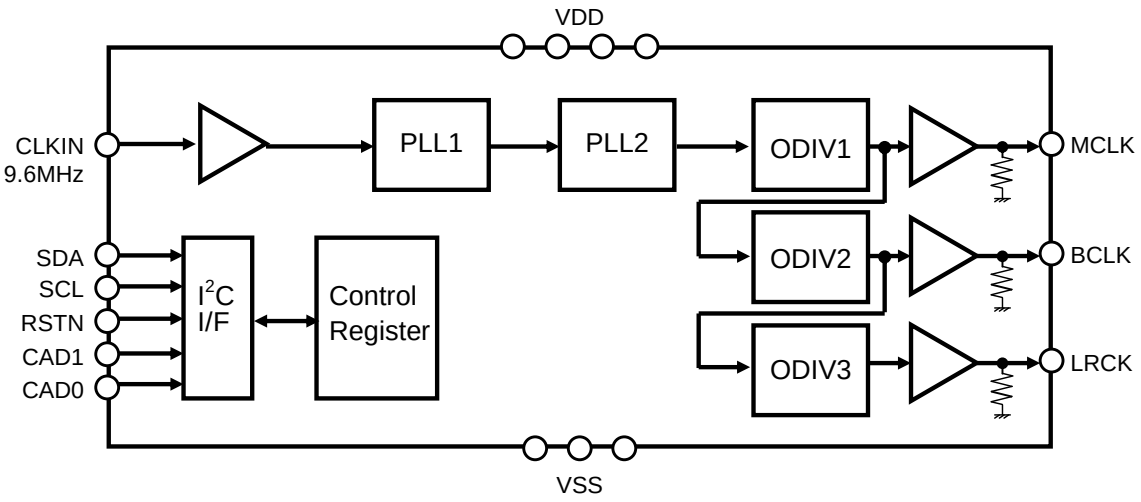


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Layout

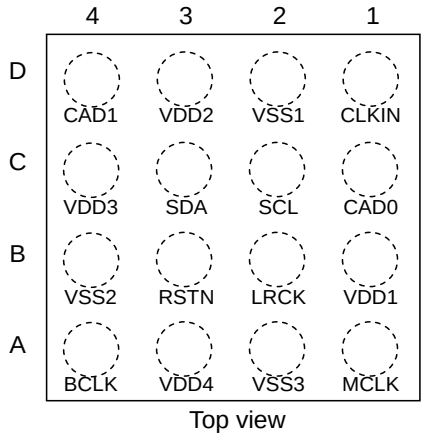


Figure 2. AK8157A Package: 16-pin WLCSP (Top View)

■ Pin Functions

No.	Pin Name	I/O	Function
A1	MCLK	O	Master Clock Output Pin (Internal pull-down pin: 160kΩ)
A2	VSS3	-	Ground Pin
A3	VDD4	-	Power Supply Pin, 1.7 ~ 2.0V
A4	BCLK	O	Audio Serial Data Clock Output Pin (Internal pull-down pin: 160kΩ)
B1	VDD1	-	Power Supply Pin, 1.7 ~ 2.0V
B2	LRCK	O	L/R Clock Output Pin (Internal pull-down pin: 160kΩ)
B3	RSTN	I	Register Reset Control Pin When at "L", the register of the AK8157A is held in reset. The AK8157A must always be reset upon power-up.
B4	VSS2	-	Ground Pin
C1	CAD0	I	Chip Address 0 Pin
C2	SCL	I	Control Data Clock Input Pin
C3	SDA	I/O	Control Data Input / Output Pin
C4	VDD3	-	Power Supply Pin, 1.7 ~ 2.0V
D1	CLKIN	I	9.6MHz External Clock Input Pin
D2	VSS1	-	Ground Pin
D3	VDD2	-	Power Supply Pin, 1.7 ~ 2.0V
D4	CAD1	I	Chip Address 1 Pin

Note: All input pins must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Digital	MCLK, BCLK, LRCK	These pins must be connected to VSS1-3 or open. When these pins are in disable setting, they output “L” with internal pull-down resistor.

Pull-down pin List

pull-down pin	A1, A4, B2

6. Absolute Maximum Ratings

(VSS1-3 = 0V; Note 1)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	VDD1-4	VDD	−0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	VSS−0.3	VDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.

Note 2. Connect at least 0.1μF or more decoupling capacitors between VDD1-4 and VSS1-3 to suppress affections by a static electricity noise or an over voltage (includes over shooting) that exceeds absolute maximum ratings.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1-3 = 0V; Note 1)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Power Supplies	(Note 3)	VDD1-4	VDD	1.7	1.8	2.0	V

Note 1. All voltages with respect to ground.

Note 3. VDD1-4 should be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be connected close to each VDD pin. The power-up sequence between VDD1-4 are not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ AC Characteristics

(Ta=25°C; VDD1-4 = 1.7 ~ 2.0V; unless otherwise specified.)

Parameter	Pin	Min.	Typ.	Max.	Unit
Input Clock Frequency	CLKIN	-	9.6	-	MHz
Input Capacitance	CLKIN	-	3	-	pF
Output Clock Frequency	MCLK BCLK LRCK	16.384 2.048 32	- - -	24.576 24.576 384	MHz MHz kHz
Output Clock Rise / Fall Time (Note 4)	MCLK BCLK LRCK	-	6	12	ns
RMS Jitter (10Hz ~ 5MHz)	MCLK	-	25	-	ps
Output Clock Duty Cycle (Note 5)	MCLK BCLK LRCK	45	50	55	%
Output High / Low Pulse Width (Note 6)	MCLK BCLK LRCK	10	-	-	ns
Output Lock Time (Note 7)	MCLK BCLK LRCK	-	-	1	ms
BICK "↑" to LRCK Edge (tBLR) (Note 8) (BCLK = 2.048MHz ~ 12.288MHz) (BCLK = 16.384MHz ~ 24.576MHz)	BCLK LRCK	 20 10	 - -	 - -	 ns ns
LRCK Edge to BICK "↑" (tLRB) (Note 8) (BCLK = 2.048MHz ~ 12.288MHz) (BCLK = 16.384MHz ~ 24.576MHz)	BCLK LRCK	 20 10	 - -	 - -	 ns ns

Note 4. Rise Time = 20%VDD to 80%VDD, Fall Time = 80%VDD to 20%VDD Measured with Load Capacitance of CL = 80pF.
Note 5. Measured with Load Capacitance of CL = 80pF.
Note 6. High Pulse Width is measured at 80%VDD Level, Low Pulse Width is measured at 20%VDD Level, Measured with Load Capacitance of CL = 80pF.
Note 7. The time until the output settles to ±0.1% of the specified frequency from the point that the power supply reaches VDD.
Note 8. BCLK rising edge must not occur at the same time as LRCK edge.

■ Power Supply Current

(Ta=25°C; VDD1-4 = 1.7 ~ 2.0V; unless otherwise specified.)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current:				
Normal operation (Note 9) (VREF_PD bit = PLL_PD bit = PLL1_PD bit = "L") VDD1-4	-	8	13	mA
Power down (Note 10) (VREF_PD bit = PLL_PD bit = PLL1_PD bit = "H") VDD1-4	-	0	10	μA

Note 9. CLKIN = 9.6MHz, MCLK = 24.576MHz, BCLK = 24.576MHz, LRCK = 384kHz. No Output Load Capacitance. MDSEL1-0 bits = MCKSEL1-0 bits = "11".

Note 10. In the power down mode. VREF_PD bit = PLL_PD bit = PLL1_PD bit = "H", and all other digital input pins including CLKIN pin are held VSS1-3.

■ DC Characteristics

(Ta=25°C; VDD1-4 = 1.7 ~ 2.0V; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage	VIH	80%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%VDD	V
High-Level Output Voltage (Iout = –4mA)	VOH	80%VDD	-	-	V
Low-Level Output Voltage					
(MCLK, BCLK, LRCK pins: Iout = 4mA)	VOL	-	-	20%VDD	V
(SDA pin: Iout = 3mA)	VOL	-	-	20%VDD	V
Input Leakage Current	Iin	-	-	±10	μA
Output Hi-z Leakage Current	Iout	–10	+11	+80	μA

■ **Switching Characteristics**

(Ta=25°C; VDD1-4 = 1.7 ~ 2.0V; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 11)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
RSTN Pulse Width (Note 12)	tRST	150			ns

Note 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 12. The register of the AK8157A can be reset by bringing the RSTN pin to “L”.

■ **Timing Diagram**

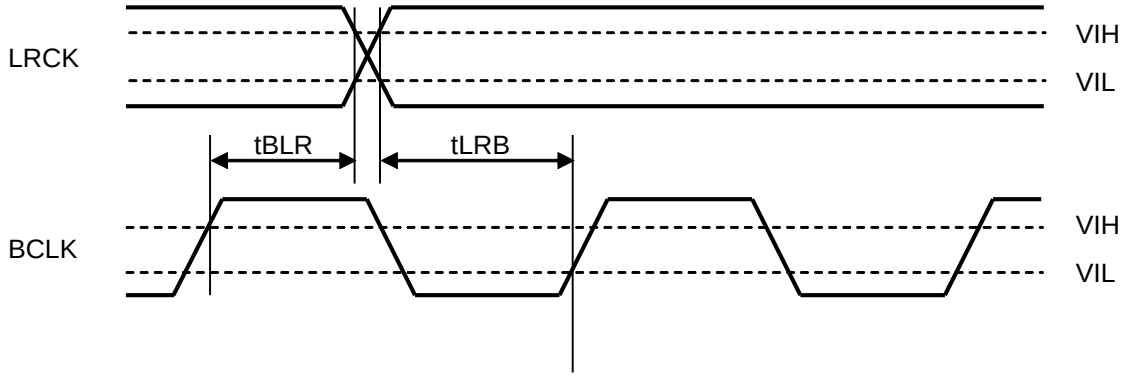


Figure 3. Audio Interface Timing

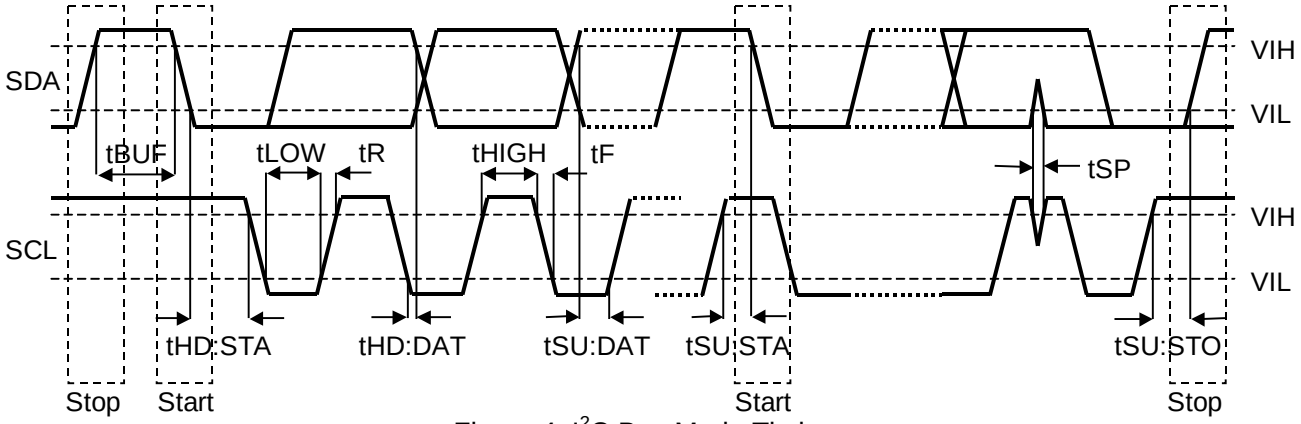


Figure 4. I^2C Bus Mode Timing

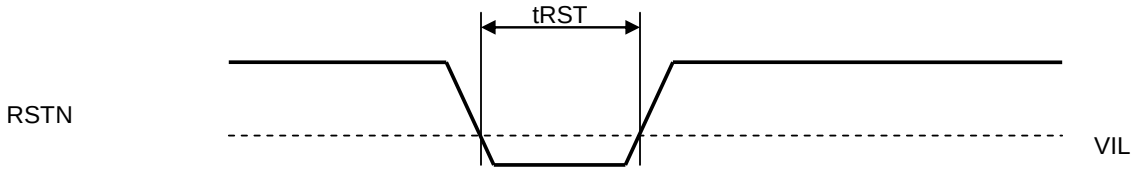


Figure 5. Reset Timing

9. Functional Descriptions

■ System Clock Timing

The AK8157A can generate MCLK, BCLK and LRCK simultaneously from 9.6MHz external input clock. It requires operating the AK8157A with an audio device such as the AK4490, the AK4495 and so on. MCLK, BCLK and LRCK phases are synchronized on a falling edge. (Figure 6).

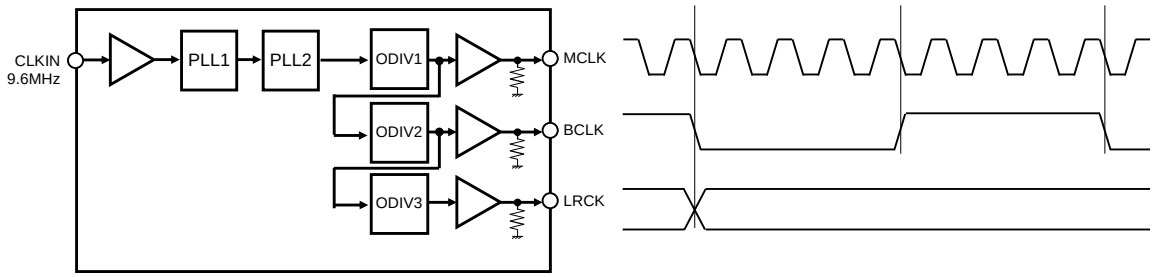


Figure 6. System Clock Timing

The MCLK, BCLK and LRCK frequencies corresponding to each sampling speed can be selected by MDSEL1-0 bits and MCKSEL1-0 bits (Table 1). Normal speed, double speed, quad speed and oct speed modes are available with the AK8157A.

Table 1. Output Clock Configuration

MDSEL1-0 bits	MCKSEL1-0 bits	MCLK (MHz)		BCLK (MHz)	LRCK (kHz)	Sampling Speed
				64fs	fs	
00	00	16.384	512fs	2.048	32	Normal
	01	22.5792		2.8224	44.1	
	10 / 11	24.576		3.072	48	
01	00	16.384	256fs	4.096	64	Double
	01	22.5792		5.6448	88.2	
	10 / 11	24.576		6.144	96	
10	00	16.384	128fs	8.192	128	Quad
	01	22.5792		11.2896	176.4	
	10 / 11	24.576		12.288	192	
11	00	16.384	64fs	16.384	256	Oct
	01	22.5792		22.5792	352.8	
	10 / 11	24.576		24.576	384	

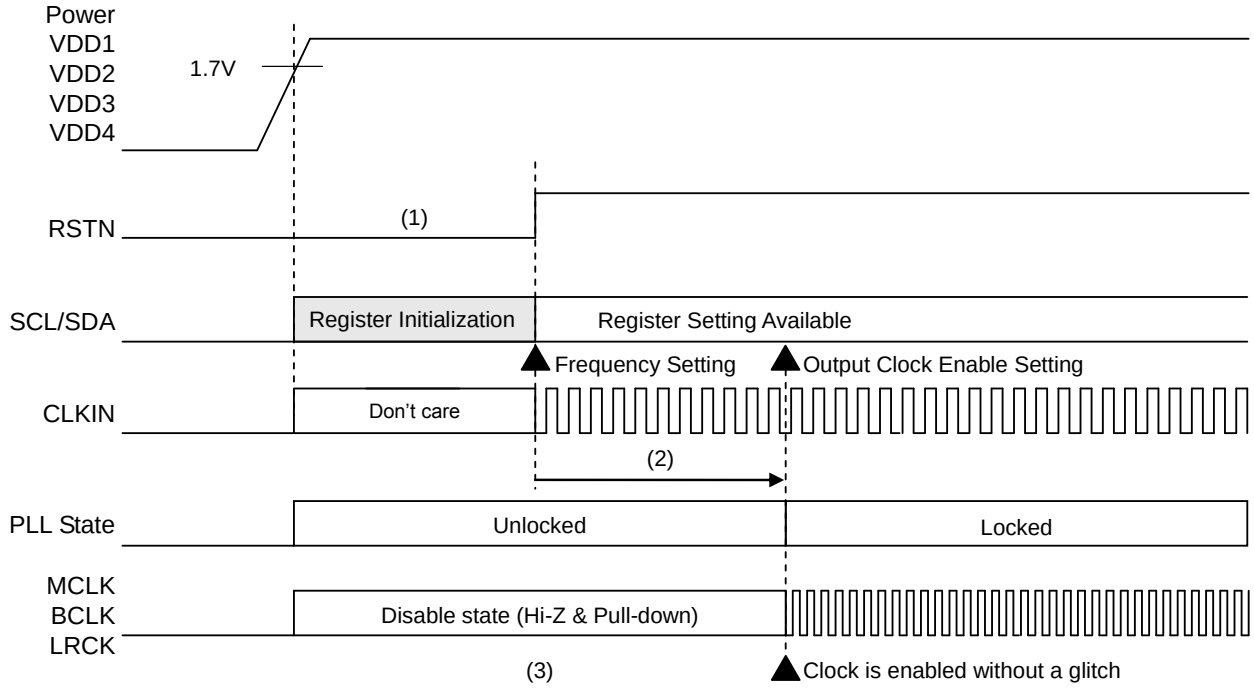
■ System Reset

The AK8157A should be reset once by bringing the RSTN pin = “L” upon power-up. It initializes register settings of the device.

■ Power-up Timing

Registers of the AK8157A are initialized by bringing the RSTN pin to “L”. The MCLK, BCLK and LRCK outputs are floating (Hi-Z) and connected to 160kΩ pull-down internally. PLL1, PLL2 and VREF circuits are power-up.

Registers of the AK8157A are able to write when RSTN pin is change to “H”.



(1) VDD1-4 power supply should be powered up at the same time by bringing the RSTN pin to “L”. Registers of the AK8157A are initialized by bringing the RSTN pin to “L”.
After VDD1-3 reach 1.7V, the RSTN pin should be changed from “L” to “H” with an interval of 200μs or more.

(2) When the RSTN pin is “H”, the output clock frequency configuration can be selected by internal register setting (MDSEL1-0 bits and MCKSEL1-0 bits). After setting the output clock frequency configuration, MCK_DIS bit, BCK_DIS bit and LR_DIS bit are recommended to change from “1” to “0” with an interval of 1ms or more to output MCLK, BCLK and LRCK clocks without a glitch.

(3) The MCLK, BCLK and LRCK outputs are floating (Hi-Z) and connected to 160kΩ pull-down internally.

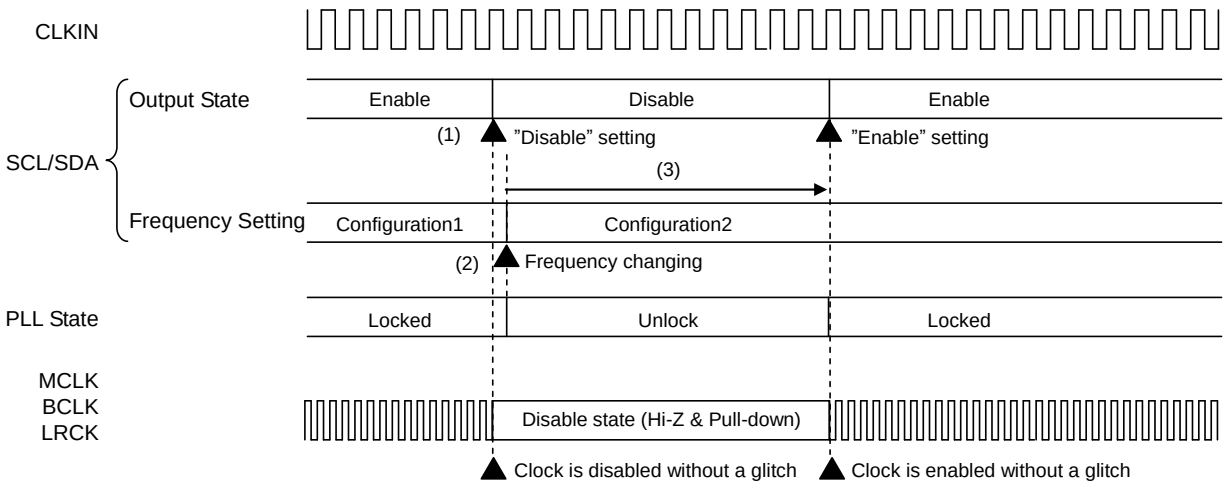
Figure 7. Power-up Timing Example

■ Glitch-free Function

The AK8157A has a Glitch-free function. MCLK, BCLK and LRCK output clocks can be switched enable and disable without a glitch.

■ Frequency Configuration Change Sequence

When outputs frequency of the MCLK, BCLK and LRCK are changed by internal register setting (MDSEL1-0 bits and MCKSEL1-0 bits), it is recommended to disable output clocks to not output unstable frequency clock.



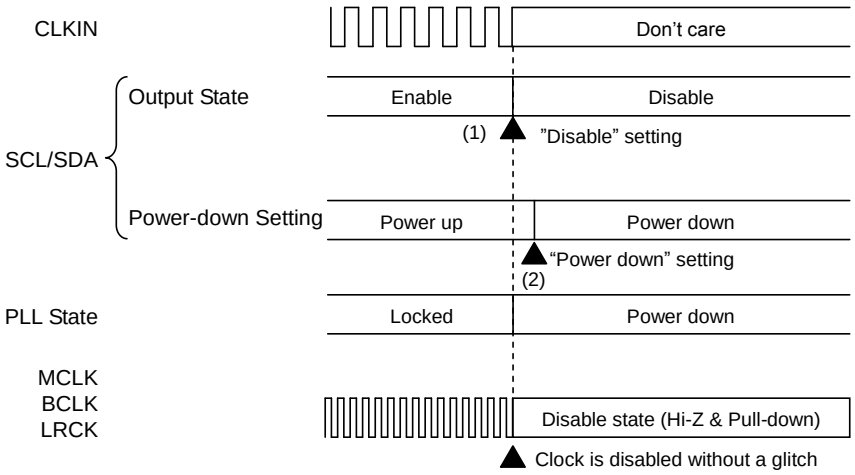
(1) MCK_DIS bit, BCK_DIS bit and LR_DIS bit are changed from "0" to "1".
(2) The output clock frequency configuration can be changed by internal register setting (MDSEL1-0 bits and MCKSEL1-0 bits).
(3) After changing the output clock frequency Configuration2, it is recommended to change MCK_DIS bit, BCK_DIS bit and LR_DIS bit to "0" from "1" with an interval of 1ms or more. Then MCLK, BCLK and LRCK can be output without a glitch.

Figure 8. Frequency Configuration Change Sequence Example

■ Power-down and Power-up Sequence by Internal Registers

Internal circuits of the AK8157A can be powered down and up by setting registers (PLL1_PD bit, PLL2_PD bit and VREF_PD bit). It is recommended to disable output clocks to not output unstable frequency clocks when internal circuits of the AK8157A are powered down and up.

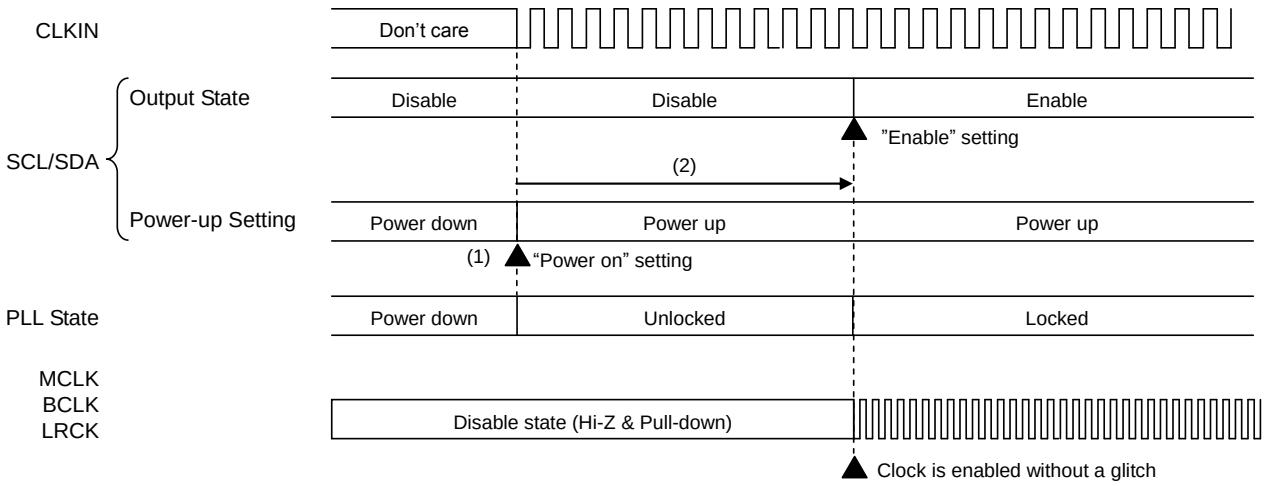
(1) Power-down by changing MCK_DIS bit, BCK_DIS bit and LR_DIS bit from “0” to “1”



(1) MCK_DIS bit, BCK_DIS bit and LR_DIS bit are changed from “0” to “1”.
(2) Internal circuits of the AK8157A are powered down by setting internal registers (PLL1_PD bit, PLL2_PD bit and VREF_PD bit).

Figure 9. Power-down Sequence Example

(2) Power-up by changing MCK_DIS bit, BCK_DIS bit and LR_DIS bit from “1” to “0”



(1) Internal circuits of the AK8157A are switched to power-up state by setting internal registers (PLL1_PD bit, PLL2_PD bit and VREF_PD bit).
(2) After PLL1_PD bit, PLL2_PD bit and VREF_PD bit are changed, it is recommended to change MCK_DIS bit, BCK_DIS bit and LR_DIS bit to “0” from “1” with an interval of 1ms or more for glitch-free outputs of MCLK, BICK and LRCK.

Figure 10. Power-up Sequence Example

■ Register Control Interface

I²C-bus Control Mode

The AK8157A supports the fast-mode I²C-bus (max: 400kHz, Ver 1.0).

1. WRITE Operations

Figure 11 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 17). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as “00100”. The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1pins, CAD0 pin) sets these device address bits (Figure 12). If the slave address matches that of the AK8157A, the AK8157A generates an acknowledgement and the operation is executed. The master must generate the acknowledgement -related clock pulse and release the SDA line (HIGH) during the acknowledgement clock pulse (Figure 18). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.
The second byte consists of the control register address of the AK8157A and the format is MSB first. (Figure 13). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 14). The AK8157A generates an acknowledgement after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 17).
The AK8157A can perform more than one byte write operation per sequence. After receipt of the third byte the AK8157A generates an acknowledgement and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “01H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 19) except for the START and STOP conditions.

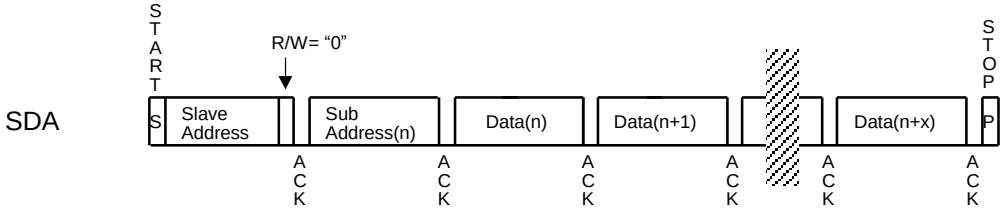


Figure 11. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1-0 is set by the pin)

Figure 12. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 13. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 14. The Third Byte and After The Third Byte

2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK8157A. After transmission of data, the master can read the next address’s data by generating an acknowledgement instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “01H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK8157A supports two basic read operations: Current Address Read and Random Address Read.

2-1. Current Address Read

The AK8157A has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK8157A generates an acknowledgement, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledgement but generates a stop condition instead, the AK8157A ceases the transmission.

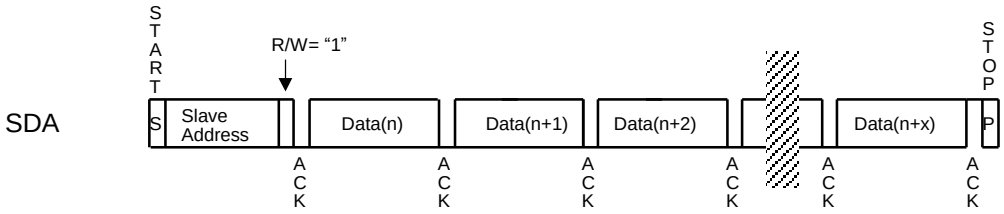


Figure 15. Current Address Read

2-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK8157A then generates an acknowledgement, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledgement but generates a stop condition instead, the AK8157A ceases the transmission.

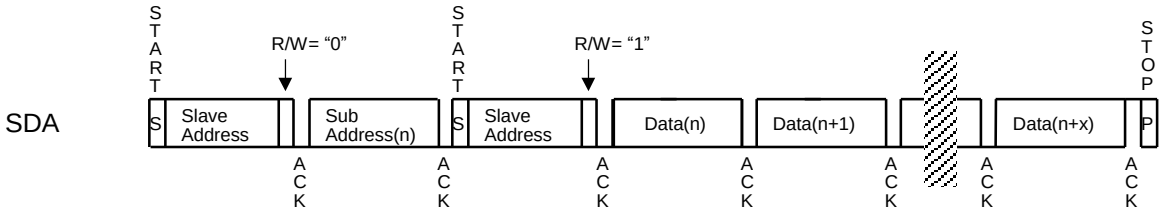


Figure 16. Random Address Read

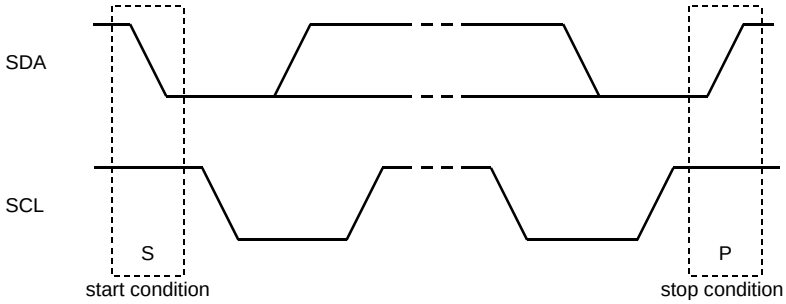


Figure 17. Start Condition and Stop Condition

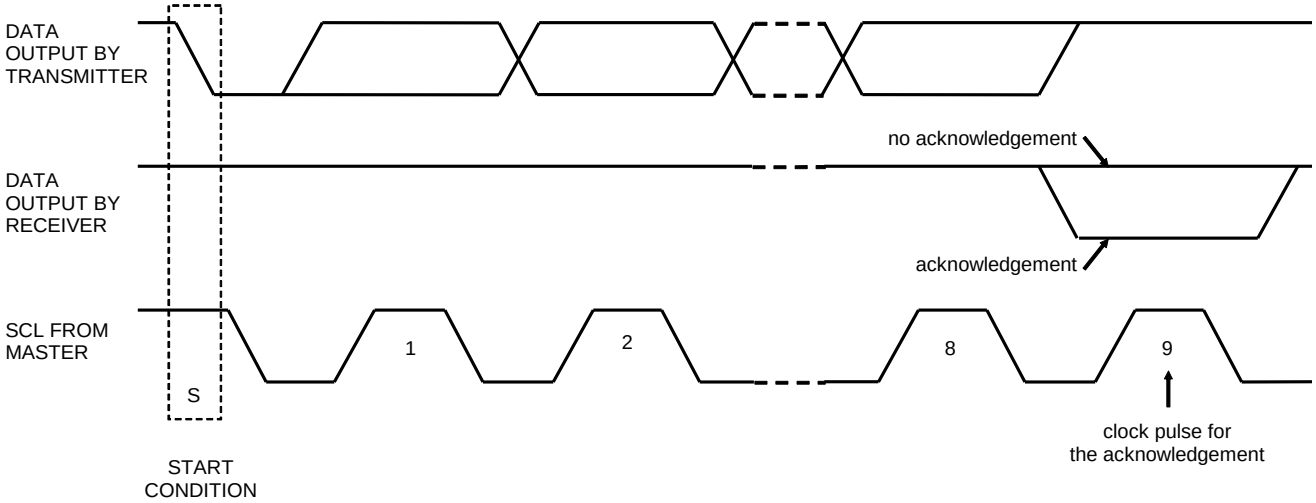


Figure 18. Acknowledgement (I^2C Bus)

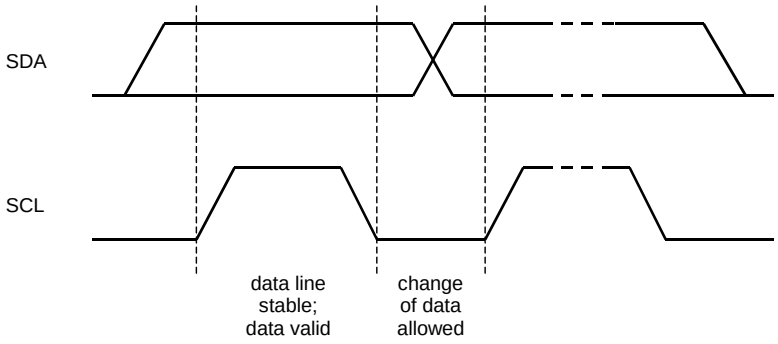


Figure 19. Bit Transfer (I^2C Bus)

Function List

Table 2. Function List

Function	Default	Address	Bit
Power Management	Power-up	00H	PLL1_PD PLL2_PD VREF_PD
Output Clock Control	Disable Clock Output	00H	MCK_DIS BCK_DIS LR_DIS
The Output Clock Frequency Selection of the MCLK pin	MCLK = 16.384MHz	01H	MCKSEL1-0
The Output Clock Mode Selection of the Sampling Speed	LRCK = 32kHz BCLK = 2.048MHz	01H	MDSEL1-0

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	LR_DIS	BCK_DIS	MCK_DIS	reserved	reserved	VREF_PD	PLL2_PD	PLL1_PD
01H	Control 2	reserved	reserved	MDSEL1	MDSEL0	reserved	reserved	MCKSEL1	MCKSEL0

Notes:
The AK8157A supports read command in I^2C-bus control mode.
Data must not be written into addresses from 02H to 1FH.
The reserved bits defined as “0” must contain a “0” value.
When the RSTN pin goes to “L”, the registers are initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	LR_DIS	BCK_DIS	MCK_DIS	reserved	reserved	VREF_PD	PLL2_PD	PLL1_PD
R/W		R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	0

PLL1_PD: PLL1 Power Management
0: Power up (default)
1: Power down

PLL2_PD: PLL2 Power Management
0: Power up (default)
1: Power down

VREF_PD: Internal VREF Power Management
0: Power up (default)
1: Power down

MCK_DIS: MCLK pin Output Clock Control
0: Enable: Clock Output
1: Disable: “L” Output by 160kΩ (typ.) pull-down resistor (default)

BCK_DIS: MCLK pin Output Clock Control
0: Enable: 64fs Clock Output
1: Disable: “L” Output by 160kΩ (typ.) pull-down resistor (default)

LR_DIS: LRCK pin Output Clock Control
0: Enable: fs Clock Output
1: Disable: “L” Output by 160kΩ (typ.) pull-down resistor (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	reserved	reserved	MDSEL1	MDSEL0	reserved	reserved	MCKSEL1	MCKSEL0
R/W		R	R	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

MCKSEL1-0: The Output Clock Frequency Selection of the MCLK pin
Initial value is “00” (MCLK pin = 16.384MHz).

Table 3. MCLK pin Output Clock Frequency

MCKSEL1	MCKSEL0	MCLK Output Clock (MHz)	
0	0	16.384	(default)
0	1	22.5792	
1	0	24.576	
1	1	24.576	

MDSEL1-0: The Output Clock Mode Selection of the Sampling Speed
Initial value is “00” (Sampling Speed = Normal Speed Mode).

Table 4. Output Clock Sampling Speed Mode

MDSEL1	MDSEL0	Sampling Speed Mode	
0	0	Normal Speed	(default)
0	1	Double Speed	
1	0	Quad Speed	
1	1	Oct Speed	

10. Recommended External Circuits

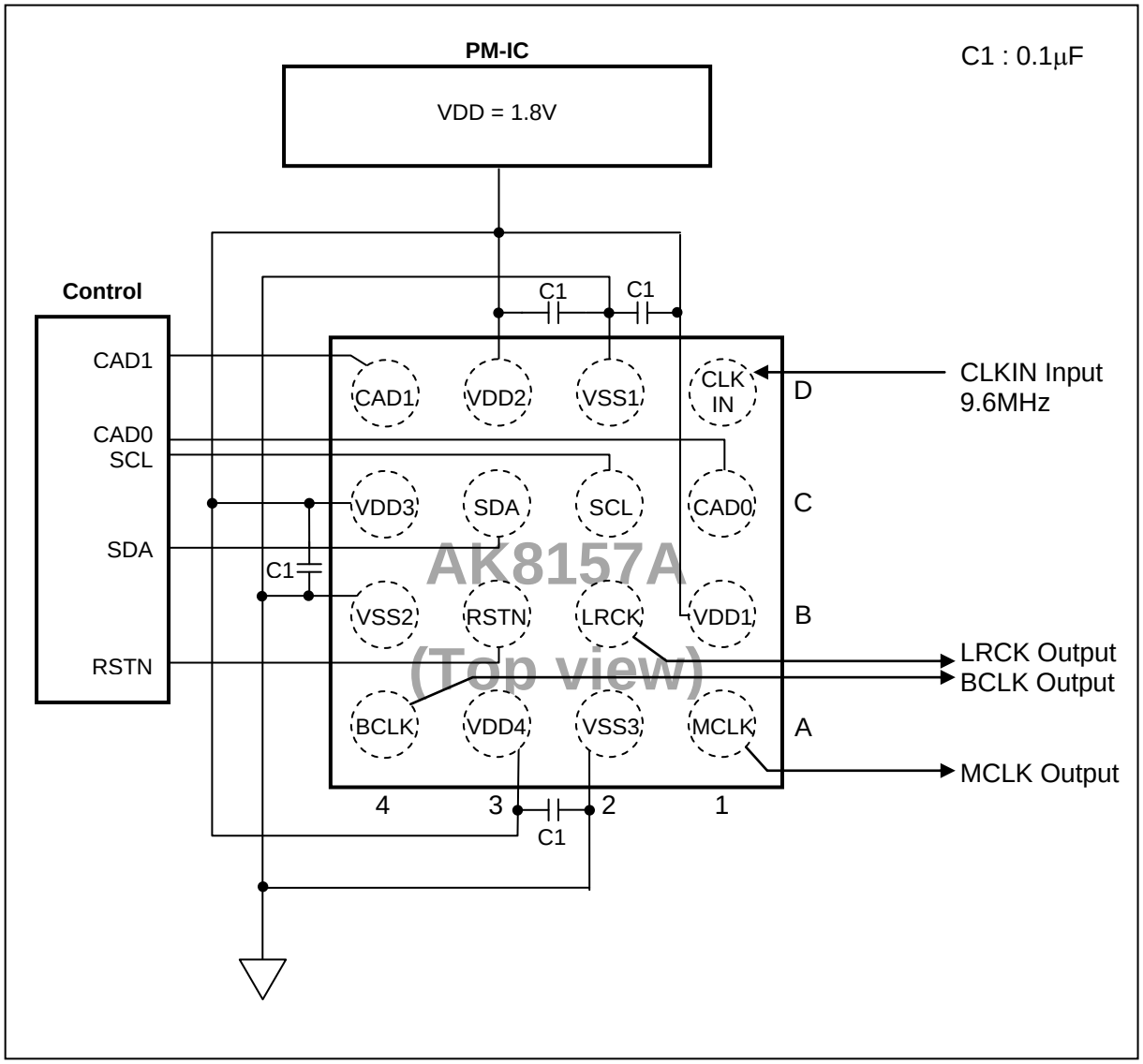


Figure 20. Recommended External Circuits

PCB Layout Consideration

The AK8157A is a high-accuracy and low-jitter clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 20.

Power supply line & Ground pin connection

The AK8157A has four power supply pins (VDD1, VDD2, VDD3 and VDD4) which deliver power to internal circuitry segments, and it has three ground pins (VSS1-3). These pins require connecting to ground plane which will eliminate any common impedance with other critical switching signal return.

0.1μF decoupling capacitors placed at VDD1, VDD2, VDD3 and VDD4 should be grounded at close to the VSS1, the VSS2 and VSS3, respectively.

The AK8157A is recommended to use with a premium DAC, the AK4490. Circuits for a high quality premium audio solution are shown as below.
In this circuit, a 9.6MHz external clock is input to the AK8157A. MCLK, BCLK and LRCK are generated by the AK8157A. SDATA for the AK4490 is output from the external DSP in synchronization with BCLK and LRCK.

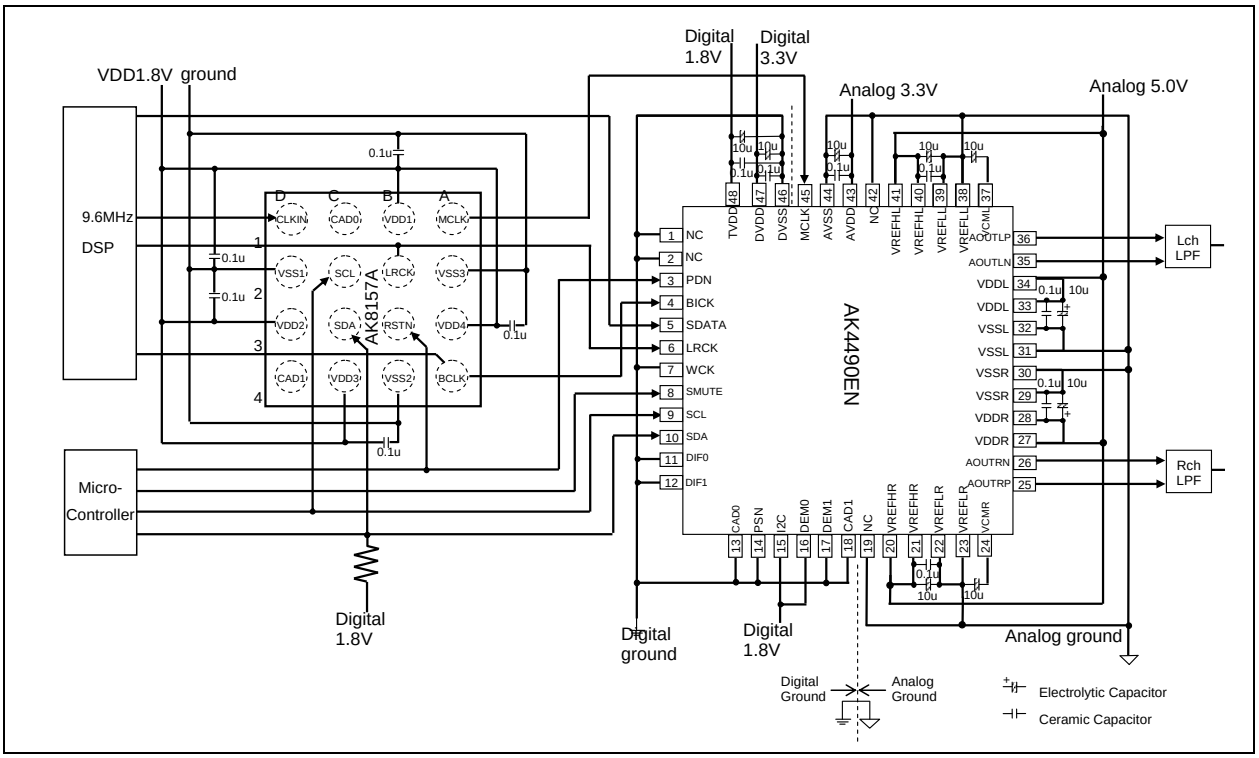
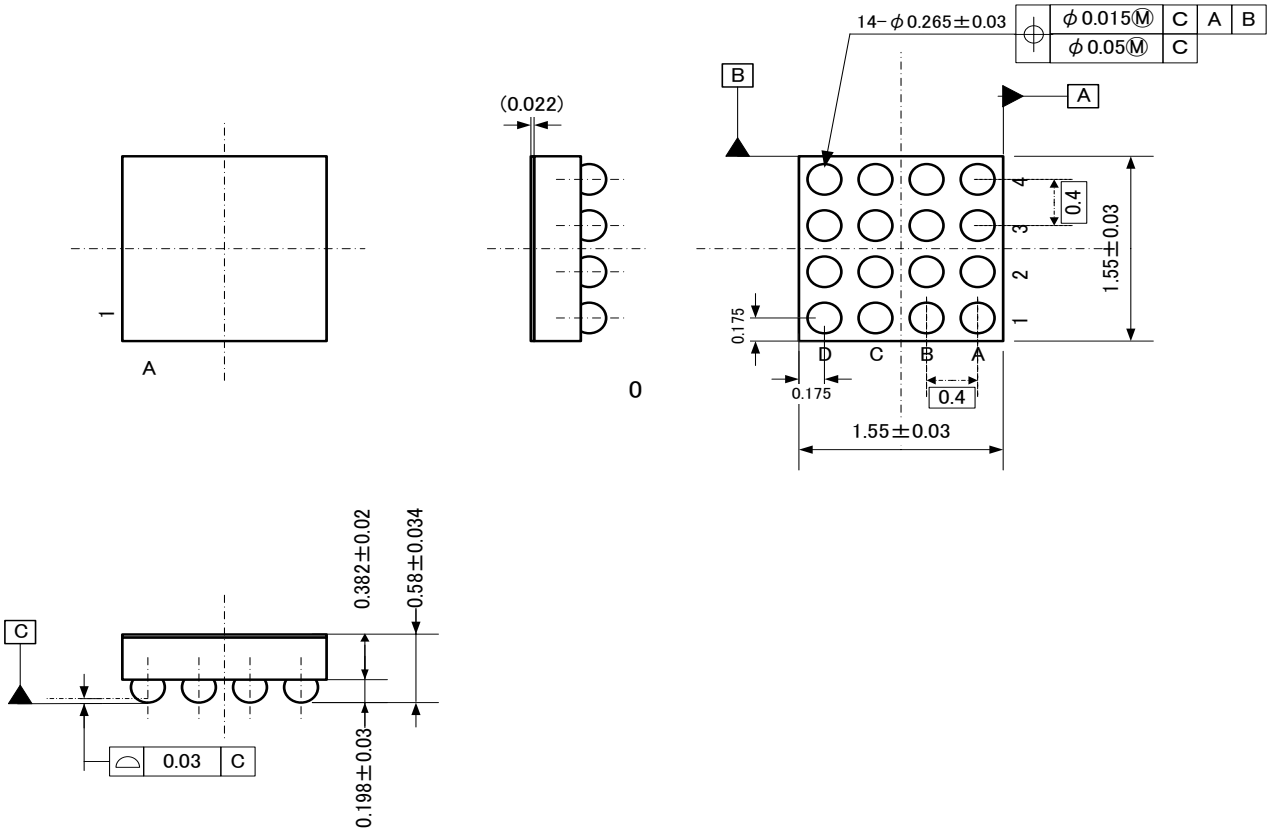


Figure 21. High Quality Premium Audio Solution of the AK4490 with the AK8157A

11. Package

■ Outline Dimensions

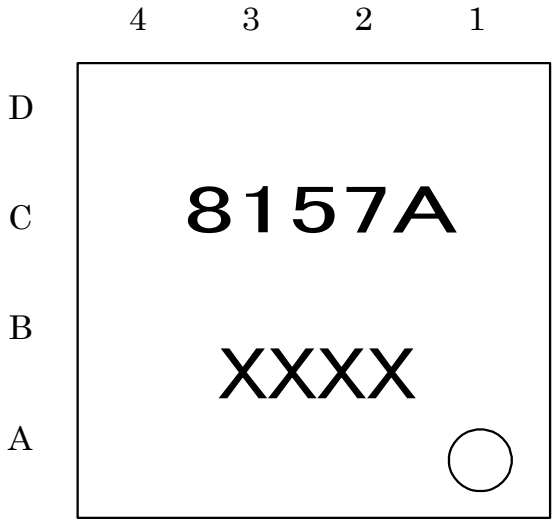
0.4mm pitch 1.55mm x 1.55mm 16-pin WLCSP (Unit: mm)



■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
Solder ball material: SnAgCu

■ **Marking**



1) Pin #A1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 8157A

12. Ordering Guide

■ **Ordering Guide**

AK8157A	–40 ~ +85°C	16-pin WLCSP (0.4mm pitch)
AKD8157A	Evaluation Board for the AK8157A	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/03/16	00	First Edition		

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