AP3603

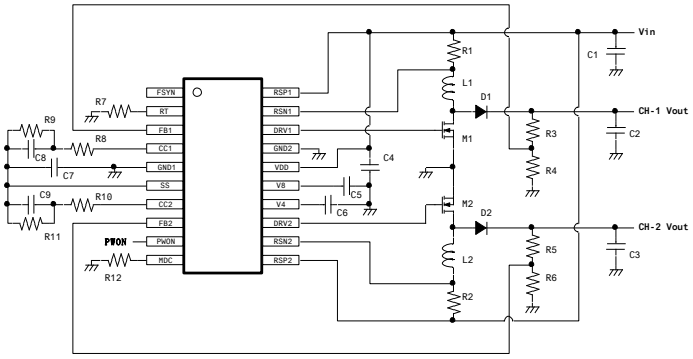
High Power Dual Output Step-Up DC-DC Controller

1. General Description

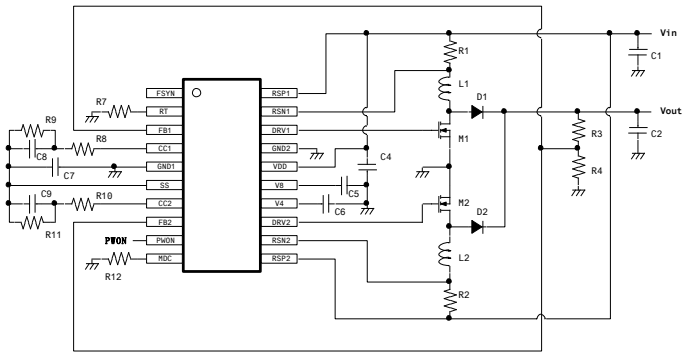
The AP3603 is a dual output step-up DC-DC controller. The output voltage can be set up to 60V by an external feedback resistor. A wide input range of 6.4V to 20V is available, which is possible to realize a high power boost source from the battery or the other power sources. The AP3603 supports either 200W×2ch dual outputs or 400W×1ch dual phase single output. PWM switching frequency is set from 40kHz to 500kHz by an external resistor. As the protective functions, it has output over voltage protection and over current protection. The AP3603 is housed in a space-saving 20-pin HTSSOP package.

2. Features

- Input Voltage Range 6.4 to 20V
- Oscillation Frequency Setting Range 40k to 500kHz（Set by external resistor）
- 8V Gate Driver for External N-channel MOSFET（ON resistance : 3Ω)
- Over Temperature Protection
- Output Over Voltage Protection
- Quasi-Foldback Over Current Protection
- Accuracy of Feedback Voltage +3% /−2 % (Tj=-40～145℃)
- Dual Output or Dual Phase Single Output Application is Selectable
- Package 20-pin HTSSOP



Dual Output Application

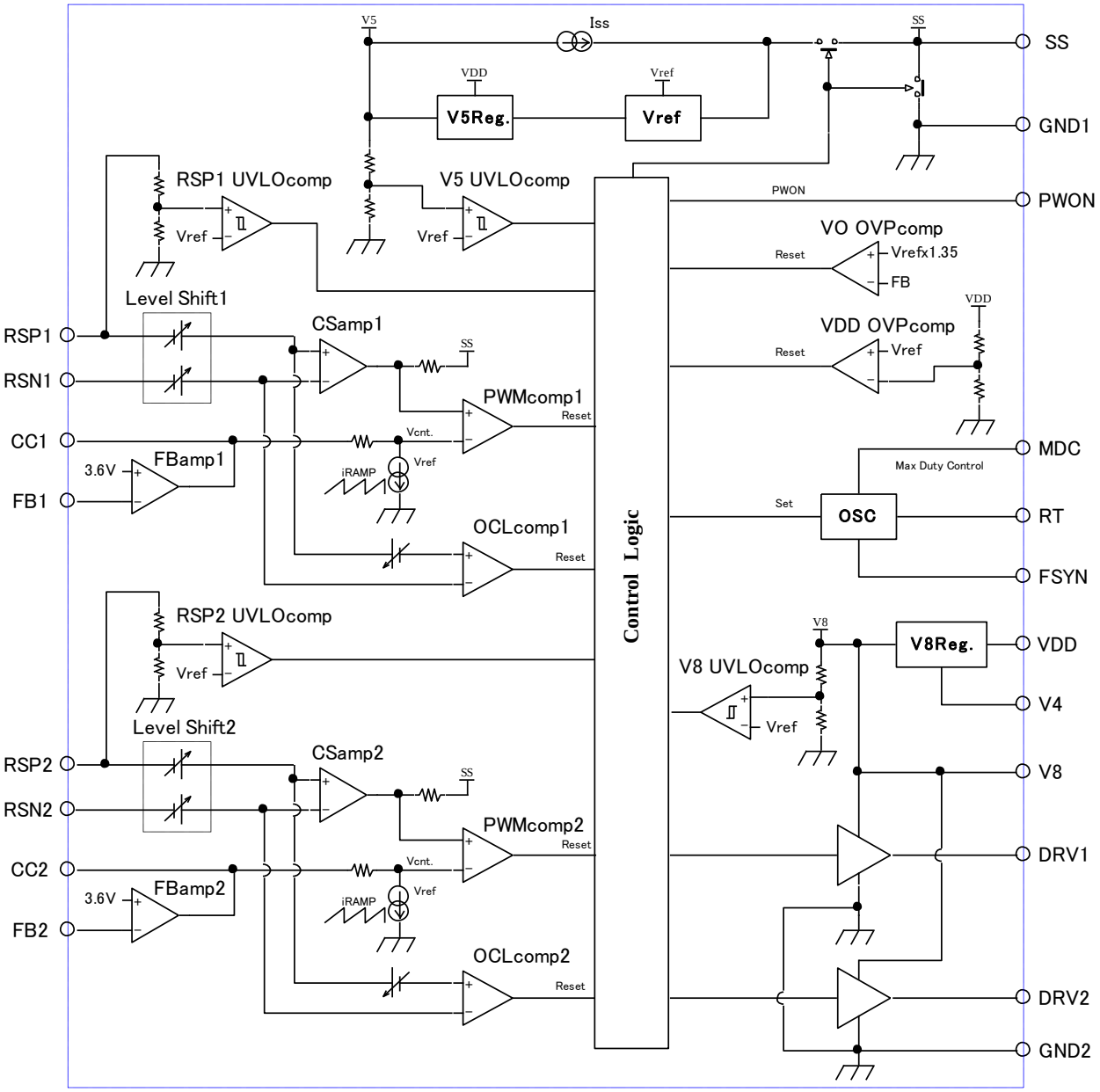


Dual Phase Application

Applications	Input Voltage	Output Voltage	Output Current	Output Power	Circuit
Power Amplifier	12V	20V	CH-1 7.5A CH-2 7.5A	CH-1 150W CH-2 150W	Dual Output
Booster 200W class	6.4V	12V	CH-1 17A CH-2 17A	CH-1 204W CH-2 204W	Dual Output
Booster 400W class	6.4V	12V	34A	400W	Dual Phase Single Output

3. Table of Contents

4. Block Diagram

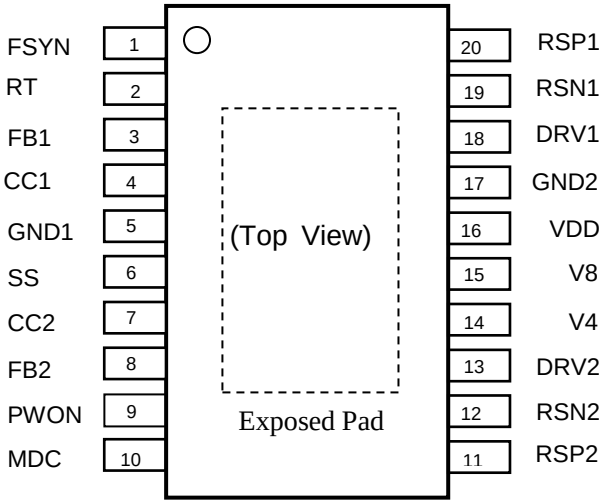


5. Ordering Guide

AP3603	-40～125°C	20-pin HTSSOP

6. Pin Configurations and Functions

■ Pin Configurations



■ Functions

No.	Pin Name	I/O	Function
1	FSYN	I	External Synchronous Pin This pin switches boost N-channel MOSFET of CH1 ON, synchronizing the falling edge of input clock. The pin is pulled-up by 10uA constant current internally.
2	RT	I	PWM Frequency Setting Pin Connect the resistor to GND1 for setting the PWM frequency. Refer 12.2 Operational Frequency Setting to calculate the resistance.
3	FB1	I	CH1 Output Voltage Feedback Pin Output voltage is controlled so that FB1 pin voltage becomes 3.6V. Connect the feedback resistance between the positive side of output capacitor and GND1, and voltage divide node of feedback resistance should be connected to FB1 pin.
4	CC1	O	CH1 Error Amplifier Output Pin Connect the resistance and capacitor in parallel between CC1 pin and SS pin to compensate phase stability.
5	GND1	-	Signal Ground Pin Connect GND2 at just below the AP3603 to prevent potential difference between this pin and the GND2 pin.
6	SS	O	CH1 and CH2 Soft Start Pin Connect a capacitor between SS pin and GND to set the soft start time. When the capacitor value is 0.1uF, the soft start time becomes 12ms.
7	CC2	O	CH2 Error Amplifier Output Pin Connect the resistance and capacitor in parallel between CC2 pin and SS pin to compensate phase stability.
8	FB2	I	CH2 Output Voltage Feedback Pin Connect the feedback resistance between the positive side of output capacitor and GND1 during dual output application usage. Voltage divide node of feedback resistance should be connected to FB2 pin. Connect this pin to FB1 pin at the dual phase single output application usage.
9	PWON	I	Power On Signal Input Pin After “H” signal input, the internal voltage source V5 is powered up and then the start-up sequence is initiated.
10	MDC	O	Maximum On Duty Set Pin Set the maximum on time by the external resistance connecting between MDC and GND1.
11	RSP2	I	CH2 Current Detect Positive Pin
12	RSN2	I	CH2 Current Detect Negative Pin
13	DRV2	O	CH2 N-channel MOSFET Drive Pin
14	V4	O	V4 Linear Regulator Output Pin Middle voltage node of boost driver. Connect MLCC 0.22µF or more between V4 pin and GND2 to stabilize the internal voltage.
15	V8	O	V8 Linear Regulator Output Pin Power source of Boost driver. Connect MLCC 2.2µF or more between V8 and GND2 to stabilize the internal voltage.
16	VDD	-	Main Power Source Pin
17	GND2	-	Power Ground Pin Connect the GND1 at just below the AP3603 to prevent potential difference between this pin and the GND1 pin.
18	DRV1	O	CH1 N-channel MOSFET Drive Pin
19	RSN1	I	CH1 Current Detect Negative Pin
20	RSP1	I	CH1 Current Detect Positive Pin

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit
Voltage between VDD, RSP1, RSP2, RSN1, RSN2 and GND	-	-0.3	40	V
Voltage between CC1, CC2, MDC, SS, FB1, FB2, RT, FSYN, PWON, V4 and GND	-	-0.3	6	V
Voltage between V8, DRV1, DRV2 and GND	-	-0.3	12	V
Voltage between V8 and V4	-	-0.3	6	V
Voltage between RSP1and RSN1, RSP2 and RSN2	-	-0.3	6	V
Storage Ambient Temperature Range	Tstg	-40	150	°C
Junction Temperature	Tj	-40	145	°C
Power Dissipation (Ta=25°C)	P_D	-	3000	mW

Note 1. GND=GND1=GND2
Note 2. Connect GND1 and GND2 at just below the AP3603 on PCB.
Note 3. Junction to Ambient Thermal Resistance θJA= 40°C /W
Ambient temperature of 25ºC using JEDEC 4L board. (114.3mm×76.2mm)

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

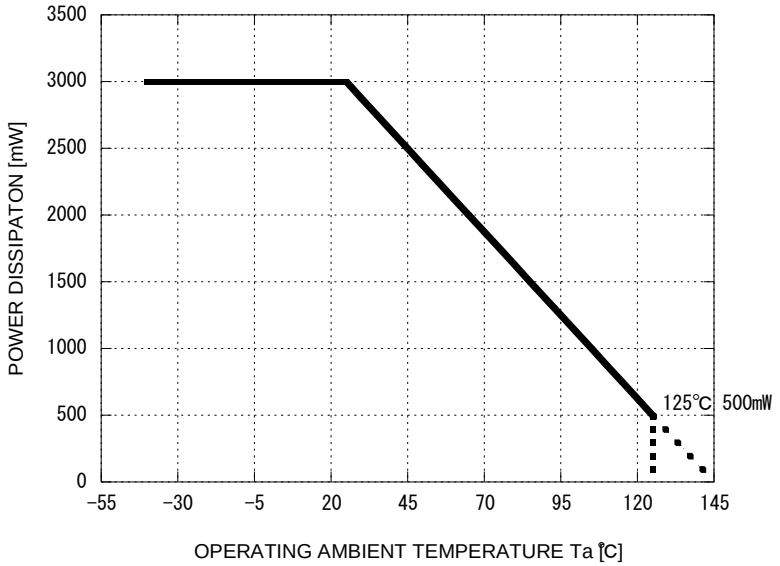


Figure 1. Power Dissipation

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit
Operating input voltage range	Vin	6.4	-	20	V
Operating ambient temperature	Ta	-40	-	125	°C

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

9. Electrical Characteristics

(V_{VDD}=12V, Tj=-40～145°C unless otherwise specified.)

Parameter	Symbol	min	typ	max	Unit	Condition
Output Voltage Range	Vout	-	-	60	V	
8V Driver Power Source	V8	7.6	8.0	8.3	V	
4V Drive Power Source	V4	3.7	4.0	4.2	V	
Feedback Voltage	VrefFB	3.51	3.58	3.69	V	
Shutdown Current 1	$I_{SDN}1$	-	-	10	uA	VDD supply, VDD=10～20V, PWON=0V
Shutdown Current 2	$I_{SDN}2$	-	-	2	uA	RSP1/2supply, RSP1/2 =10～36V, PWON=0V
Static Circuit Current1	$I_{SUPPLY}1$	-	-	3.5	uA	VDD supply
Static Circuit Current2	$I_{SUPPLY}2$	-	-	250	uA	RSP1/2 supply, RSP1/2 =10～36V
Power-ON Voltage	V_{PWON}	2.4	-	-	V	
Power-OFF Voltage	V_{PWOFF}	-	-	0.6	V	
Power-ON Pin Current "H"	I_{PWON}ON	-	15	-	uA	V_{PWON}=5V(Input Current)
Power-ON Pin Current "L"	I_{PWON}OFF	-	-	1.5	uA	V_{PWON}=0V(Output Current)
V8 Output Under Voltage Protection（UVP）	$V8_{UVP}$	5.0	5.28	5.6	V	
V8 UVP Hysteresis	$V8_{UVLOhys}$	0.2	0.28	0.4	V	
RSP Input Under Voltage Protection（UVP）	RSP_{UVP}	3.5	3.75	4.2	V	
RSP Input Under Voltage Protection Release	$RSP_{UVLO\ DIS}$	4.2	4.5	4.8	V	
Soft Start Pin Charge Current	I_{SSON}	8.5	10	11.5	uA	
Soft Start Time	T_{SS}	-	12	-	ms	Css=0.1uF
Over Current Detect Voltage	V_{OCL}	80	100	120	mV	Voltage between RSP and RSN
Output Over Voltage Protection	OVP	130	139	150	%	Ratio to Reference Voltage of Feedback
VDD Over Voltage Protection	VDD_{OVP}	21.5	-	-	V	
Oscillation Frequency	Fclk	-14	0	14	%	40k～500kHz setting Dual Phase 80k～1000kHz
External Synchronous Clock Input Range	Fsync	80	-	120	%	Fclk(typ)Ratio.
External Synchronous Clock Input threshold	Vsync	0.6	-	2.4	V	
External N-channel MOSFET Switching Time (Note 4)	Trise	80	100	150	ns	C_L=10nF 10%to90% V_{VDD}=13V f=250kHz
	Tfall	20	55	150	ns	C_L=10nF 90%to10% V_{VDD}=13V f=250kHz
Minimum On Time	MIN_{ON}	-	200	-	ns	
Minimum Off Time	MIN_{OFF}	-	250	-	ns	R_{MDC}＞127kΩ
Thermal Protection Operating Temperature (Note 4,Note 5)	TSD	-	175	-	°C	
Thermal Protection Hysteresis (Note 4,Note 5)	TSDhys	-	15	-	°C	

Note 4. Guaranteed by design.

Note 5. This function protects the AP3603 against an overheat situation. However, it does not guarantee the operation under the condition that the overheat situation beyond the specifications continues.

10. Functional Descriptions

10.1 Basic Operation

The AP3603 operates in current mode PWM controlling. The feedback voltage (FB1 pin and FB2 pin) is compared to an internal reference voltage by an error amplifier. Then the output of an error amplifier (CC1 pin and CC2 pin) is converted into a current reference which compares to the inductance current. The ON time of an external N-channel MOSFET continues until the inductor current reaches to the current reference. The inductor current is detected by the current sensing resistor (R1 and R2) which is connected between RSP and RSN. When the current reaches the target, the external N-channel MOSFET turns off and the AP3603 continues these cycles for the asynchronous PWM operation.

10.2 Shut Down

Even if the main power supply (V_{VDD}) is supplied, the AP3603 is in shutdown status if the PWON pin is "L". Under this condition, the shutdown current is maximum 10uA.

10.3 Power On Sequence

When PWON pin becomes "H" from "L", V5 and UVLO circuits start up. After V5 starts up, the voltage reference and the over temperature protection circuits start. The AP3603 starts up protective circuit, V4 circuit and V8 circuits if it judges it is not under the over temperature condition. After V8 circuit has settled to 8V, internal oscillation and soft start sequence start. Starting time of V8 is estimated as 4ms(typ) under the typical application condition using recommended components.

10.4 Soft Start

This function raise the output voltage gradually by limiting current and voltage, to prevent an over shoot when the output voltage is powered up. When a reset signal from the internal power supply circuit is released, the AP3603 start charging to an external capacitor connected to SS pin by a constant current and soft start operation is finished when the reference voltage reaches 1.2V. During this time, the current limit value and the over voltage detection value is changed in proportion to the external capacitor voltage. The start-up time of the output voltage depends on the output capacitor values and load conditions. These values are calculated by following equation.

- Over current protection : 100mV(typ)×SS pin voltage /1.2V (Voltage between RSP pin and RSN pin)
- Over voltage protection : Setting Output voltage×SS pin voltage /1.2V

10.5 Power Down Sequence

If PWON pin becomes "L" from "H" during PWM operation, the AP3603 stops switching and shunts SS pin. Only V8 circuit is shut down as internal circuit.

10.6 Over Voltage Protection

This function monitors the feedback voltage and turns off an external N-channel MOSFET in case the output voltage beyond +139% from setting voltage.

10.7 Quasi-Foldback Over Current Protection (PWM operation)

AP3603 monitors the coil current by the voltage difference between RSP and RSN during on-time of external N-channel MOSFET. When the difference reaches 100mV fixed value, AP3603 turns off the external N-channel MOSFET and prevents coil and MOSFET from destruction. This OCL protection operates every switching cycle and so switching continues.

10.8 CC1 and CC2 Pin Voltage (Error Amplifier output) Clamping Function

The voltage of CC pin (CC1 and CC2) which is the output of error amplifier stays around 1.2V (SS pin voltage) under the condition of normal PWM operation. The feedback response goes worse in case the voltage difference between CC pin (CC1 and CC2) and 1.2V becomes large under the abnormal condition like the output voltage beyond setting voltage. It causes the over shoot or under shoot. The AP3603 clamps the voltage of CC pin (CC1 and CC2) as below to prevent CC pin (CC1 and CC2) voltage from going out of a normal operating condition

Detect condition	Release condition	Operation
CCx pin voltage≦0.9V or FBx pin voltage≦3.6V×75%	Switching command has requested or FBx pin voltage≧3.6V×85%	CCx pin connects to SS pin and Error Amplifier output disconnect to CCx pin

10.9 External Synchronous Operation

External synchronization is available by an input timing signal to the FSYN pin. The AP3603 enters external synchronous operation mode when edge of FSYN turns off the external MOSFET connected to DRV2. If the high level input of FSYN continues more than 1 cycle of internal CLK, the AP3603 change the synchronization from external clock to internal oscillator. The input signal to the FSYN pin for synchronization must be 50% duty. FSYN pin must be open in case of no use of external synchronous operation. The AP3603 does not operate if FSYN pin connect to GND because internal OSC does not generate the clock signal. At the case of using an external synchronous operation, FSYN pin must be open before and during startup. And input the external clock to FSYN pin after V8 voltage reach the target (8V) approximately.

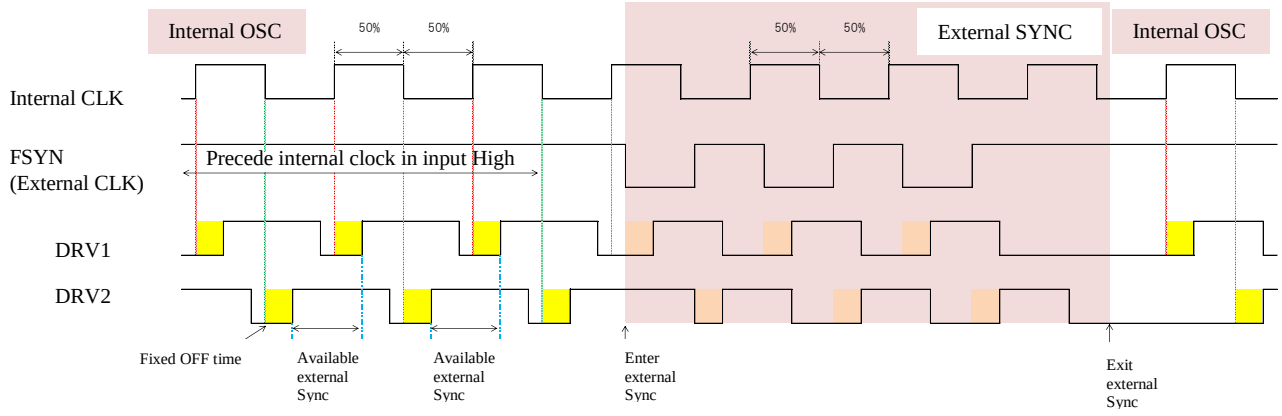


Figure 2. External Synchronous Timing Chart

11. Timing Chart

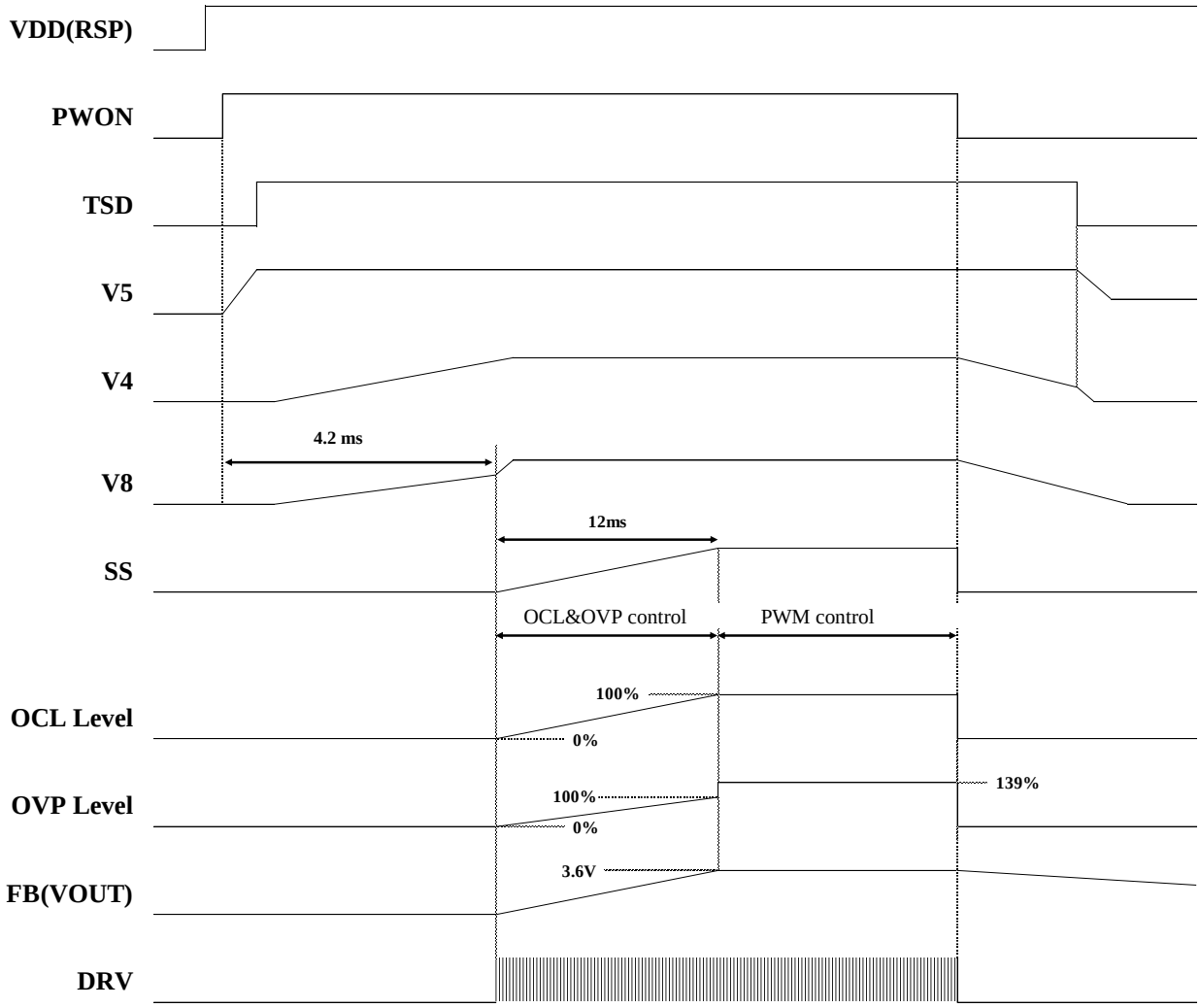


Figure 3.Timing Chart

12. Application Information

12.1 Output Voltage Setting

Output voltage is settled by feedback resistors that are connected between the output capacitor and the GND. The value of R3, R4 (output capacitor-FB pin) and R5, R6(FB pin-GND1) is calculated by the next equations.

$$CH1\,Vout = 3.6 \times \left(1 + \frac{R3}{R4}\right) \quad [V] \qquad CH2\,Vout = 3.6 \times \left(1 + \frac{R5}{R6}\right) \quad [V]$$

12.2 Operational Frequency Setting

Operational frequency is settled by the resistor R7 between the RT pin and the GND. The value of the resistor is calculated by the next equations.

$$R7 = \frac{0.5}{Frequency \quad Hz} \times \frac{1.2V}{3.2pF \times 1.5V \times 4} \quad [\Omega]$$

12.3 Maximum ON Duty Setting

Maximum On duty is settled by the resistor between MDC pin and GND. The value of the resistor is calculated by the next equations.

R_{MDC} [Ω]	Duty(typ) [%]
10k	60%
27k	70%
47k	80%
82k	90%
127k or more	(Note 6)

Note 6. Maximum ON duty is fixed by the operational frequency and minimum off time 250ns (typ). If f>250kHz, duty may be limited by the minimum off time of the IC.

$$Max\,Duty = (1 - 250ns \times Frequency) \times 100 \quad [\%]$$

12.4 Maximum Output Voltage

The maximum output voltage depends on maximum ON duty. It is estimated by the next equation.

$$Max\,Vout = \frac{Vin}{1.1 - Duty} \quad [V]$$

13. Attention of PCB Layout

■ Recommended Layout

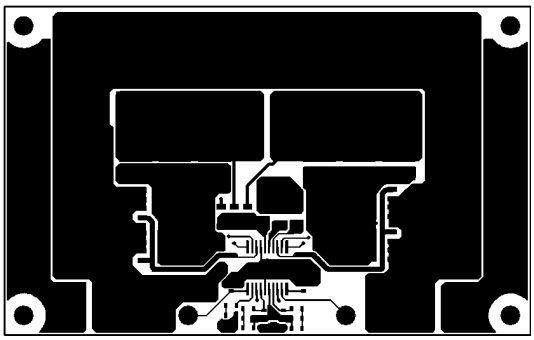


Figure 4. Top Layer

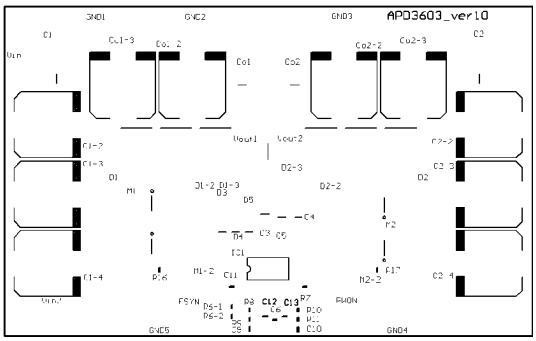


Figure 5. Top Layer Silk

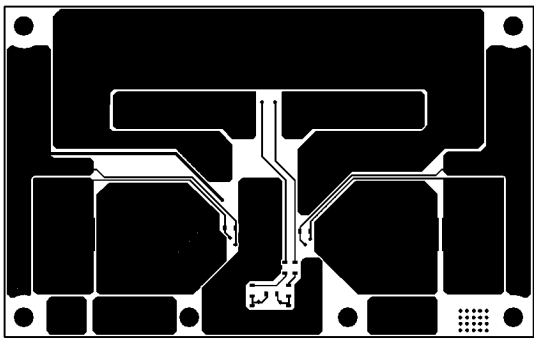


Figure 6. Bottom Layer

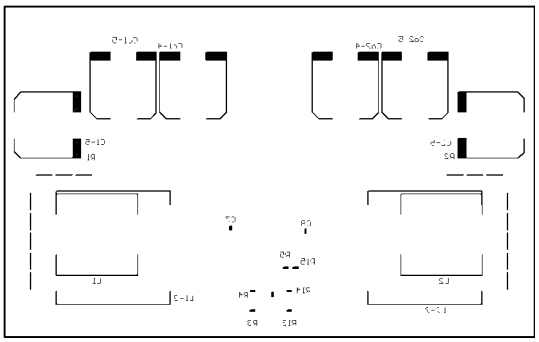


Figure 7. Bottom Layer Silk

■ GND Layout

GND plane should be as large as possible. The output capacitor and input capacitor should be connected to the same ground plane.

■ Switching Node Layout

The switching node line between external N-channel MOSFETs, the Schottky barrier diode and power inductor should be thick and short. Wiring to the DRV1 and DRV2 should be as short as possible.

■ Current Sense Resistor Layout

A current sense resistor should be located as close as possible to the AP3603 so that the wirings to the RSP pin and the RSN pin from the both ends of the current sense resistor have the same resistance.

■ Feedback Pin Layout

Feedback resistors connected in series between the output capacitor and the GND should be connected as near as possible to the output capacitor and as far as possible from the switching node. The middle point of feedback two resistors should be as close as possible to the FB pin.

■ Capacitors for V8, V4 and SS

Capacitors between V8 pin and GND2, V4 pin and GND2, SS pin and GND1 should be connected as near as possible to the each terminals of the AP3603.

■ Bypass Capacitor

The bypass capacitor between the VDD pin and the GND2 should be connected as near as possible to the AP3603.

14. Typical Characteristics

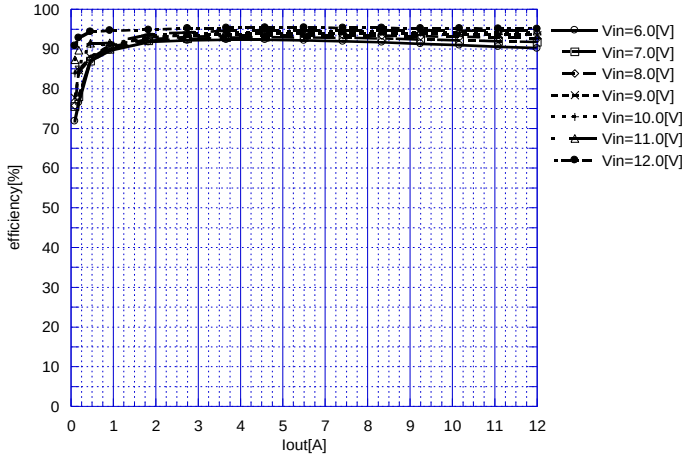


Figure 8. Efficiency 12V Output

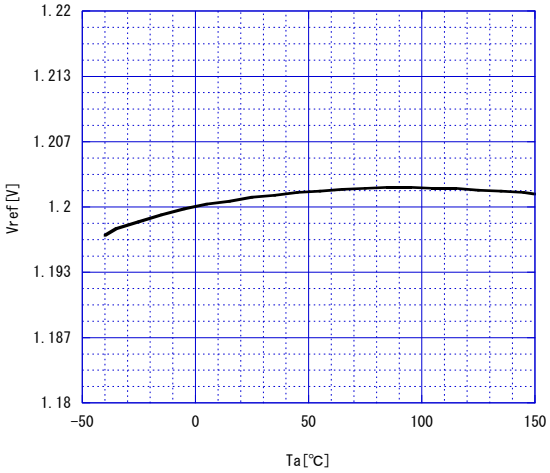


Figure 9. Vref vs. Ta

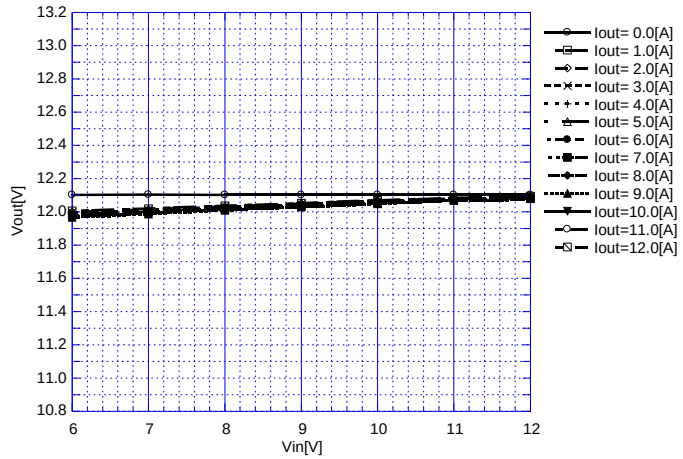


Figure 10. Line Regulation 12V Output

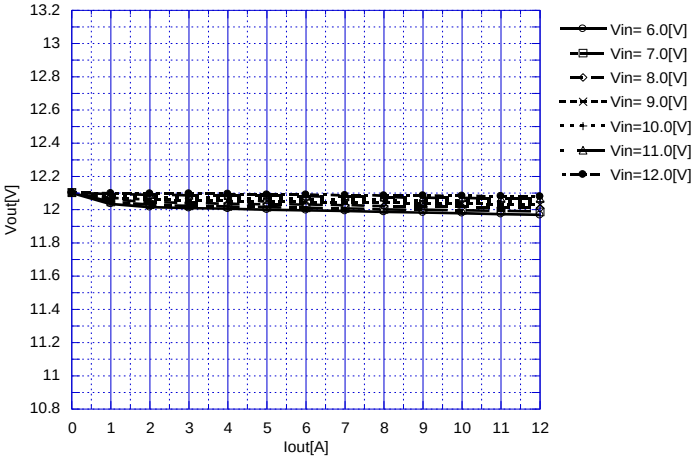


Figure 11. Load Regulation 12V Output

15. Recommended External circuits

■ Recommended External Circuit of Dual Output

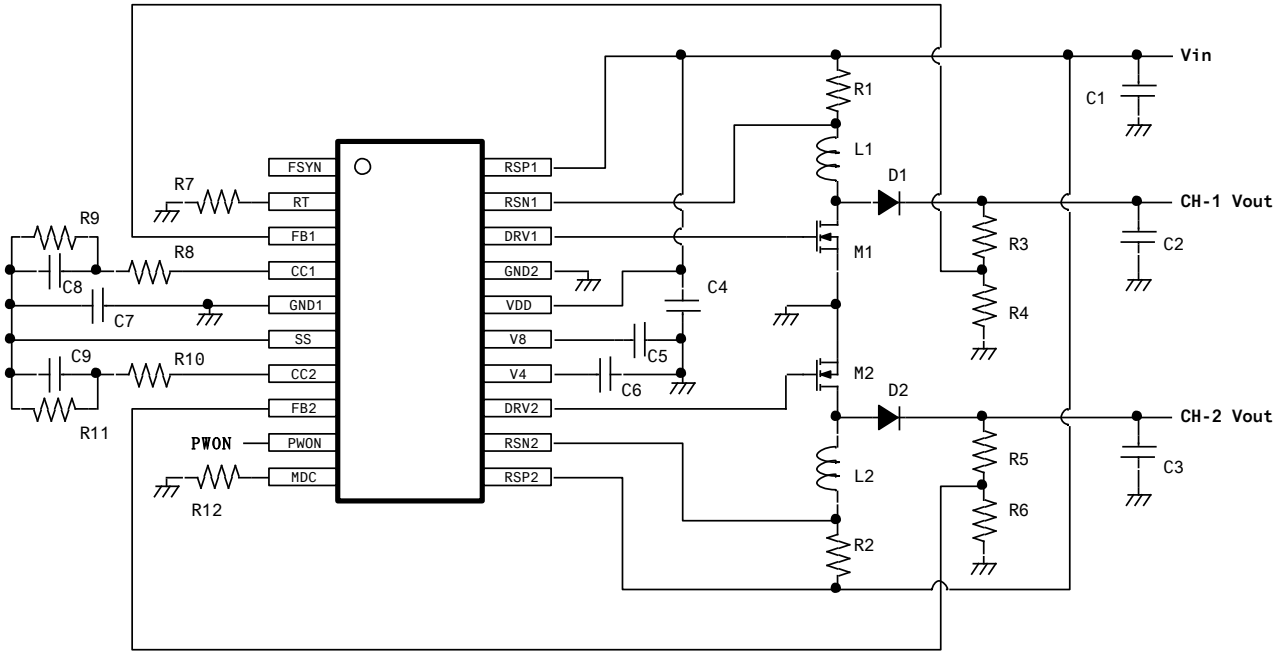


Figure 12. Dual Output Step Up Application

■ Parts List

(Vin=6.4V～12V、Vout=12V、Io=17A、f=400kHz)

Parameter	Symbol	Condition
Input capacitor	C1	10uF×10parallel
Output Capacitor	C2	330uF/16V×4parallel 10uF/25V(MLCC)x2parallel
Output Capacitor	C3	330uF/16V×4parallel 10uF/25V(MLCC)x2parallel
Bypass capacitor	C4	0.1uF
Capacitor for V8	C5	2.2uF
Capacitor for V8 Middle point	C6	0.22uF
Capacitor for soft start	C7	0.1uF
Phase Compensation Capacitor	C8	6800pF
Phase Compensation Capacitor	C9	6800pF
Current Sense Resistor	R1	2mΩ
Current Sense Resistor	R2	2mΩ
CH1 feedback resistor(H)	R3	110kΩ
CH1 feedback resistor(L)	R4	47kΩ
CH2 feedback resistor(H)	R5	110kΩ
CH2 feedback resistor(L)	R6	47kΩ
Frequency setting resistor	R7	75kΩ
CH1 phase compensation resistor	R8	4.7kΩ
CH1 phase compensation resistor	R9	47kΩ
CH2 phase compensation resistor	R10	4.7kΩ
CH2 phase compensation resistor	R11	47kΩ
Catcher diode	D1,D2	40V30A
Power inductor	L1,L2	2.2uH
N-channel MOSFET	M1,M2	40V100A

■ Recommended External Circuit of Dual Phase Single Output

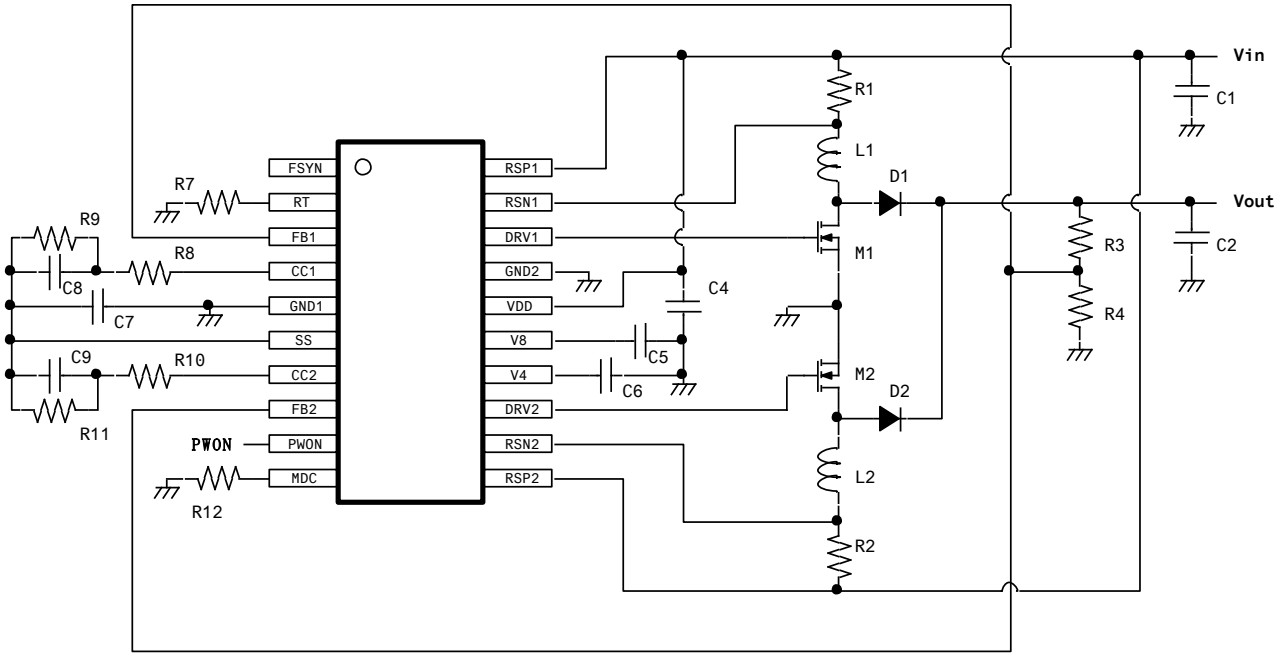


Figure 13. Dual Phase Step-Up Application

■ Parts List

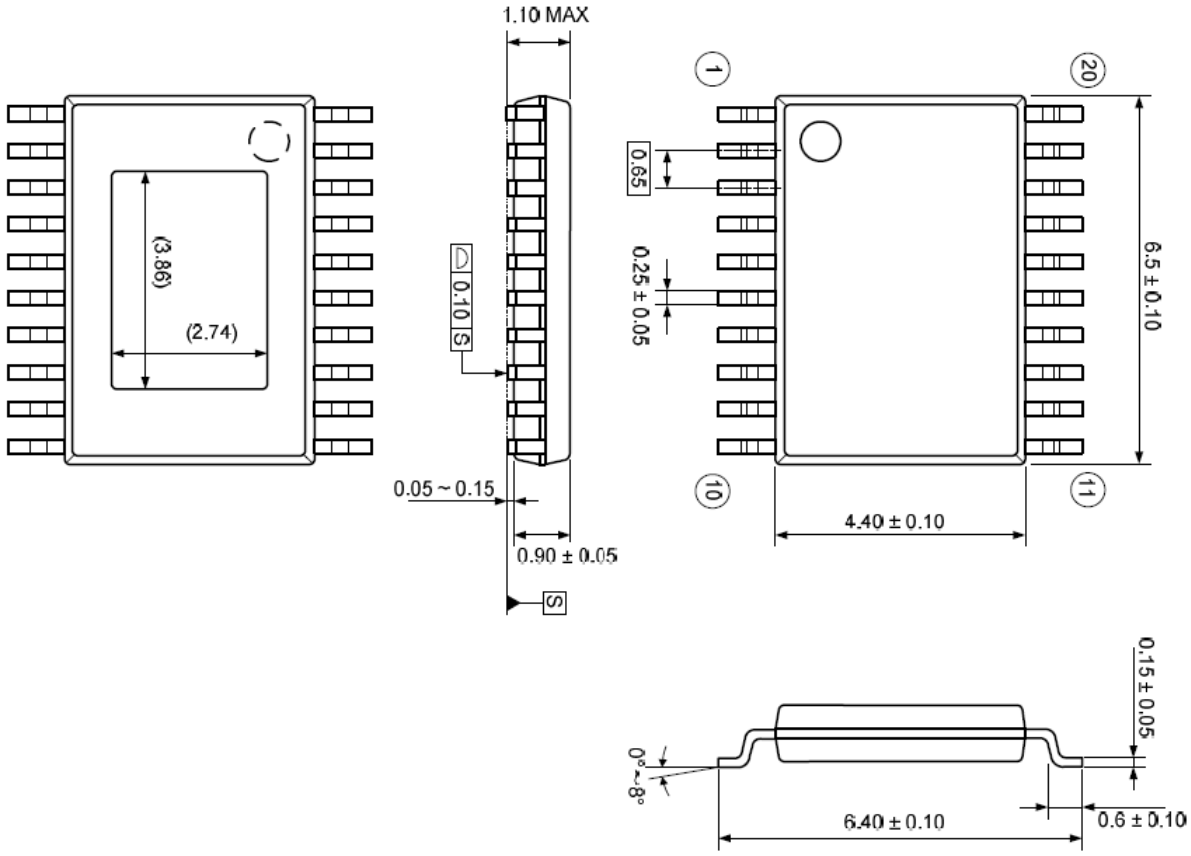
(Vin=6.4～12V、Vout=12V、Iout=34A、f=400kHz)

Parameter	Symbol	Conditions
Input Capacitor	C1	10uF×10parallel
Output Capacitor	C2	330uF/16V×4parallel 10uF/25V(Ceramic)x2parallel
Bypass capacitor	C4	0.1uF
Capacitor for V8	C5	2.2uF
Capacitor for V8 Middle point	C6	0.22uF
Soft Start Capacitor	C7	0.1uF
Capacitor for phase compensation	C8	6800pF
Current Sense Resistor	R1	2mΩ
Current Sense Resistor	R2	2mΩ
Feedback resistor(H)	R3	110kΩ
Feedback resistor(L)	R4	47kΩ
Frequency setting resistor	R7	150kΩ
Phase Compensation Resistor	R8	4.7kΩ
Phase Compensation Resistor	R9	47kΩ
Catcher diode	D1,D2	40V30A
Power inductance	L1,L2	3.3uH
N-channel MOSFET	M1,M2	40V50A

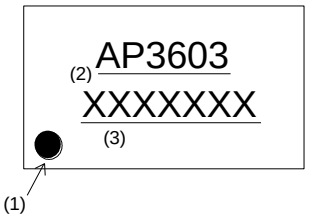
16. Package

■ Outline Dimensions

・20-pin HTSSOP (Unit : mm)



■ Marking



(1) 1pin Indication
(2) Product No.
(3) Date Code (7digits)

17. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/02/09	00	-	First edition
15/03/12	01	8	Add 10.7 Quasi-Foldback Over Current Protection (PWM operation)
15/07/30	02	1 3 9 11	2.Features; Correction of the explanation of input voltage 5. Ordering Guide; Correction of the explanation of ordering number, Correction of the explanation of 10.9 external synchronous operation 12. Application Information; Correction of the explanation of 12.1 output voltage setting.

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