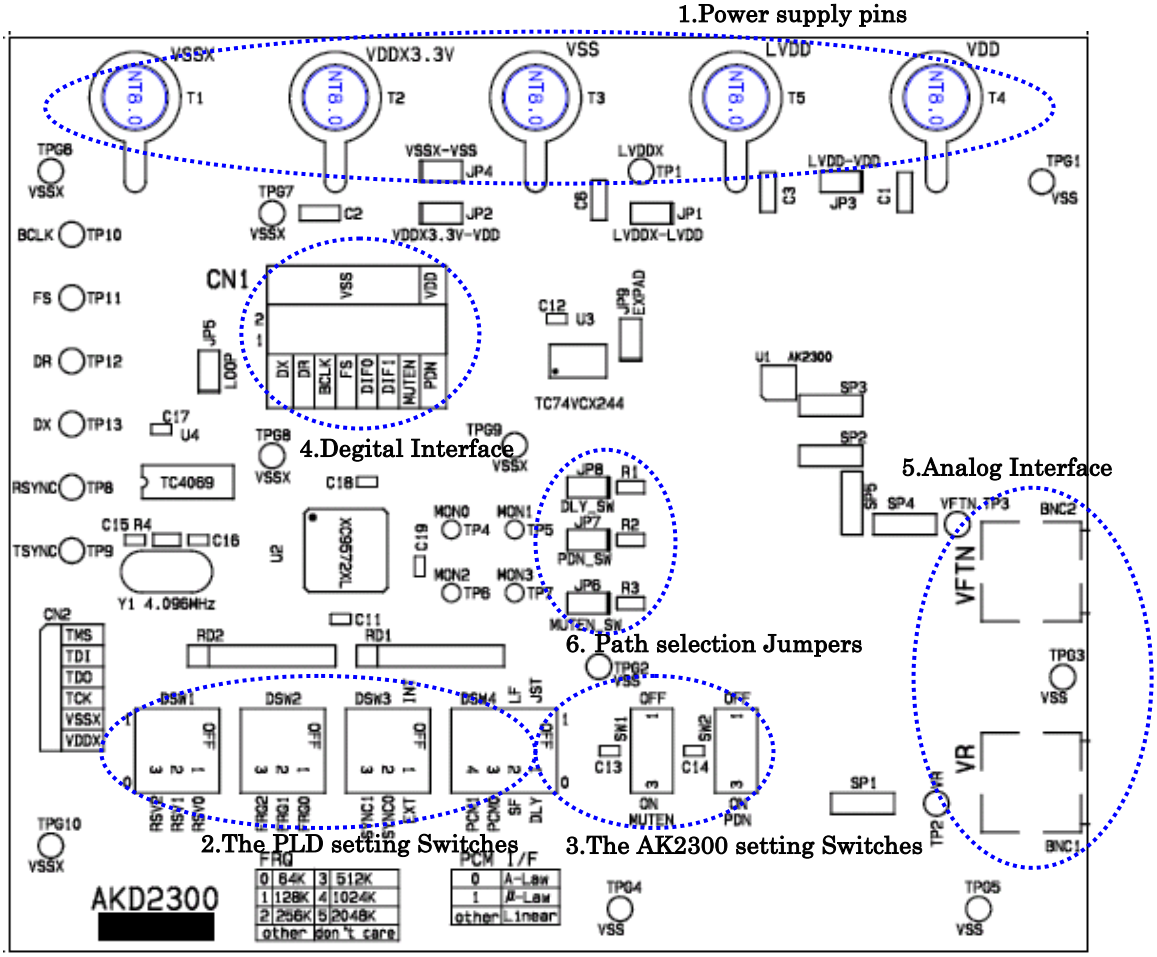
AKD2300

AK2300 Evaluation Board

Board Function

The AKD2300 is the evaluation board for the AK2300.The AKD2300 has on-board(internal) clock generate function. The evaluation can begin by setting the DIP Switches. External resistance and capacitors of the I/O amplifier can be changed. It provides easy the setting of the parameter of the desire.

Board Layout



The AKD2300 has six following components.

1 : Power supply pins

2 : The PLD setting Switches

3 : The AK2300 setting Switches

4 : Digital Interface

5 : Analog Interface

6 : Path selection Jumpers of the AK2300 input data

Power supply pins

Power supply pins is VDD,VSS,LVDD,LVDDX,VDDX_3.3V,VSSX.
Please feed 1.7V～3.6V to the LVDD and LVDDX, and feed 2.6V～3.6V to the VDD. Supply 3.3V to VDDX_3.3V. However, set to become VDD≧LVDD. Connect VSS and VSSX with GND.
Each power supply and GND can be connected by the JP1 and the JP2 and the JP3 and the JP4.
These jumpers settings are shown below. When the digital noise influences on analog characteristics, please remove these jumpers to separate these power line.

Jumper Name	Function
JP1	LVDD and LVDDX are connected.
JP2	VDD and VDDX_3.3V are connected.
JP3	VDD and LVDD are connected.
JP4	VSS and VSSX are connected.

The PLD Setting Switches

The DSW2 and the DSW3 and the DSW4 are switches of the PLD settings. (DSW1 is unused)
The functions of the switches are shown below.

DSW2

Switch Name	Function			
FRQ2 **FRQ1** **FRQ0**	**BCLK Selection** This switch is selects internal BCLK frequency.			
	FRQ2	FRQ1	FRQ0	Frequency
	0	0	0	64kHz
	0	0	1	128kHz
	0	1	0	256kHz
	0	1	1	512kHz
	1	0	0	1024kHz
	1	0	1	2048kH
	1	1	*	Don't care

DSW3

Switch Name	Function		
SYNC1 **SYNC0**	**Frame sync signal selection** (Available in INT mode only) Output a sync signal for external measurement systems to the TP8(RSYNC) and the TP9(TSYNC).		
	SYNC1	SYNC0	Output Signal
	0	0	Refer to the Figure 1.
	0	1	Refer to the Figure 1.
	1	0	Refer to the Figure 1.
	1	1	Refer to the Figure 1.
EXT/INT	**Set the method of supplying BCLK and FS.** EXT: The external clock feed from digital interface. INT: On-board(internal) clock used.		

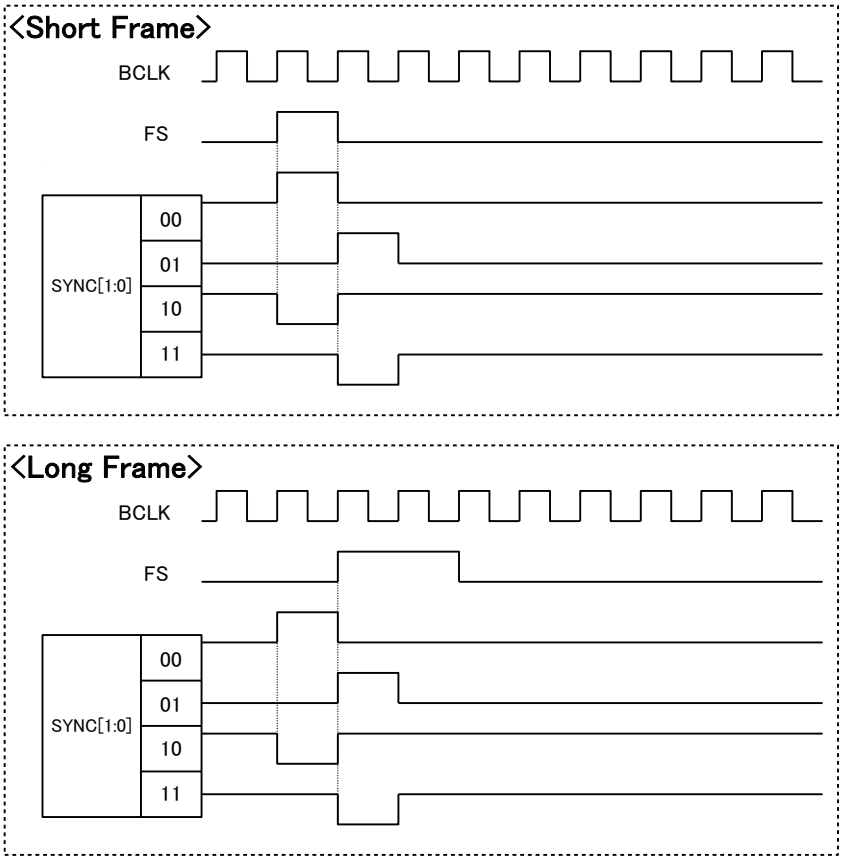


Figure 1

DSW4

Switch Name	Function		
PCM1 **PCM0**	**PCM Interface setting1** This switch selects data format of PCM interface.		
	PCM1	PCM0	PCM Interface
	0	0	A-Law (DIF0 = L)
	0	1	μ-Law (DIF0 = H)
	1	*	Linear (DIF0 = FS)
SF/LF	**PCM Interface setting2** This switch selects FS type at the INT mode. SF: Short Frame(Refer to the Figure 1) LF: Long Frame(Refer to the Figure 1)		

The AK2300 Setting Switches

The SW1 and the SW2 and the DSW4-4 are switches of the AK2300 settings.
The functions of the switches are shown below.

SW1

Switch Name	Function
MUTEN	**PCM Codec output settings** This switch sets the output of PCM CODEC mute. OFF: Normal operation ON: Mute

SW2

Switch Name	Function
PDN	**Power down mode settings** This switch sets power-down mode of the AK2300. OFF: Normal operation ON: Power down mode

DSW4-4

Switch Name	Function
DLY/JST	**PCM Interface settings3** This switch selects input and output timing of PCM data. DLY(DIF1 = L): MSB of DX/DR are input/output by next rising edge of BCLK after the rising edge of FS. (Refer to the Figure 2) JST(DIF1 = H): MSB of DX/DR are input/output by rising edge of FS. (Refer to the Figure 2)

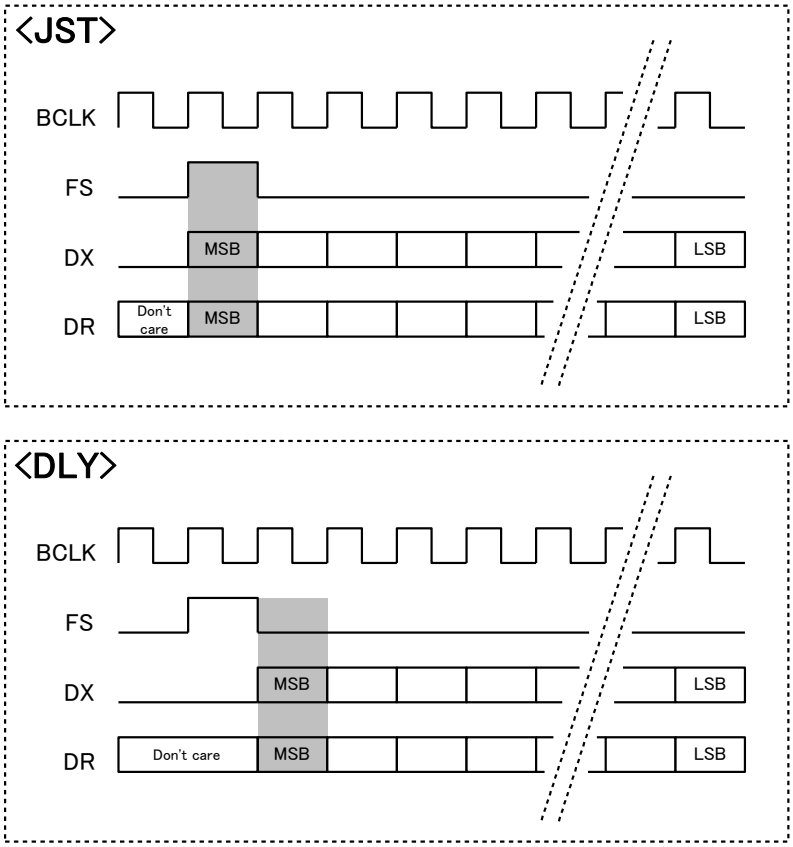


Figure 2

Digital Interface

The AKD2300 has CN1 as a digital interface.

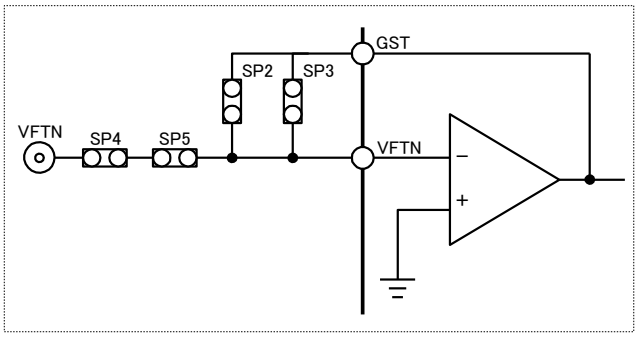
Pin No	Signal Name	Function
1	DX	This pin outputs the DX data from the AK2300.
3	DR	This pin inputs the DR data to the AK2300. When the JP5 is used, As for DX data the loop backing is by DR data.
5	BCLK	This pin inputs external signal BCLK. *
7	FS	This pin inputs external signal FS. *
9	DIF0	This pin inputs external signal DIF0. *
11	DIF1	This pin inputs external signal DIF1.
13	MUTEN	This pin inputs external signal MUTEN.
15	PDN	This pin inputs external signal PDN.
16	VDD	This pin is connected with VDD.
2/4/6/8 10/12/14	VSS	These pins are connected with VSS.

*:Available in EXT mode only.

Analog Interface

The AKD2300 has BNC connector VFTN for transmission amplifier input and BNC connector VR for reception amplifier output.
Insert resistance and capacitors of each amplifier in the socket pin. It provides easy the setting of the parameter of the desire. When shipped, it is set in the parameter of the application circuit of the AK2300 data sheets.

◆Analog input circuit



◆Analog output circuit

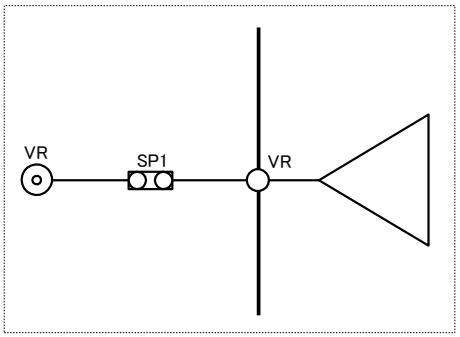


Figure 3

Path selection jumpers of the AK2300 input data

The JP6 and the JP7 and the JP8 are selected input signal (MUTEN,PDN,DIF1) path of the AK2300.
These jumpers settings are shown below.

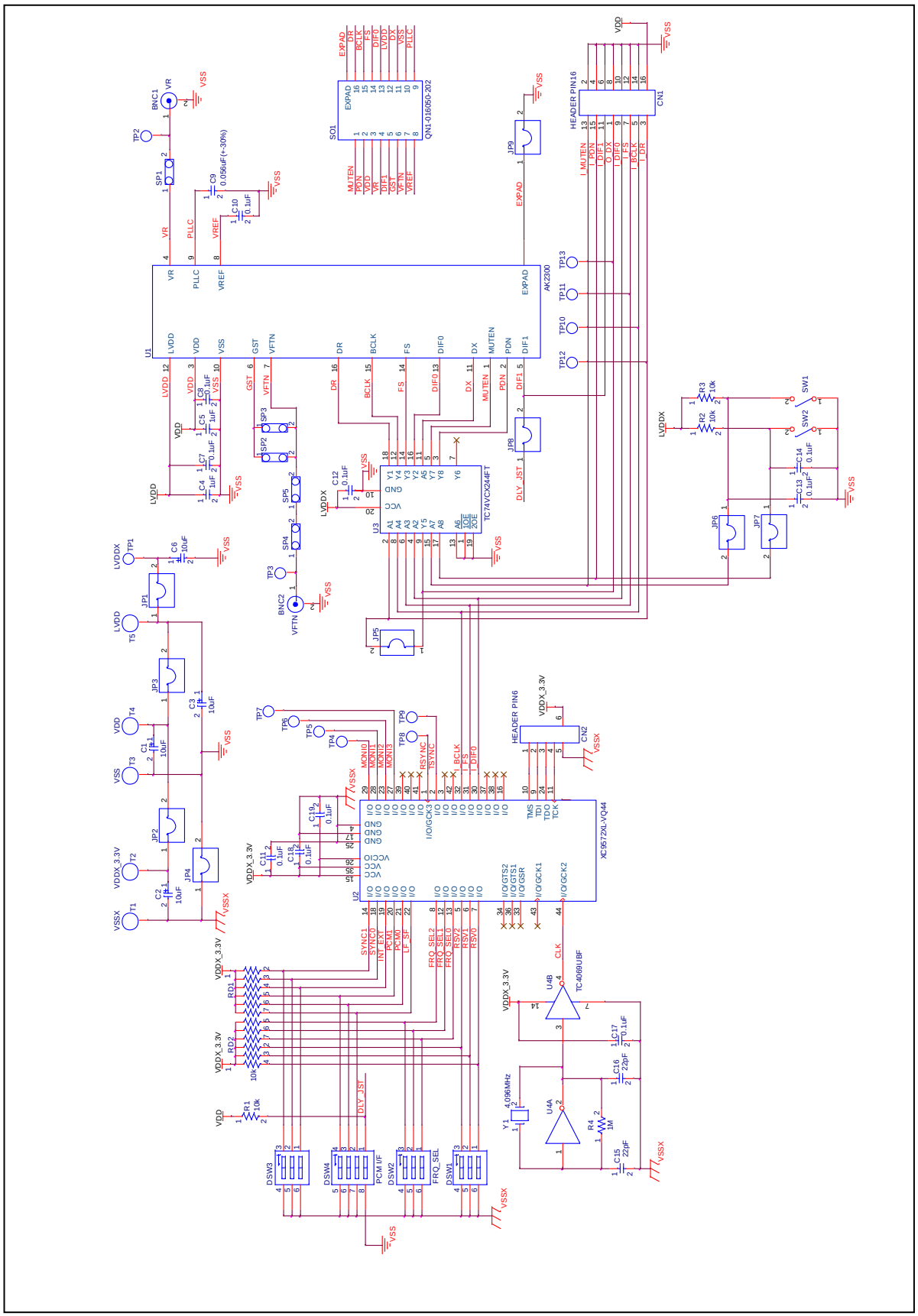
Jumper Name	State	Function
JP6	Short	The MUTEN pin inputs the SW1 setting.
	Open	The MUTEN pin inputs the CN1 setting.
JP7	Short	The PDN pin inputs the SW2 setting.
	Open	The PDN pin inputs the CN1 setting.
JP8	Short	The DIF1 pin inputs the DSW4(DLY-JST) setting.
	Open	The DIF1 pin inputs the CN1 setting.

Connection selection jumpers of the AK2300 Exposed Pad

Jumper Name	State	Function
JP9	Short	Exposed Pad of the AK2300 and VSS are connected.
	Open	Exposed Pad of the AK2300 is Opened.

Board Circuit

The circuit chart of the AKD2300 is shown in the following.



Revision History

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
10/05/13	KM103500	0	First edition	-	
15/02/23	KM103501	0	Add	9-10	“Revision History” and “IMPORTANT NOTICE” are added.

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