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AKD4122A-A

Evaluation board Rev.0 for AK4122A

GENERAL DESCRIPTION

The AKD4122A-A is an evaluation board for the digital sample rate converter, the AK4122A with built-in digital audio interface receiver (DIR). The AKD4122A-A has the digital audio interface and can achieve the interface with digital audio system via opt-conductor.

Ordering guide

AKD4122A-A --- Evaluation board for AK4122A
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- DIR/DIT with optical input/output
- 10pin Header for AKM AD/DA evaluation board
- BNC connector for an external clock input
- 10pin Header for serial control mode

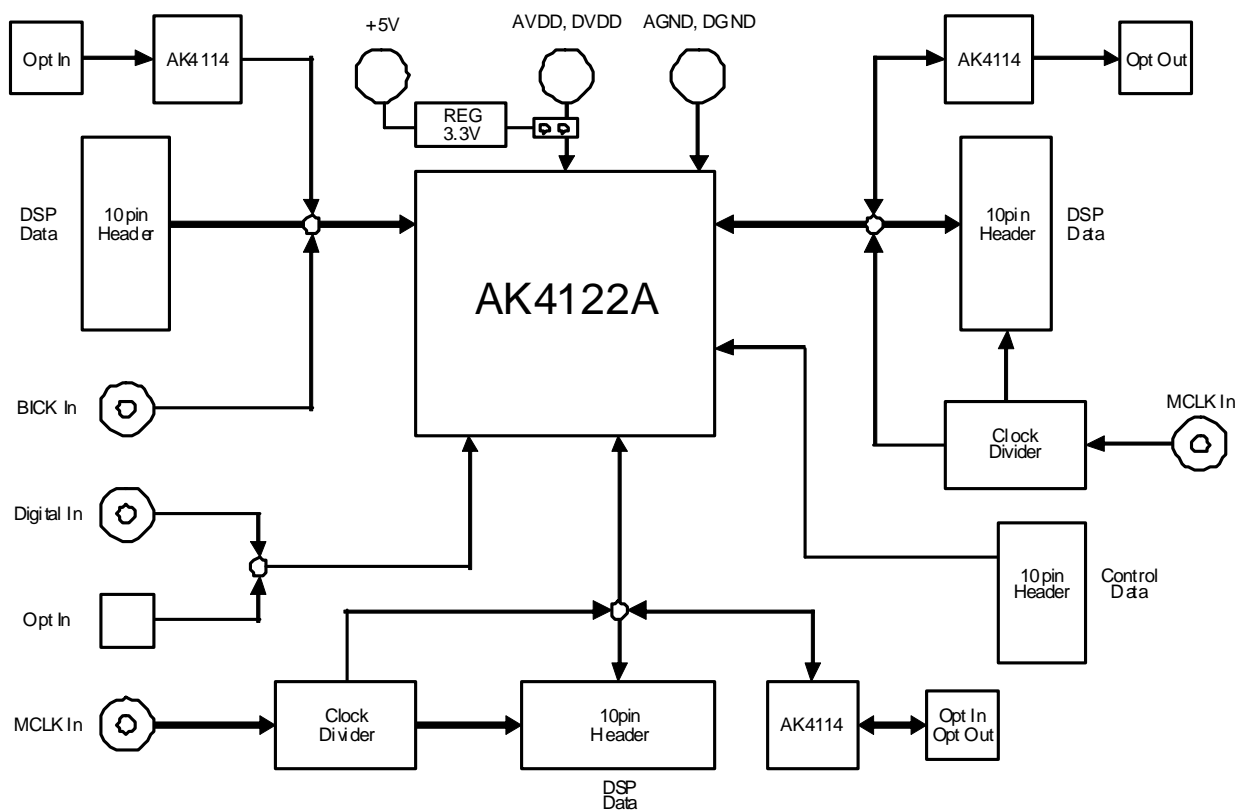


Figure 1. AKD4122A-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

[AVDD]	(red)	= 3.0 ~ 3.6V (typ. 3.3V, AVDD pin)
[DVDD]	(red)	= 3.0 ~ 3.6V (typ. 3.3V, DVDD pin)
[+5V]	(orange)	= +5V (for regulator)
[VCC]	(blue)	= 3.0 ~ 3.6V (typ. 3.3V, for digital logic)
[AGND]	(black)	= 0V
[DGND]	(black)	= 0V

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins. (See the followings.)

3) Power on.

The AK4122A should be reset once bringing SW6 (PDN) "L" upon power-up.

■ Evaluation mode

I/O ports and jumper pins on the board should be set according to the following explanation in order to evaluate each pass of the AK4122A. The block diagram is shown in Figure 2.

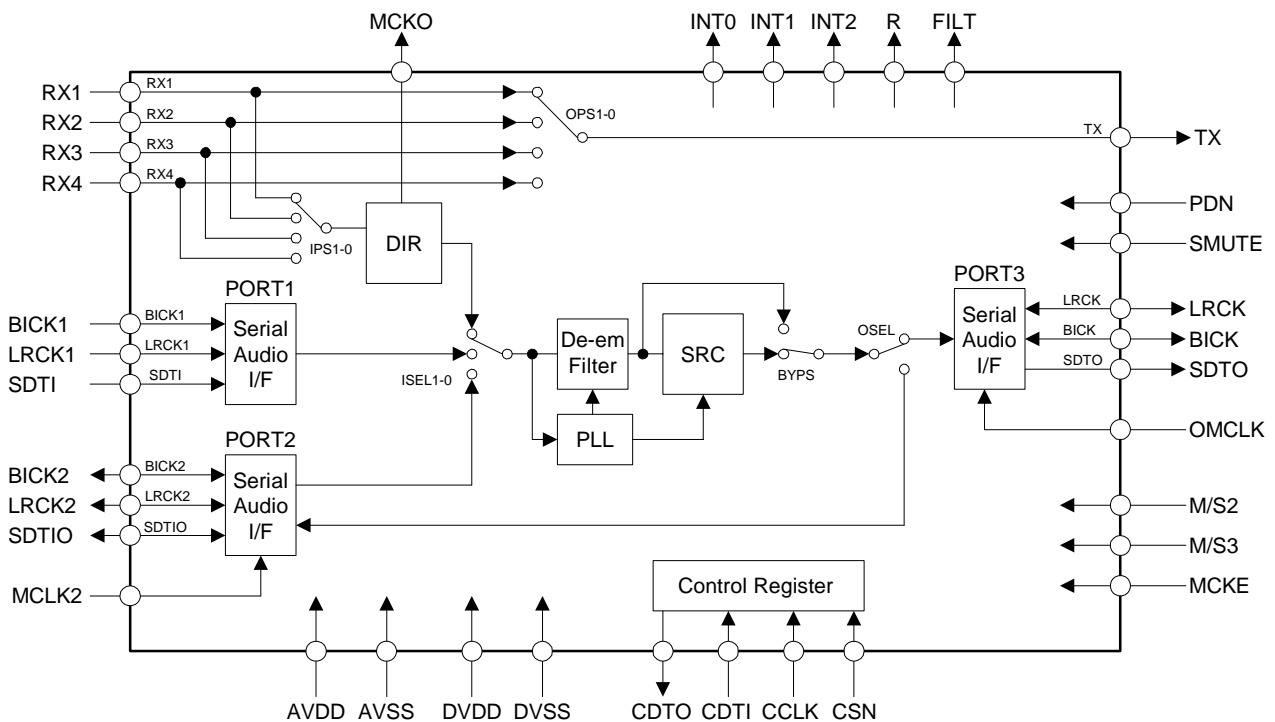


Figure 2. AK4122A Block Diagram

(1) AK4122A PORT1 → SRC → AK4122A PORT3

Refer to page 5 for input port setting, and page 15 ~ 18 for output port setting.

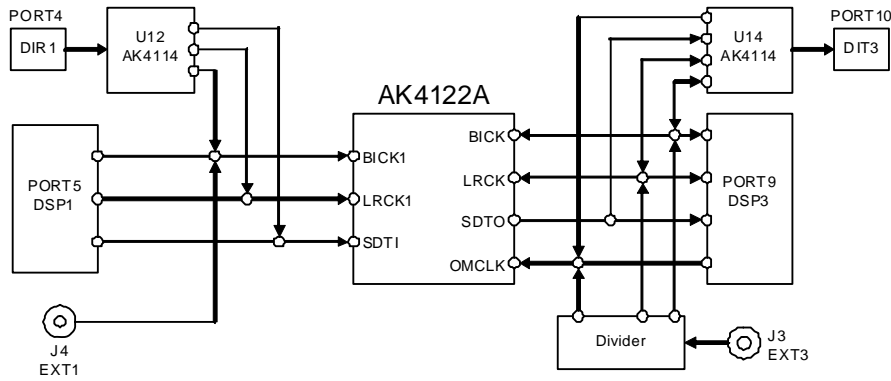


Figure 3. AK4122A PORT1 → SRC → AK4122A PORT3

(2) AK4122A PORT2 → SRC → AK4122A PORT3

Refer to page 6 ~ 9 for input port setting, and page 15 ~ 18 for output port setting.

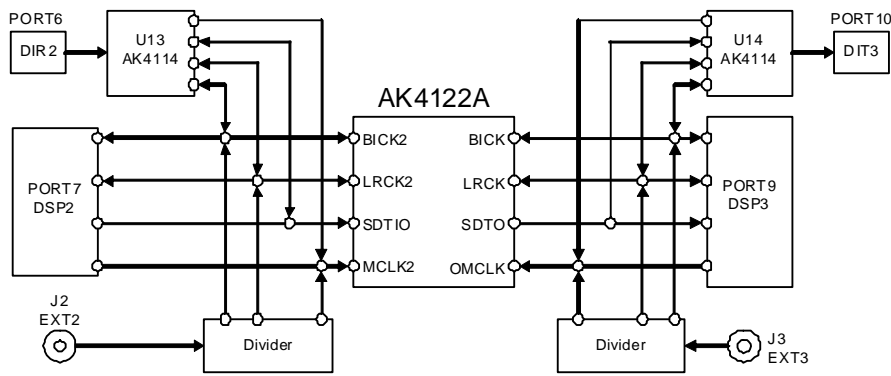


Figure 4. AK4122A PORT2 → SRC → AK4122A PORT3

(3) AK4122A DIR → SRC → AK4122A PORT3

Refer to page 10 for input port setting, and page 15 ~ 18 for output port setting.

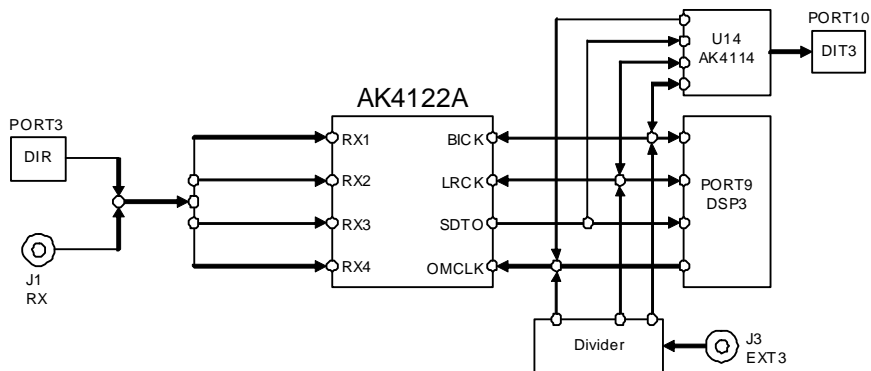


Figure 5. AK4122A DIR → SRC → AK4122A PORT3

(4) AK4122A PORT1 → SRC → AK4122A PORT2

Refer to page 5 for input port setting, and page 11 ~ 14 for output port setting.

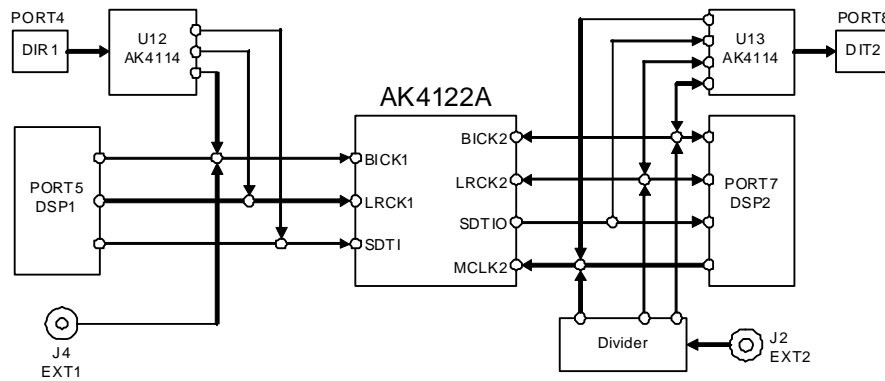


Figure 6. AK4122A PORT1 → SRC → AK4122A PORT2

(5) AK4122A DIR → SRC → AK4122A PORT2

Refer to page 10 for input port setting, and page 11 ~ 14 for output port setting.

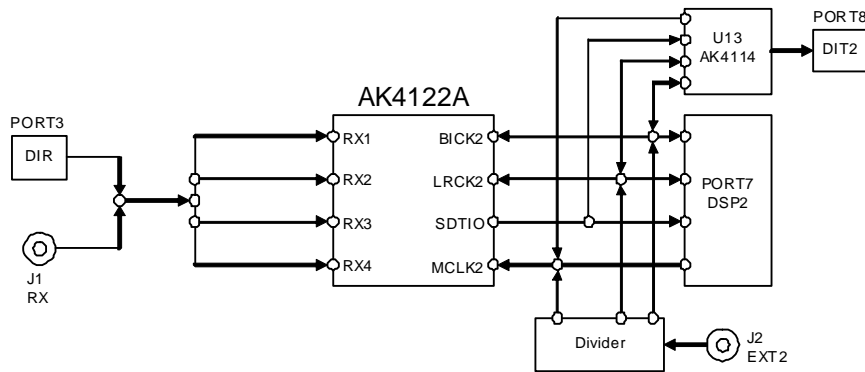


Figure 7. AK4122A DIR → SRC → KA4122 PORT2

(6) Bypass Mode

Refer to page 5 ~ 10 for input port setting, and output port setting should be master mode. The bypass mode of the AK4122A is set by the register.

In bypass mode, the DIT function of the AK4114 can not be used as the output port. 10pin PORT should be used instead.

Input BICK, LRCK, and DATA are output from the output port side in the bypass mode.

(1) Setting for Input port (AK4122A PORT1)

(1-1) Slave Mode

1. When using DIR function of AK4114 (U12)

When using PORT4 (DIR1), nothing should be connected to J4 (EXT1) and PORT5 (DSP1). JP12 (EXT1) should be short.



- SW2 setting (See Table 1, Table 2)
Upper-side is "H" and lower-side is "L".

SW2 No.	Name	ON ("H")	OFF ("L")
1	OCKS	Fixed to "L"	
2	DIF0	AK4114 Audio Format Setting Refer to Table 2	
3	DIF1		
4	DIF2		

Table 1. SW2 setting

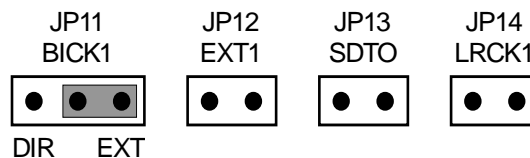
Mode	Audio I/F Format	AK4114			AK4122A		Default
		DIF2	DIF1	DIF0	DIF1	DIF0	
0	16bit, LSB justified	0	0	0	0	0	
1	24bit, MSB justified	1	0	0	0	1	Default
2	24bit, I ² S Compatible	1	0	1	1	0	
3	24bit, LSB justified	0	1	1	1	1	

Table 2. AK4114 Audio interface format setting

* **DIF1-0 of the AK4122A is set by the register.**

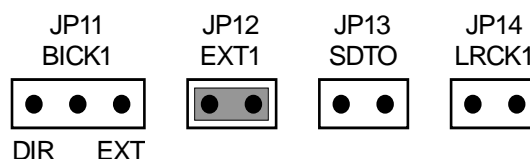
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT5 (DSP1), nothing should be connected to PORT4 (DIR1). BICK is input from J4 (EXT1), and the LRCK and SDTI are supplied from UPD. JP12 (EXT1) should be open.



3. All clocks are fed through the 10pin port

When using PORT5 (DSP1), nothing should be connected to J4 (EXT1) and PORT4 (DIR1). JP12 (EXT1) should be short.

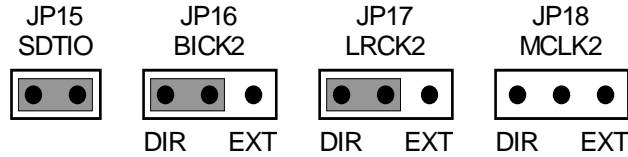


(2) Setting for Input port (AK4122A PORT2)

(2-1) Slave mode

1. When using DIR function of AK4114 (U13)

When using PORT6 (DIR2), nothing should be connected to J2 (EXT2) and PORT7 (DSP2). Set JP18 (MCLK2) to the “DIR” when MCLK is supplied to the AK4122A.



- SW3 setting (See Table 3, Table 4, Table 5)
Upper-side is “H” and lower-side is “L”.

SW3 No.	Name	ON (“H”)	OFF (“L”)
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 4	
2	DIF0	AK4114 Audio Format Setting Refer to Table 5	
3	DIF1		
4	DIF2		

Table 3. SW3 setting

Mode	OCKS	MCKO1	X’tal	fs	
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 4. AK4114 MCKO1 setting

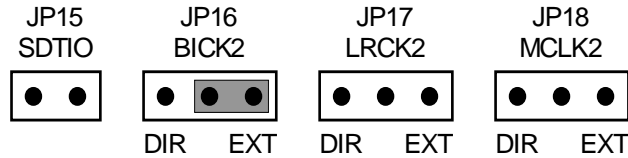
Mode	Audio I/F Format	AK4114			AK4122A		Default
		DIF2	DIF1	DIF0	IDIF1	IDIF0	
0	16bit, LSB justified	0	0	0	0	0	Default
1	24bit, MSB justified	1	0	0	0	1	
2	24bit, I ² S Compatible	1	0	1	1	0	
3	24bit, LSB justified	0	1	1	1	1	

Table 5. AK4114 Audio interface format setting

* IDIF1-0 of the AK4122A is set by the register.

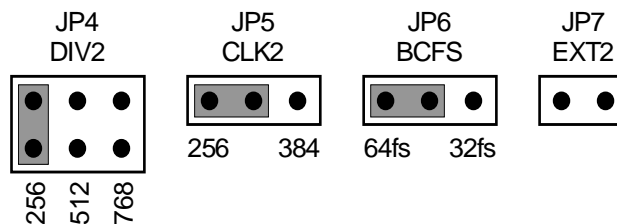
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2). MCLK is input from J2 (EXT2), BICK is supplied by using the clock dividing circuit on this evaluation board and the LRCK and SDTI are supplied from UPD. Set JP18 (MCLK2) to the “EXT” when MCLK is supplied to the AK4122A.



• Clock Setting

MCLK is input from J2 (EXT2), BICK is supplied by using the clock dividing circuit. JP4 (DIV2) and JP5 (CLK2) are set by referring to Table 6. JP6 (BCFS) selects the frequency of BICK. JP7 (EXT2) should be open.

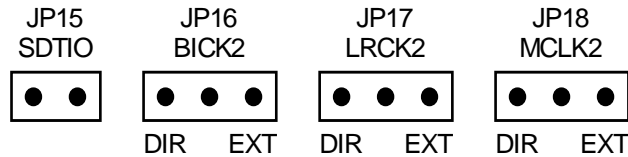


fs	MCLK	JP4(DIV2)	JP5(CLK2)
8kHz	256fs = 2.048MHz	256	256
	384fs = 3.072MHz	Open	384
	512fs = 4.096MHz	512	256
	768fs = 6.144MHz	768	256
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 6. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short.

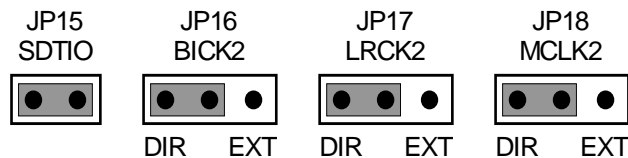


(2-2) Master mode

MCLK must be provided in the master mode.

1. When using DIR function of AK4114 (U13)

When using PORT6 (DIR2), nothing should be connected to J2 (EXT2) and PORT7 (DSP2). Set JP18 (MCLK2) to the “DIR” in order to supply MCLK to the AK4122A.



- SW3 setting (See Table 7, Table 8, Table 9)
Upper-side is “H” and lower-side is “L”.

SW3 No.	Name	ON (“H”)	OFF (“L”)
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 8	
2	DIF0	AK4114 Audio Format Setting Refer to Table 9	
3	DIF1		
4	DIF2		

Table 7. SW3 setting

Mode	OCKS	MCKO1	X’tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 8. AK4114 MCKO1 setting

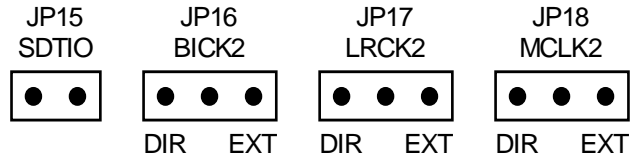
Mode	Audio I/F Format	AK4114			AK4122A	
		DIF2	DIF1	DIF0	IDIF1	IDIF0
0	24bit, MSB justified	1	1	0	0	1
1	24bit, I ² S Compatible	1	1	1	1	0

Table 9. AK4114 Audio interface format setting

* IDIF1-0 of the AK4122A is set by the register.

2. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short. MCLK is supplied to the AK4122A, and the DATA that synchronizes with BICK and LRCK output from the AK4122A is supplied to the AK4122A.



(2-3) SW1 setting

Set SW1 according to the mode of the AK4122A PORT2.

SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	M/S2	Master Mode	Slave Mode	L
2	M/S3	Master Mode	Slave Mode	L
3	TST4	Fixed to "L"		L

Table 10. SW1 setting

(3) Setting for Input port (AK4122A DIR)

(3-1) Setting for DIR input

The signal source of AK4122A's DIR can be set by JP2 (RX) and JP3 (RX1-4).

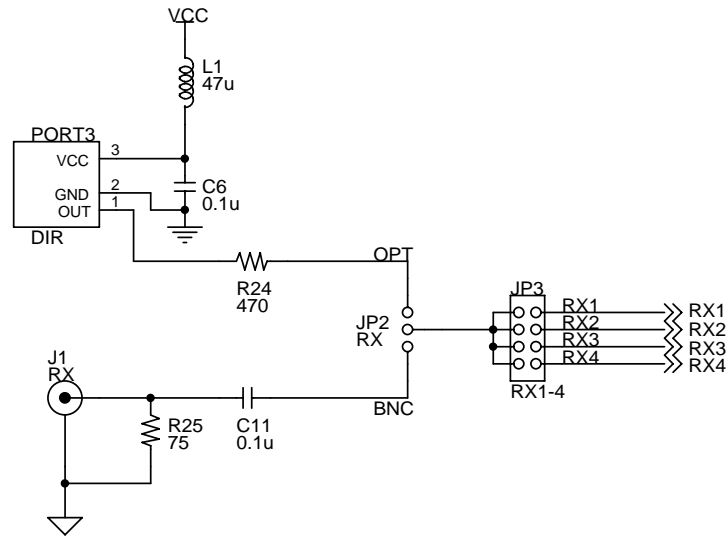


Figure 8. DIR input circuit

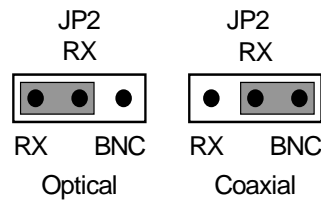


Figure 9. JP2 setting

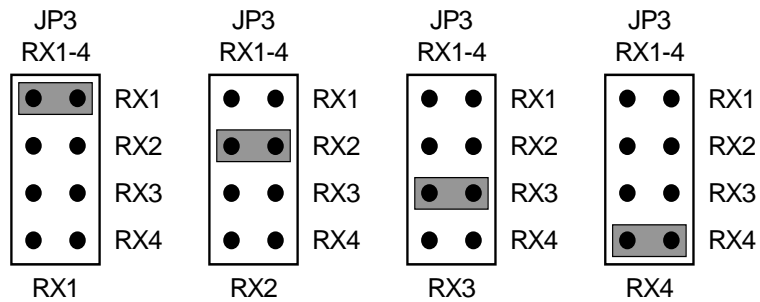


Figure 10. JP3 setting

(3-2) Setting for DIR through signal

DIR through signal of the AK4122A is output to TX pin via PORT2 (TX).

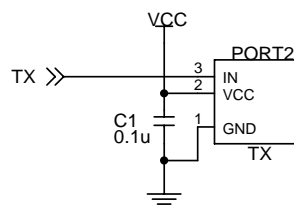


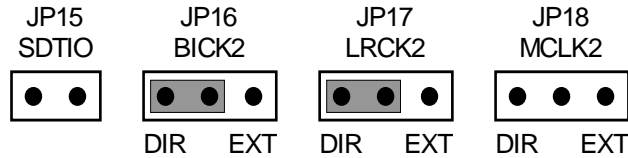
Figure 11. DIR through signal

(4) Setting for Output port (AK4122A PORT2)

(4-1) Slave mode

1. When using DIT function of AK4114 (U13)

When using X'tal (X1) and PORT8 (DIT2), nothing should be connected to PORT6 (DIR2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" when MCLK is supplied to the AK4122A. When MCLK frequency is changed, the value of X'tal (X1) frequency should be changed according to MCLK frequency.



- SW3 setting (See Table 11, Table 12, Table 13)
Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 12	
2	DIF0	AK4114 Audio Format Setting Refer to Table 13	
3	DIF1		
4	DIF2		

Table 11. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs	Default
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 12. AK4114 MCKO1 setting

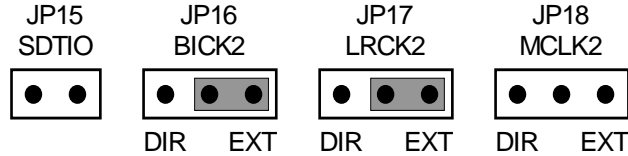
Mode	Audio I/F Format	AK4114			AK4122A		Default
		DIF2	DIF1	DIF0	IDIF1	IDIF0	
0	24bit, MSB justified	1	0	0	0	0	Default
1	24bit, MSB justified	1	0	0	0	1	
2	24bit, I ² S Compatible	1	0	1	1	0	
3	24bit, MSB justified	1	0	0	1	1	

Table 13. AK4114 Audio interface format setting

* IDIF1-0 of the AK4122A is set by the register.

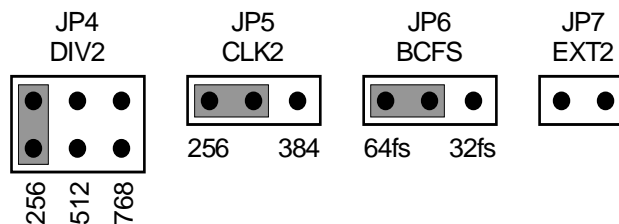
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2). MCLK is input from J2 (EXT2), BICK and LRCK are supplied by using the clock dividing circuit on this evaluation board to the AK4122A. Set JP18 (MCLK2) to the “EXT” when MCLK is supplied to the AK4122A.



- Clock Setting

MCLK is input from J2 (EXT2), BICK and LRCK are generated by using the clock dividing circuit. JP4 (DIV2) and JP5 (CLK2) are set by referring to Table 14. JP6 (BCFS) selects the frequency of BICK. JP7 (EXT2) should be open.

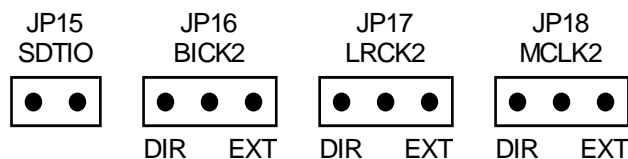


fs	MCLK	JP4(DIV2)	JP5(CLK2)
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 14. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short.

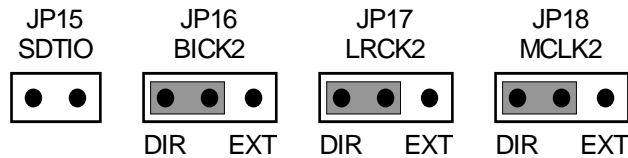


(4-2) Master mode

MCLK must be provided in the master mode.

1. When using DIT function of AK4114 (U13)

When using X'tal (X1) and PORT8 (DIT2), nothing should be connected to PORT6 (DIR2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" when MCLK is supplied to the AK4122A. When MCLK frequency is changed, the value of X'tal (X1) frequency should be changed according to MCLK frequency.



- SW3 setting (See Table 15, Table 16, Table 17)
Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 16	
2	DIF0	AK4114 Audio Format Setting Refer to Table 17	
3	DIF1		
4	DIF2		

Table 15. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 16. AK4114 MCKO1 setting

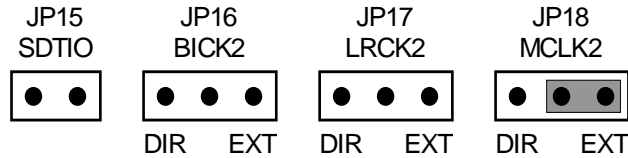
Mode	Audio I/F Format	AK4114			AK4122A	
		DIF2	DIF1	DIF0	IDIF1	IDIF0
0	24bit, MSB justified	1	1	0	0	1
1	24bit, I ² S Compatible	1	1	1	1	0

Table 17. AK4114 Audio interface format setting

* IDIF1-0 of the AK4122A is set by the register.

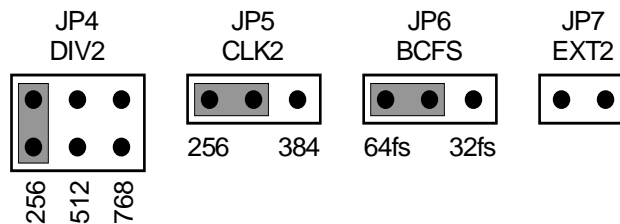
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2) and PORT8 (DIT2). MCLK is input from J2 (EXT2), BICK LRCK, and DATA are supplied from the AK4122A. Set JP18 (MCLK2) to the “EXT” in order to supply MCLK to the AK4122A.



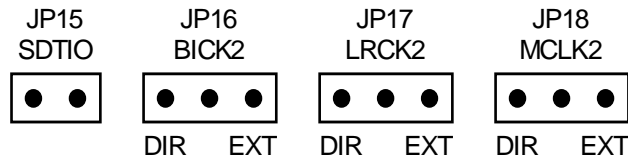
• Clock Setting

MCLK is input from J2 (EXT2). JP7 (EXT2) should be open.



3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2), PORT6 (DIR2) and PORT8 (DIT2). JP7 (EXT2) should be short. MCLK is supplied to the AK4122A, and BICK, LRCK and DATA are supplied from the AK4122A.



(4-3) SW1 setting

Set SW1 according to the mode of the AK4122A PORT2.

SW1 No.	Name	ON (“H”)	OFF (“L”)	Default
1	M/S2	Master Mode	Slave Mode	L
2	M/S3	Master Mode	Slave Mode	L
3	TST4	Fixed to “L”		L

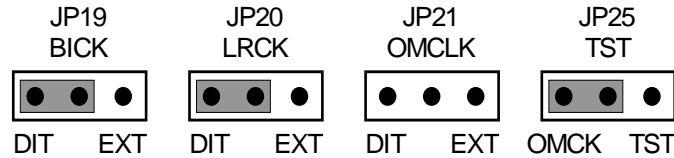
Table 18. SW1 setting

(5) Setting for Output port (AK4122A PORT3)

(5-1) Slave mode

1. When using DIT function of AK4114 (U14)

When using X'tal (X2) and PORT10 (DIT3), nothing should be connected to PORT9 (DSP3). Please set JP21 (OMCLK) to the "DIT" when MCLK is supplied to the AK4122A. When MCLK frequency is changed, the value of X'tal (X2) frequency should be changed according to MCLK frequency.



- SW4 setting (See Table 19, Table 20, Table 21)
Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 20	
2	DIF0	AK4114 Audio Format Setting Refer to Table 21	

Table 19. SW4 setting

Mode	OCKS	MCKO1	X'tal	fs	
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 20. AK4114 MCKO1 setting

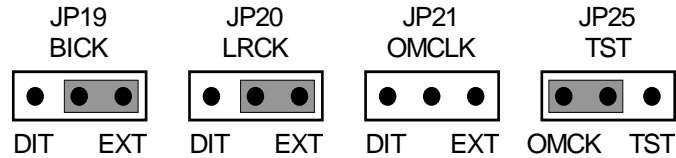
Mode	Audio I/F Format	AK4114	AK4122A	
		DIF0	ODIF	
0	24bit, MSB justified	0	0	Default
1	24bit, I ² S Compatible	1	1	

Table 21. AK4114 Audio interface format setting

* **ODIF of the AK4122A is set by the register.**

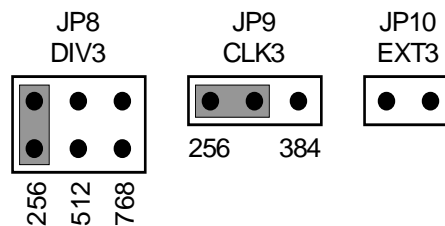
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). MCLK is input from J3 (EXT3), BICK and LRCK are supplied by using the clock dividing circuit on this evaluation board to the AK4122A. Set JP21 (OMCLK) to the “EXT” when MCLK is supplied to the AK4122A.



- Clock Setting

MCLK is input from J3 (EXT3), BICK and LRCK are generated by using the clock dividing circuit. JP8 (DIV3) and JP9 (CLK3) are set by referring to Table 22. JP10 (EXT3) should be open.

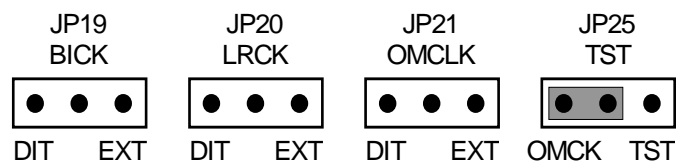


fs	MCLK	JP8(DIV3)	JP9(CLK3)
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 22. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). Set JP25 (TST) to the “OMCK” when MCLK is supplied to the AK4122A. JP10 (EXT3) should be short.

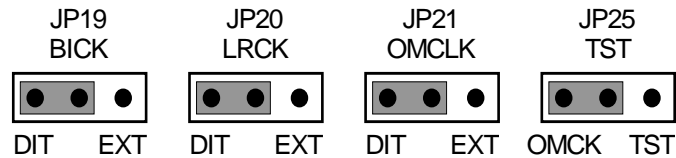


(5-2) Master mode

MCLK must be provided in the master mode.

1. When using DIT function of AK4114 (U14)

When using X'tal (X2) and PORT10 (DIT3), nothing should be connected to PORT9 (DSP3). Set JP21 (OMCLK) to the "DIT" in order to supply MCLK to the AK4122A. When MCLK frequency is changed, the value of X'tal (X2) frequency should be changed according to MCLK frequency.



- SW4 setting (See Table 23, Table 24, Table 25)
Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 24	
2	DIF0	AK4114 Audio Format Setting Refer to Table 25	

Table 23. SW4 setting

Mode	OCKS	MCKO1	X'tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 24. AK4114 MCKO1 setting

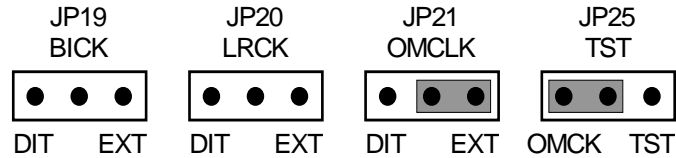
Mode	Audio I/F Format	AK4114	AK4122A
		DIF0	ODIF
0	24bit, MSB justified	0	0
1	24bit, I ² S Compatible	1	1

Table 25. AK4114 Audio interface format setting

* ODIF of the AK4122A is set by the register.

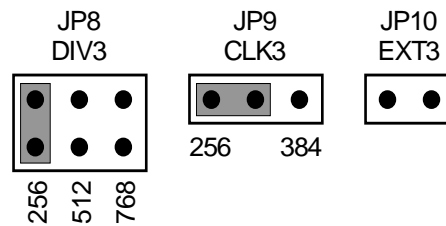
2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). MCLK is input from J3 (EXT3), BICK LRCK, and DATA are supplied from the AK4122A. Set JP21 (OMCLK) to the “EXT” in order to supply MCLK to the AK4122A.



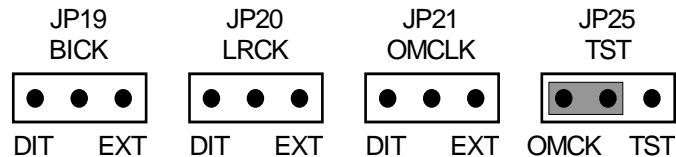
- Clock Setting

MCLK is input from J3 (EXT3). JP10 (EXT3) should be open.



3. All clocks are fed through the 10pin port

When using PORT9 (DSP3), nothing should be connected to J3 (EXT3) and PORT10 (DIT3). Set JP25 (TST) to the “OMCK” in order to supply MCLK to the AK4122A. JP10 (EXT3) should be short. MCLK is supplied to the AK4122A, and BICK, LRCK and DATA are supplied from the AK4122A.



(5-3) SW1 setting

Set SW1 according to the mode of the AK4122A PORT3.

SW1 No.	Name	ON (“H”)	OFF (“L”)	Default
1	M/S2	Master Mode	Slave Mode	L
2	M/S3	Master Mode	Slave Mode	L
3	TST4	Fixed to “L”		L

Table 26. SW1 setting

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
OPEN: Separated.
SHORT: Common. (The connector “DGND” can be open.) <Default>
2. JP22 (VDD2) : DVDD and VCC
OPEN: Separated.
SHORT: Common. (The connector “VCC” can be open.) <Default>
3. JP23 (VDD1) : AVDD and DVDD
OPEN: Separated.
SHORT: Common. (The connector “DVDD” can be open.) <Default>
4. JP24 (REG) : +5V and AVDD
OPEN: Separated.
SHORT: Common. (The connector “AVDD” can be open.) <Default>

The regulator can be supplied 3.3V to all circuits by shorting JP22, 23 and 24 and supplying 5V to +5V connector.

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW5] (SMUTE): Soft mute of AK4122A

[SW6] (PDN): Resets the AK4122A. Keep “H” during normal operation.

The AK4122A should be resets once bringing “L” upon power-up.

[SW7] (PDN1): Resets the AK4114 (U12). Keep “H” during normal operation.

The AK4114 (U12) should be resets once bringing “L” upon power-up.

Keep “L” when AK4114 (U12) is not used.

[SW8] (PDN2): Resets the AK4114 (U13). Keep “H” during normal operation.

The AK4114 (U13) should be resets once bringing “L” upon power-up.

Keep “L” when AK4114 (U13) is not used.

[SW9] (PDN3): Resets the AK4114 (U14). Keep “H” during normal operation.

The AK4114 (U14) should be resets once bringing “L” upon power-up.

Keep “L” when AK4114 (U14) is not used.

■ **Indication for LED**

[LED1] (ERF): Monitor INT0 pin of the AK4114 (U12). LED turns on when unlock or parity error occurs.

[LED2] (ERF): Monitor INT0 pin of the AK4114 (U13). LED turns on when unlock or parity error occurs.

[LED3] (INT0): Monitor INT0 pin of the AK4122A.

[LED4] (INT1): Monitor INT1 pin of the AK4122A.

[LED5] (INT2): Monitor INT2 pin of the AK4122A.

■ **Serial Control**

The AK4122A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (CTRL) with PC by 10 wire flat cable packed with the AKD4122A-A.

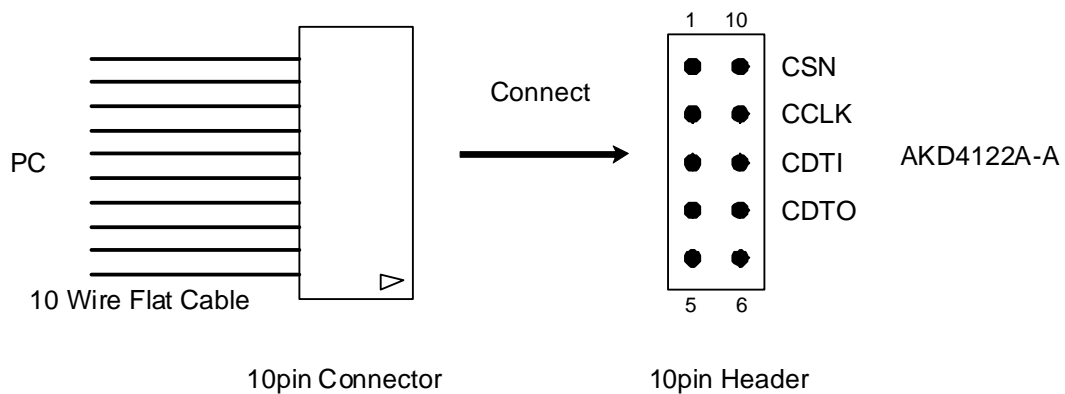


Figure 12. Connection of 10 wire flat cable

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4122A-A according to previous term.
2. Connect IBM-AT compatible PC with AKD4122A-A by 10-line type flat cable (packed with AKD4122A-A).
Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)
3. Insert the CD-ROM labeled "AK4122A Evaluation Kit" into the CD-ROM drive.
4. Access the CD-ROM drive and double-click the icon of "AKD4122A-A.exe" to set up the control program.
5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Setup" button.
3. Click "Write default" button.

Then set up the dialog and input data.

■ Explanation of each buttons

1. [Port Setup] : Set up the printer port.
2. [Write default] : Initialize the register of AK4122A.
3. [All Read] : Read the all register of AK4122A.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Write] : Dialog to write data by mouse operation.
6. [Read] : Read each register data by mouse operation.

■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input register address in 2 figures of hexadecimal.
Data Box: Input register data in 2 figures of hexadecimal.

If you want to write the input data to AK4122A, click "OK" button. If not, click "Cancel" button.

2. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the "Write" button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4122A, click "OK" button. If not, click "Cancel" button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- Power Supply : AVDD = DVDD = 3.3V
- Band width : 10Hz ~ FSO/2
- Temperature : Room
- Measurement Path : AK4122A PORT1 → SRC → AK4122A PORT3

[Measurement Result]

SRC Characteristics	Result	Unit
THD+N (Input = 1kHz, 0dBFS)		
FSO/FSI = 44.1kHz/48kHz	113.5	dB
FSO/FSI = 48kHz/44.1kHz	113.4	dB
FSO/FSI = 32kHz/48kHz	114.2	dB
FSO/FSI = 96kHz/32kHz	113.2	dB
Worst Case (FSO/FSI = 48kHz/8kHz)	111.7	dB
Dynamic Range (Input = 1kHz, -60dBFS)		
FSO/FSI = 44.1kHz/48kHz	115.1	dB
FSO/FSI = 48kHz/44.1kHz	115.1	dB
FSO/FSI = 32kHz/48kHz	115.3	dB
FSO/FSI = 96kHz/32kHz	115.2	dB
Worst Case (FSO/FSI = 32kHz/44.1kHz)	115.5	dB
Dynamic Range (Input = 1kHz, -60dBFS, A-weighted)		
FSO/FSI = 44.1kHz/48kHz	117.2	dB

[Plots]

AK4122A THD + N vs Input Level
FSI = 44.1kHz, SFO = 48kHz, fin = 1kHz

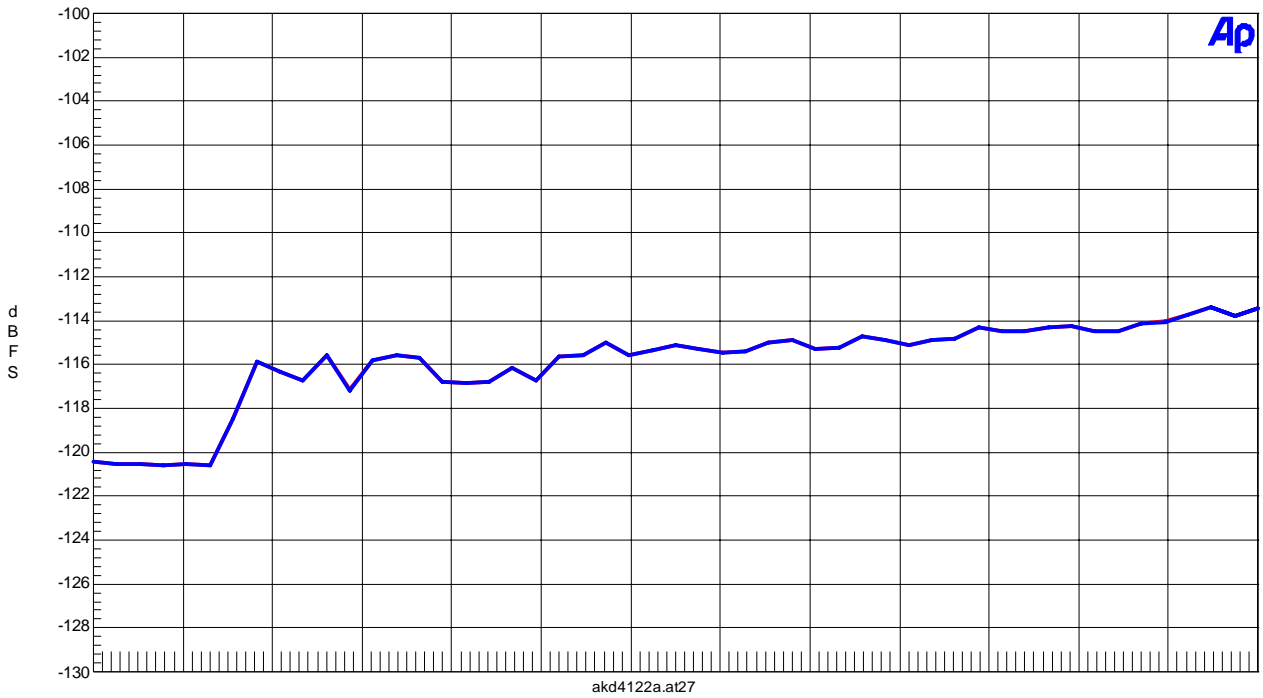


Figure 13. THD+N vs. Input Level

AK4122A THD + N vs Input Frequency
FSI = 44.1kHz, SFO = 48kHz, Input = 0dBFS

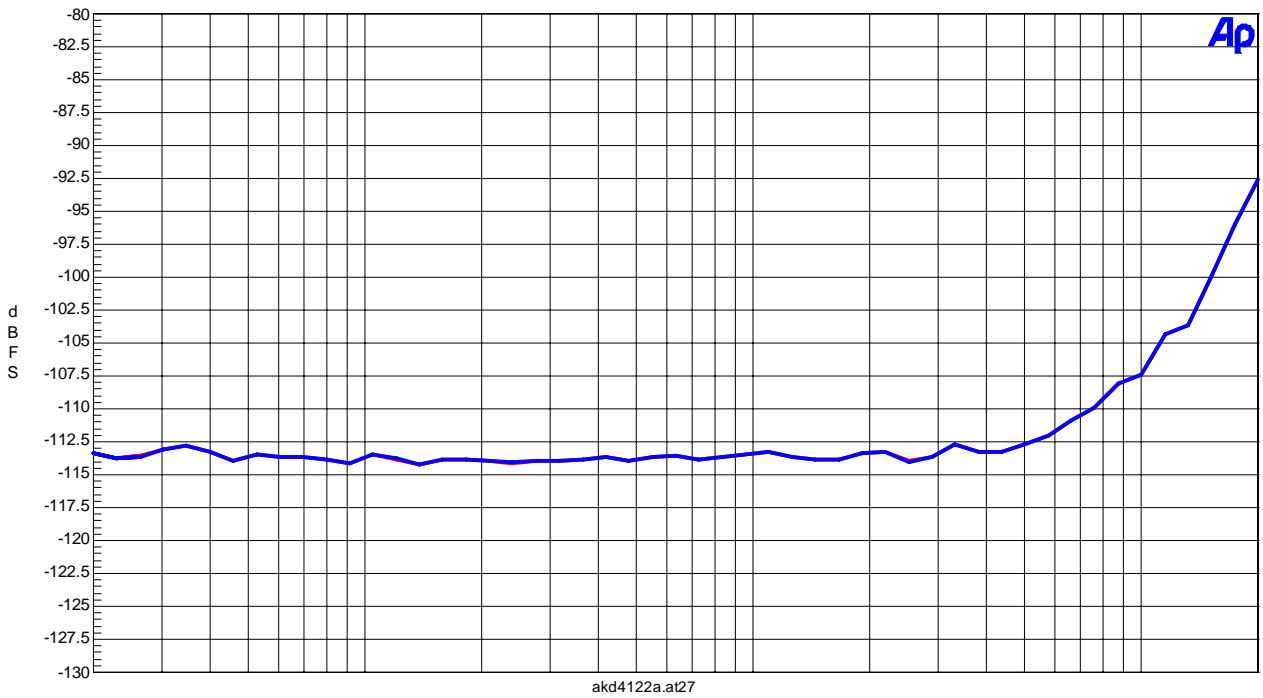


Figure 14. THD+N vs. Input Frequency (Input = 0dBFS)

AK4122A THD + N vs Input Frequency
FSI = 44.1kHz, SFO = 48kHz, Input = -60dBFS

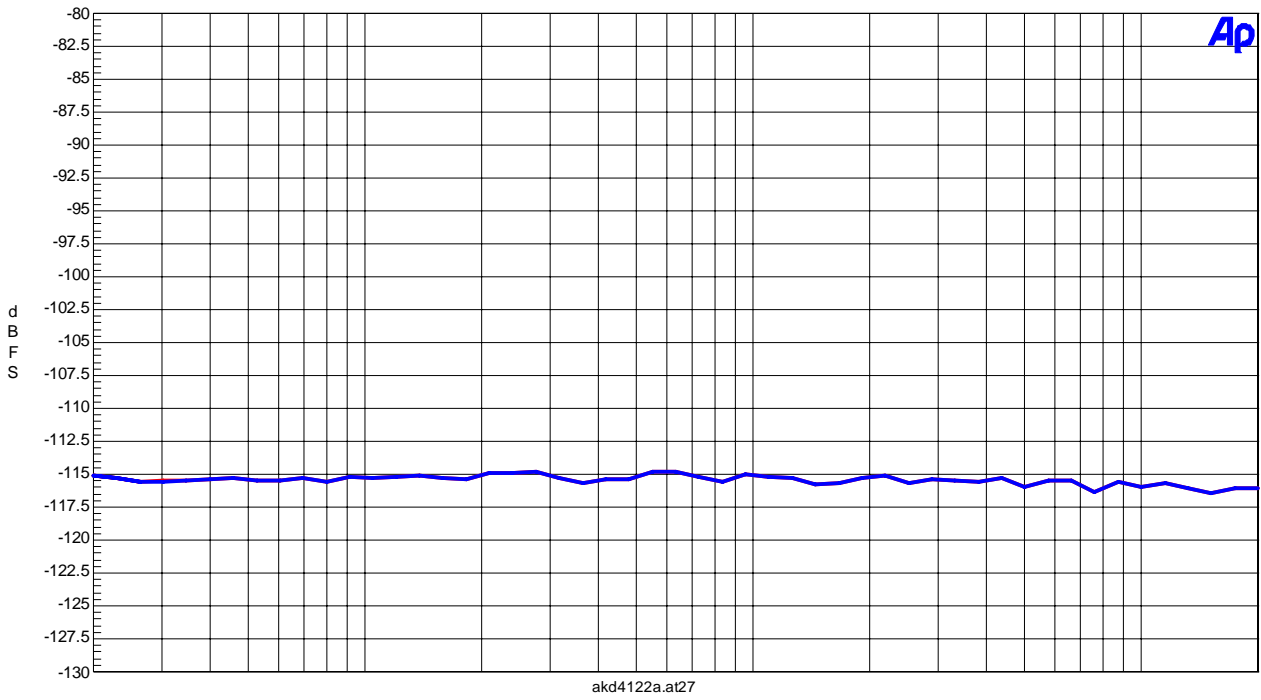


Figure 15. THD+N vs. Input Frequency (Input = -60dBFS)

AK4122A Linearity
FSI = 44.1kHz, SFO = 48kHz, fin = 1kHz

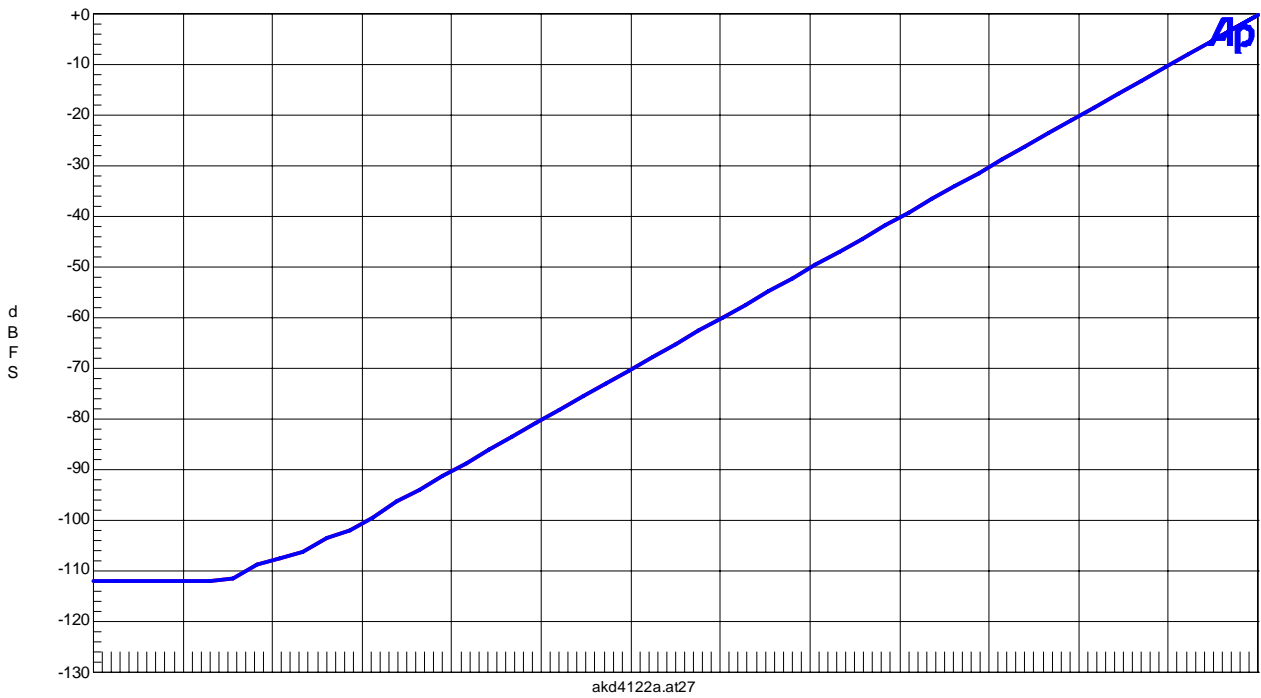


Figure 16. Linearity

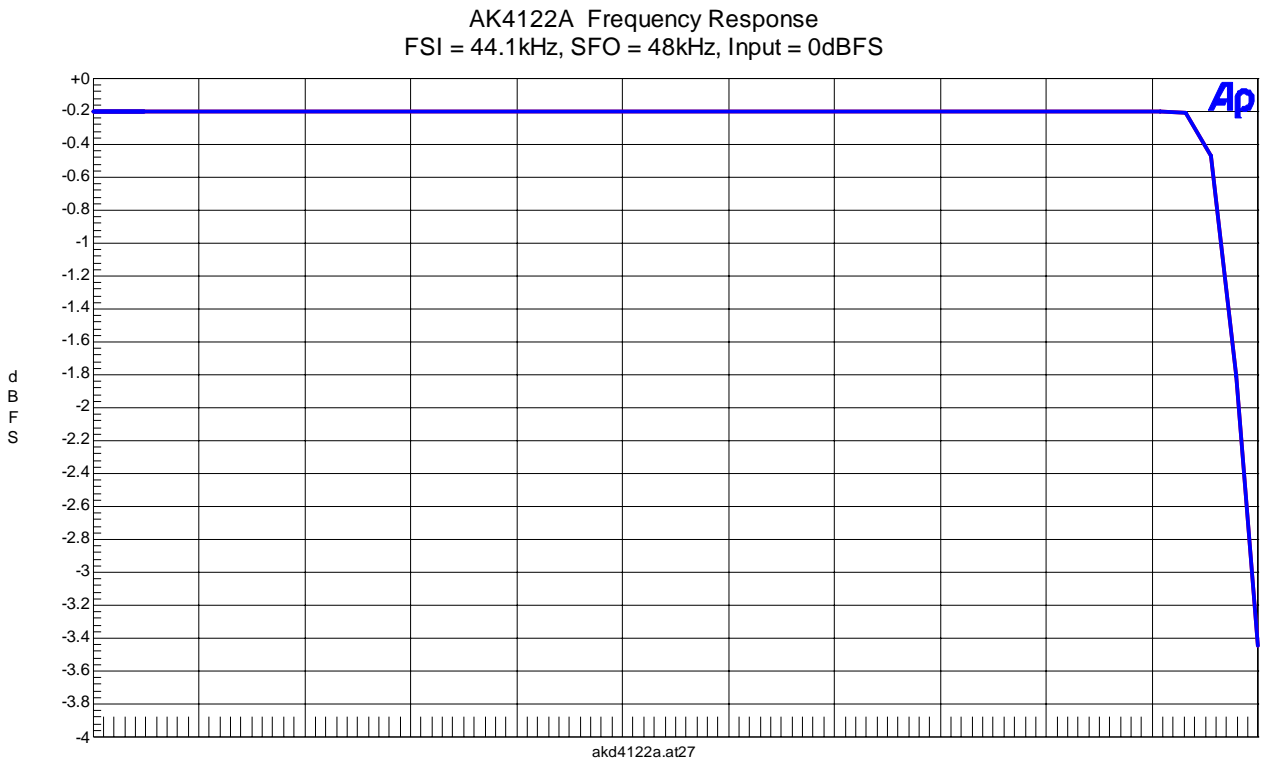


Figure 17. Frequency Response

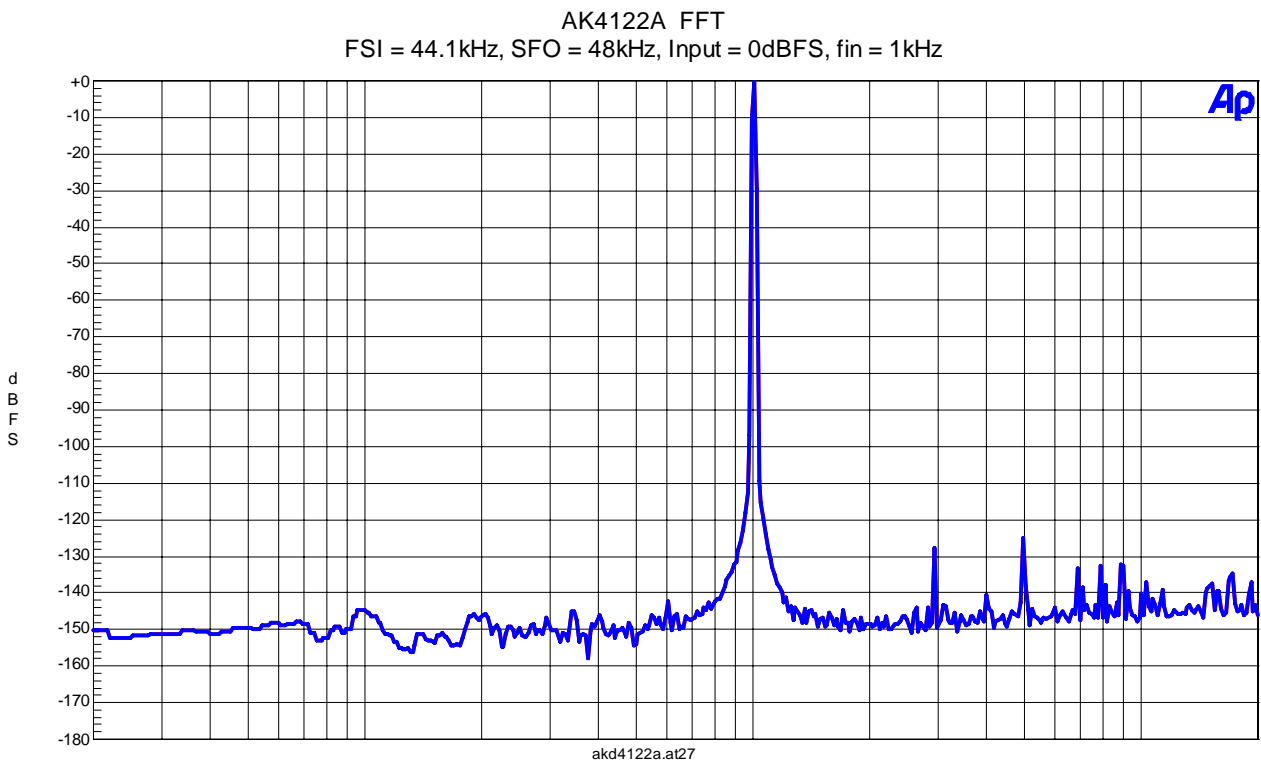


Figure 18. FFT Plot (Input = 0dBFS)

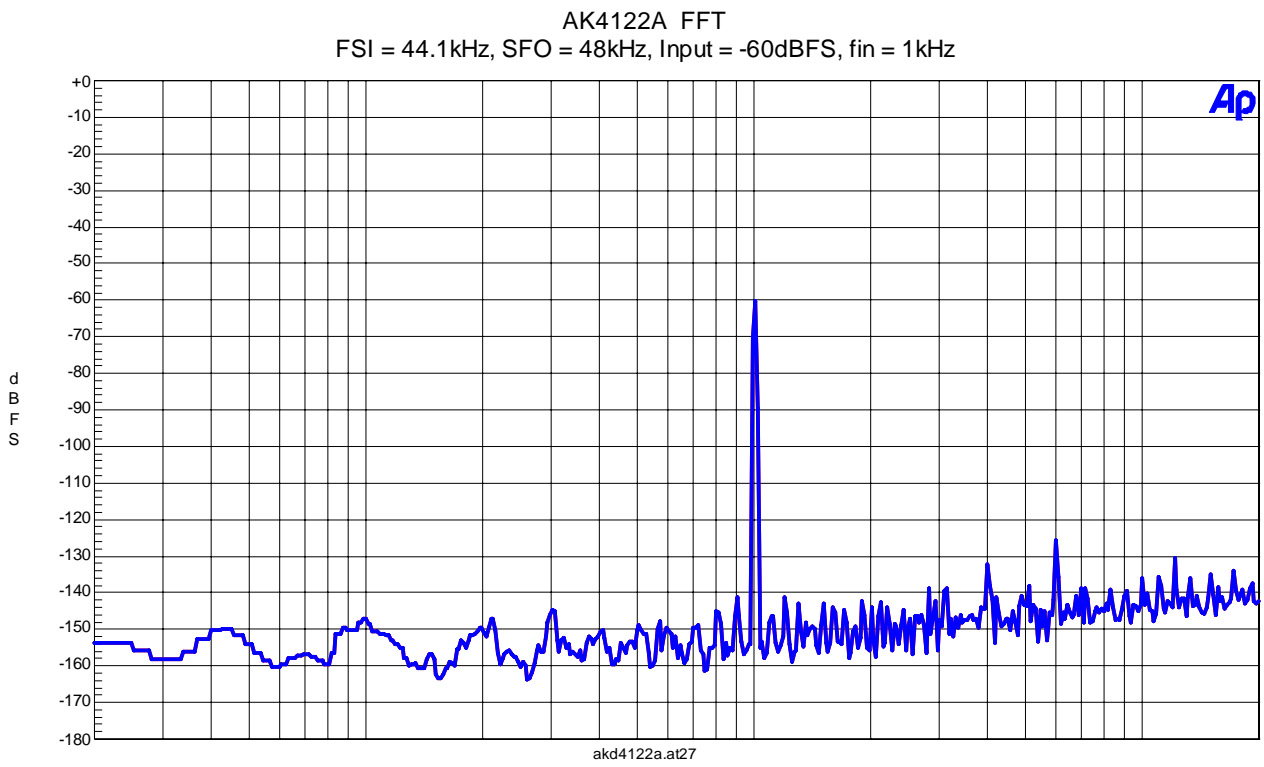


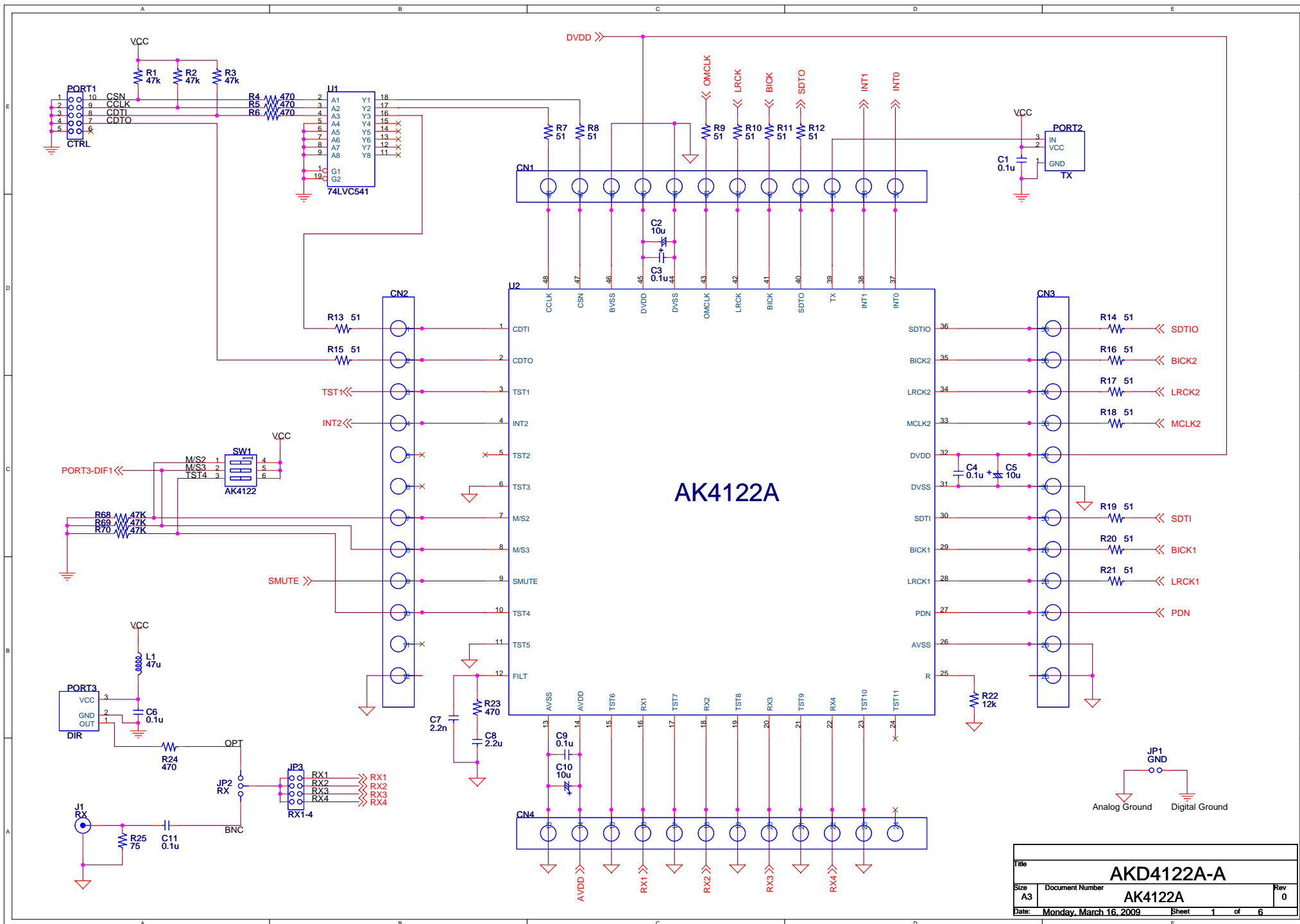
Figure 19. FFT Plot (Input = -60dBFS)

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
09/03/10	KM099400	0	First Edition		

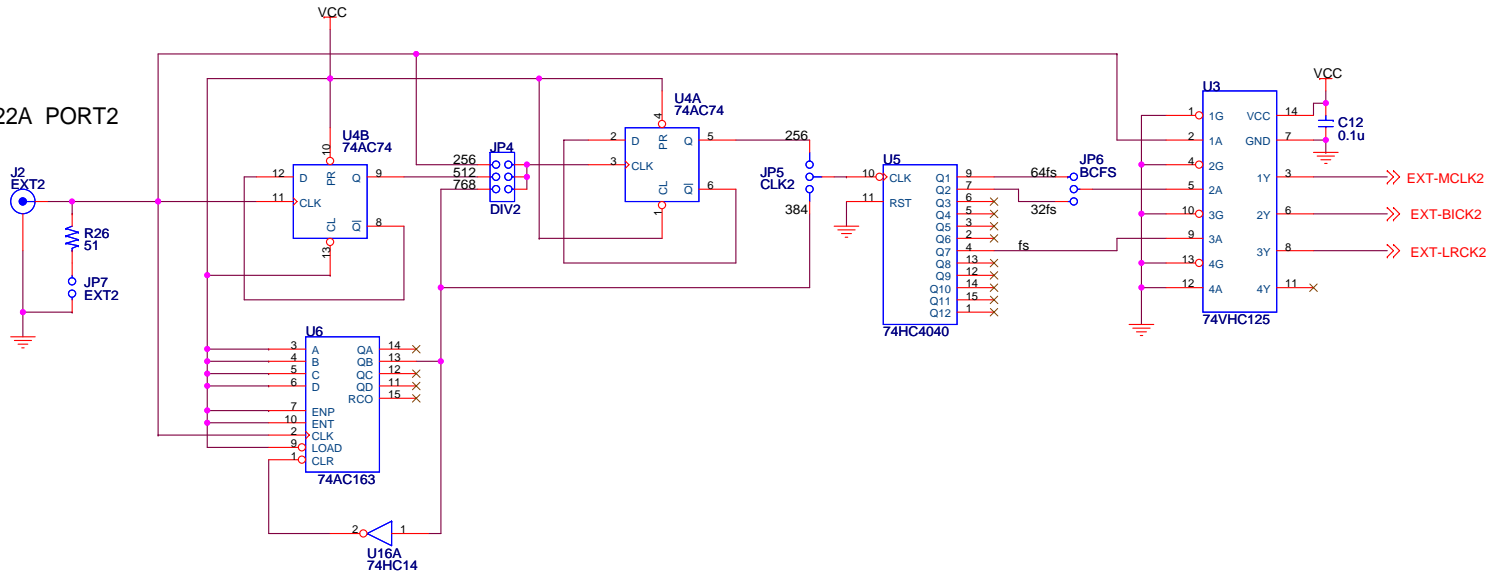
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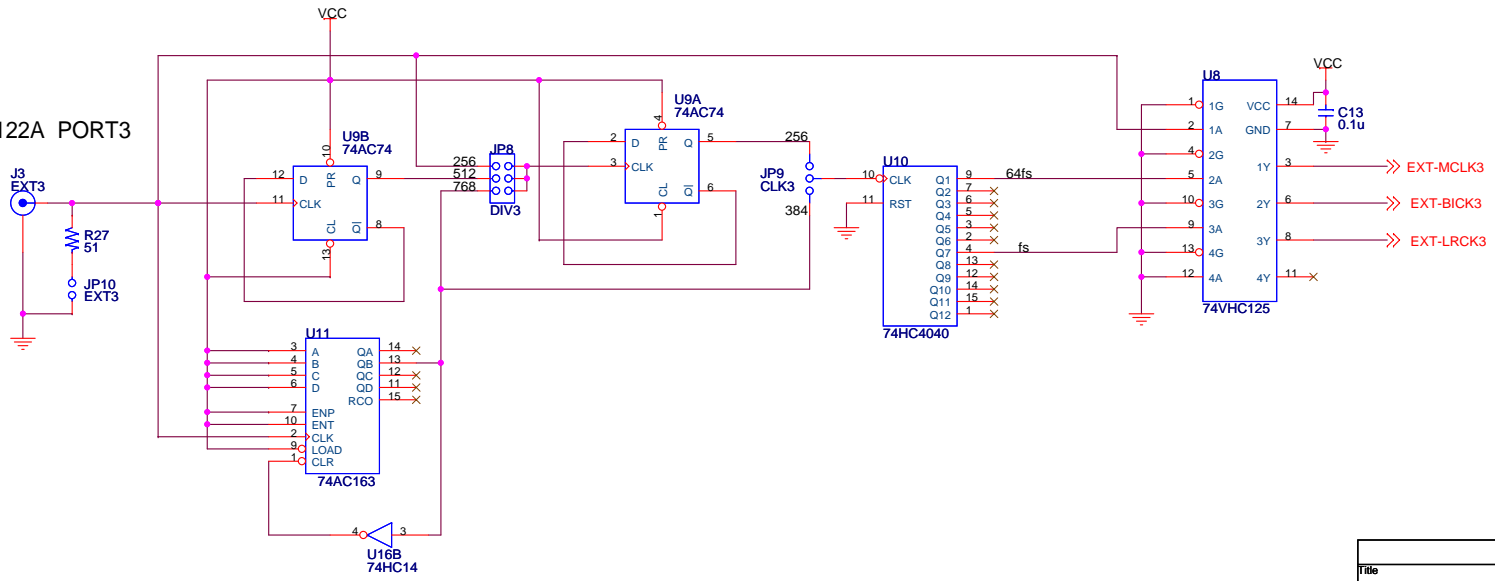


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Size	Document Number	AK4122A			Rev
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Date:	Monday, March 16, 2009	Sheet	1	of	6

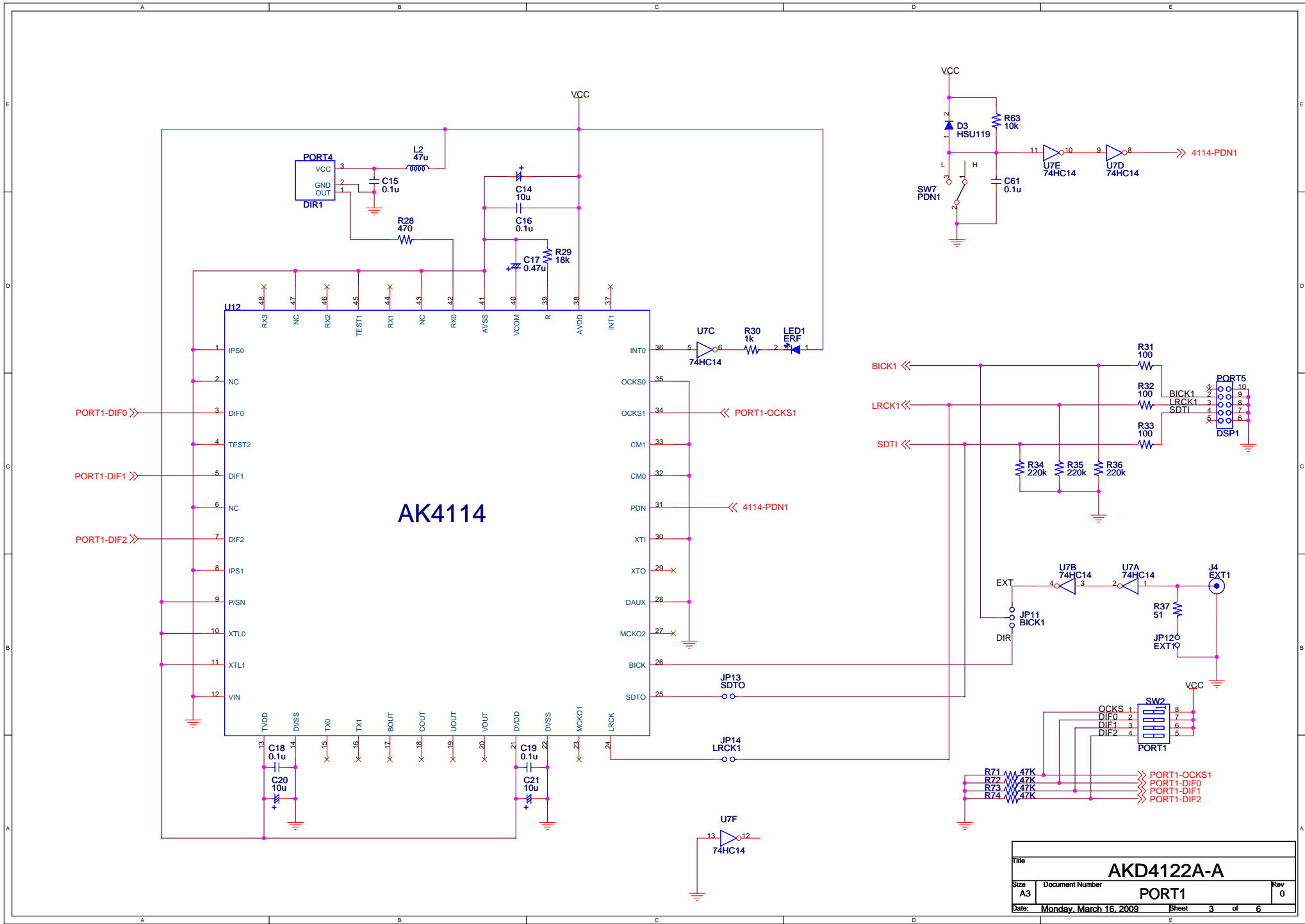
For AK4122A PORT2



For AK4122A PORT3

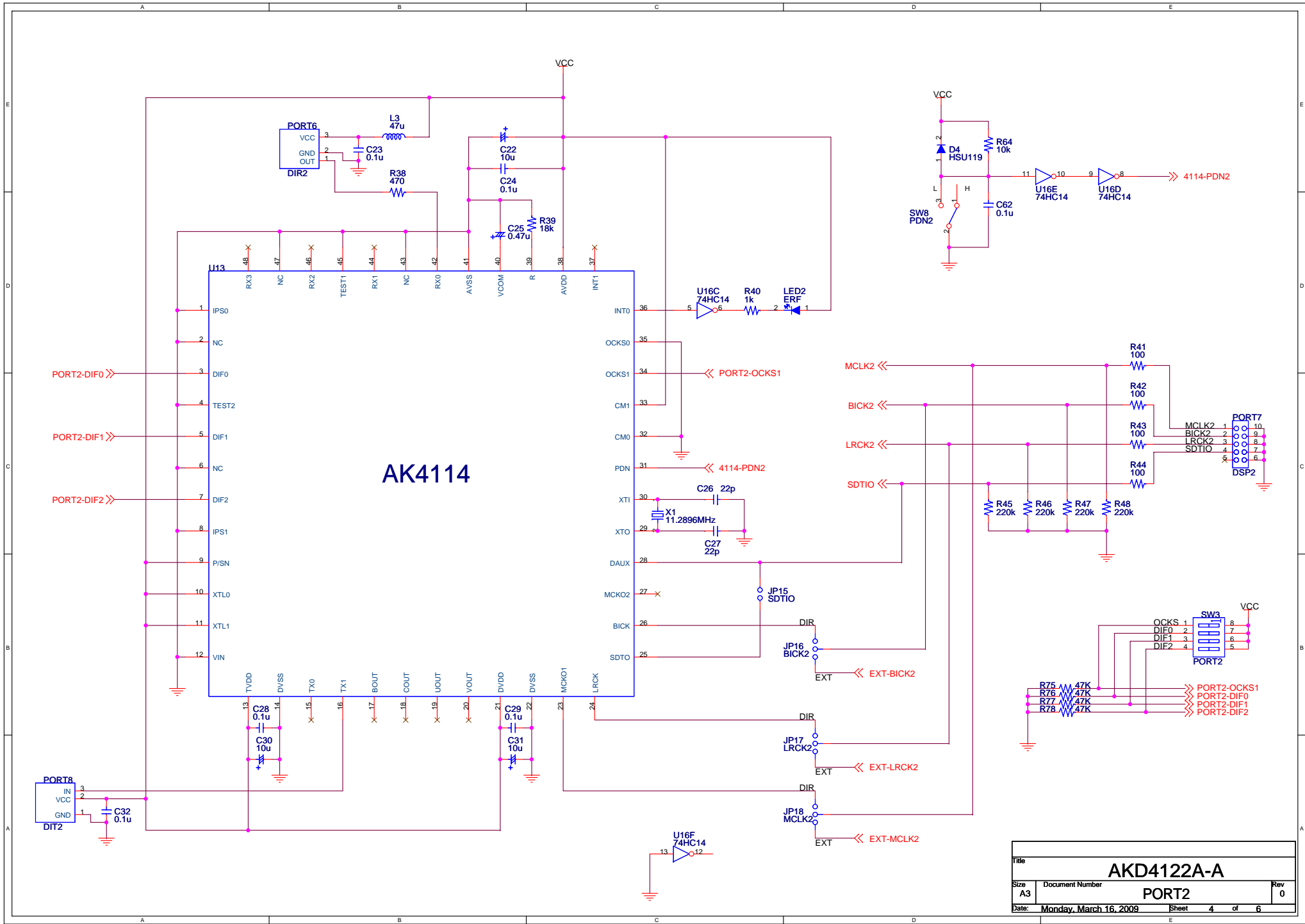


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Size	Document Number	External Clock		Rev	0
A3					
Date:	Monday, March 16, 2009	Sheet	2	of	6



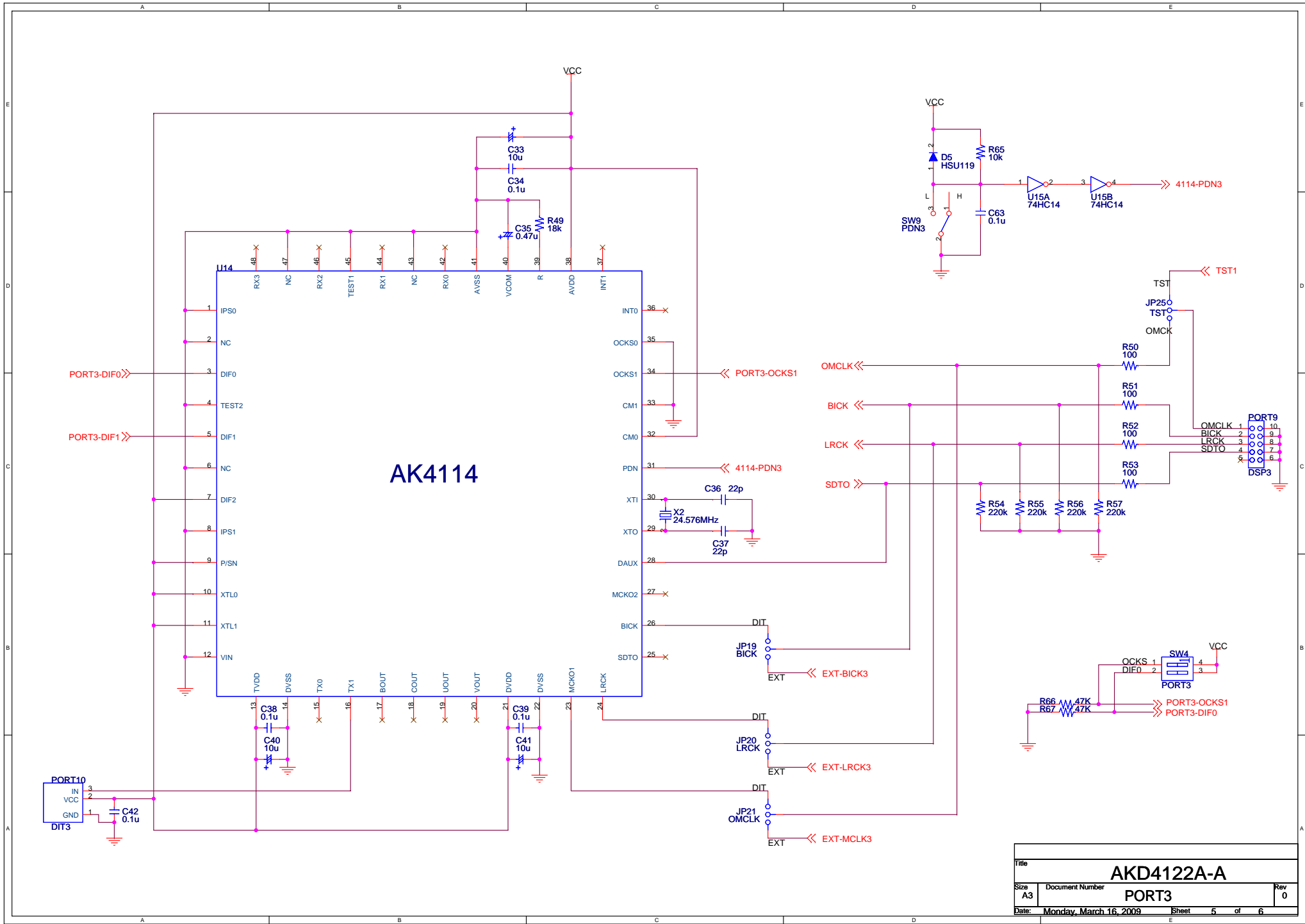
AK4114

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Size	Document Number	PORT1	
A3			Rev 0
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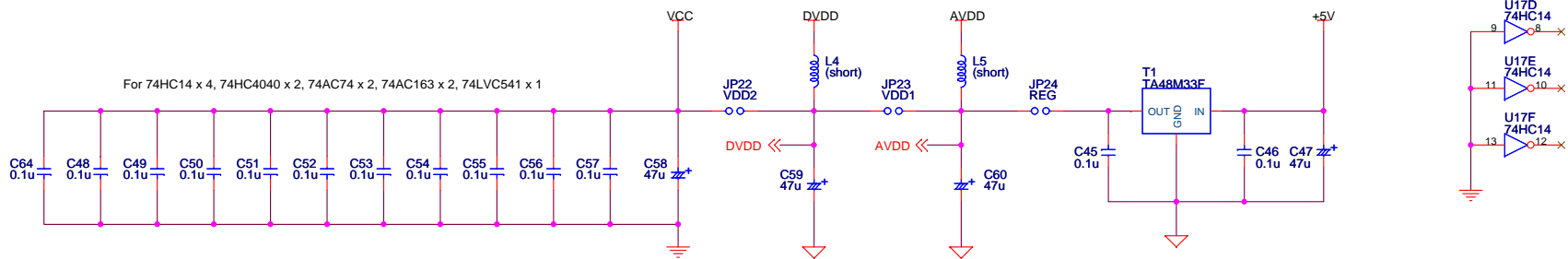
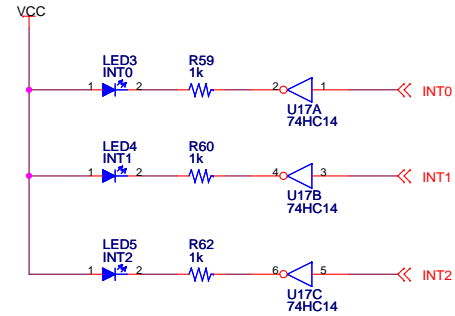
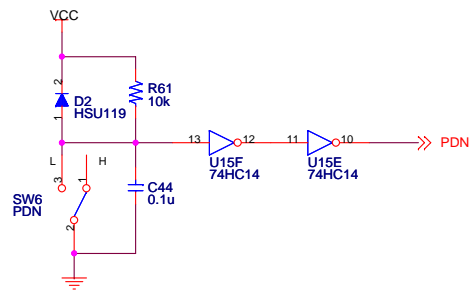
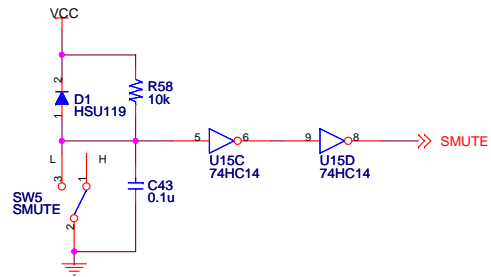
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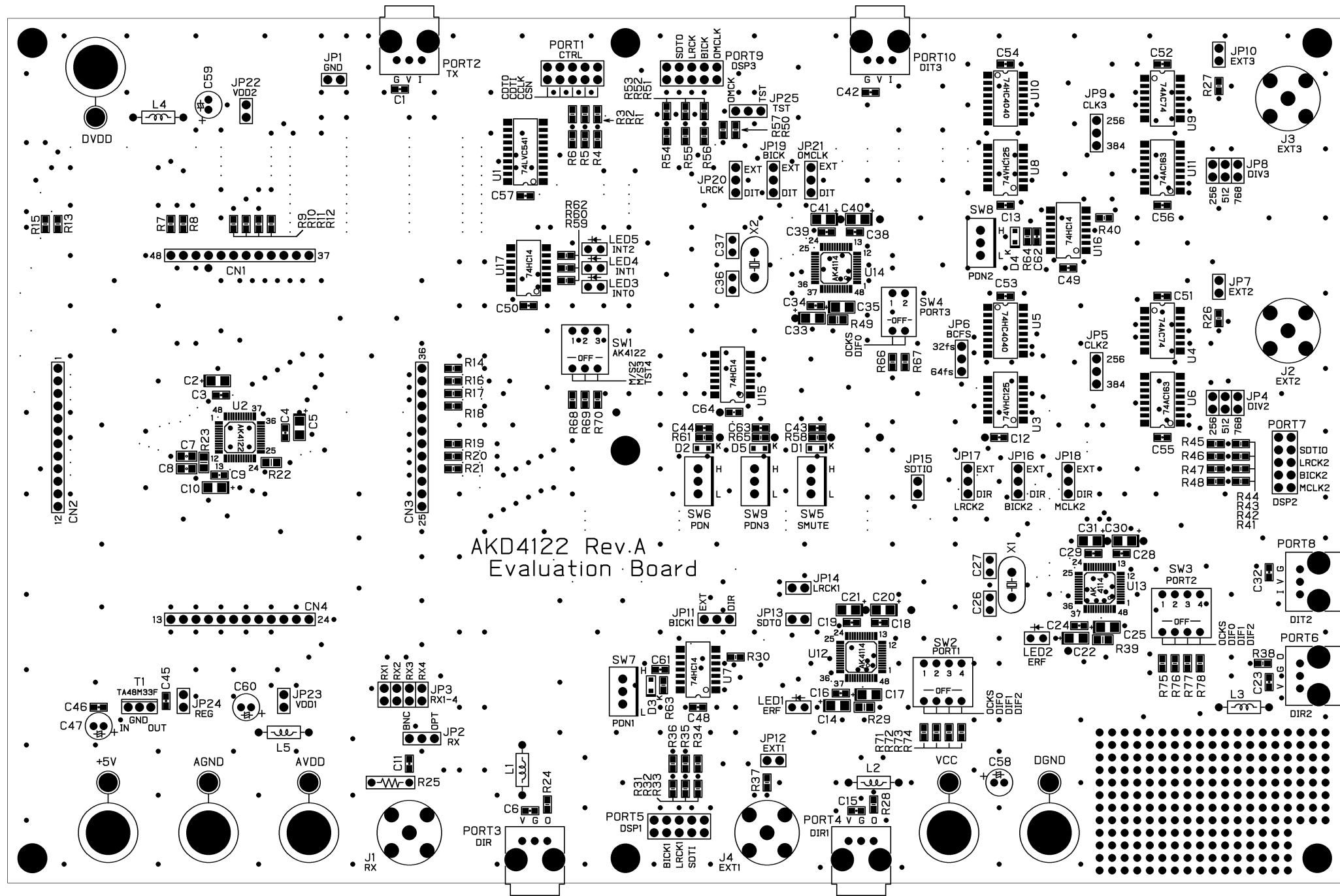


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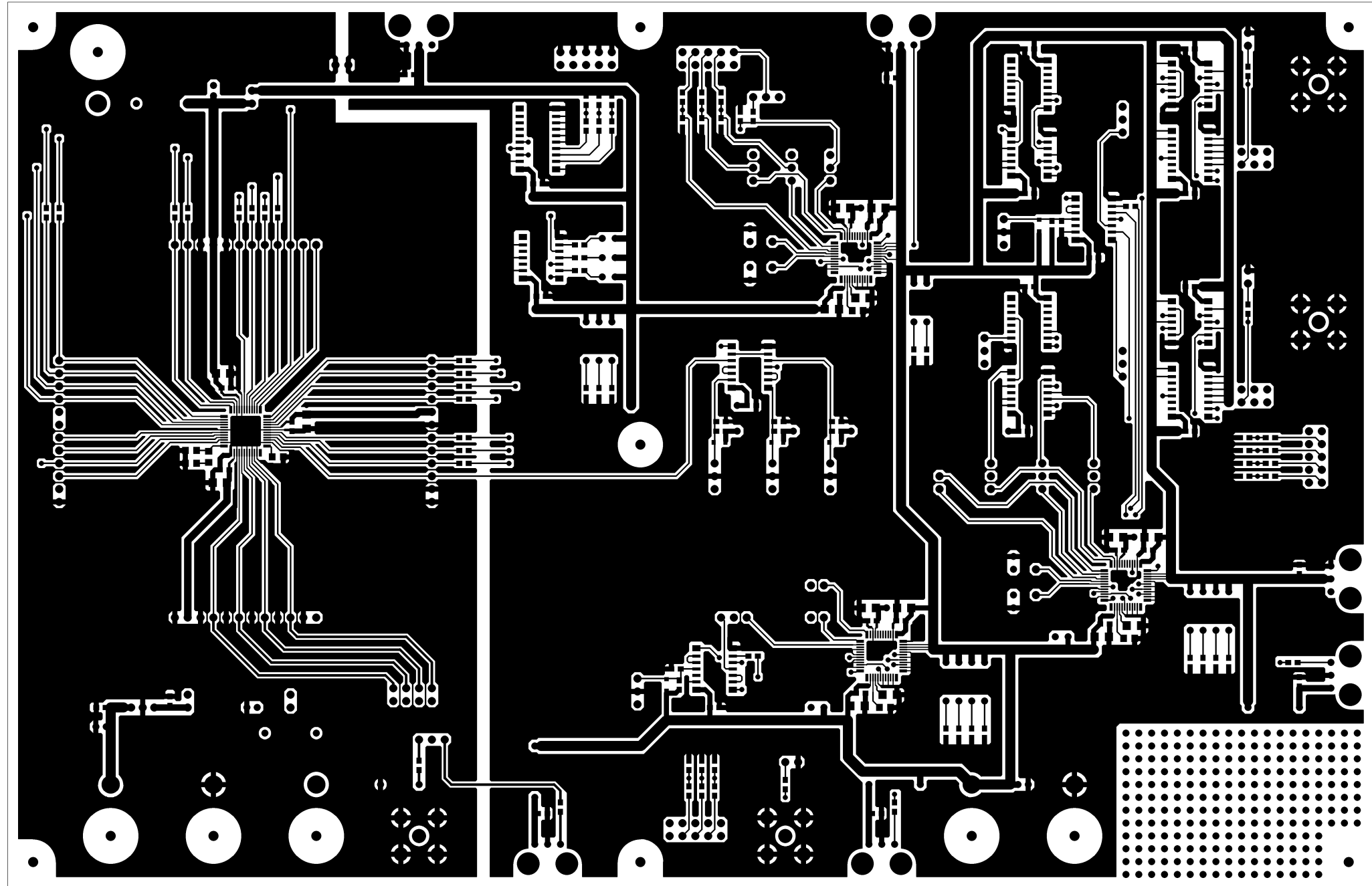


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Size	Document Number	Power Supply			Rev
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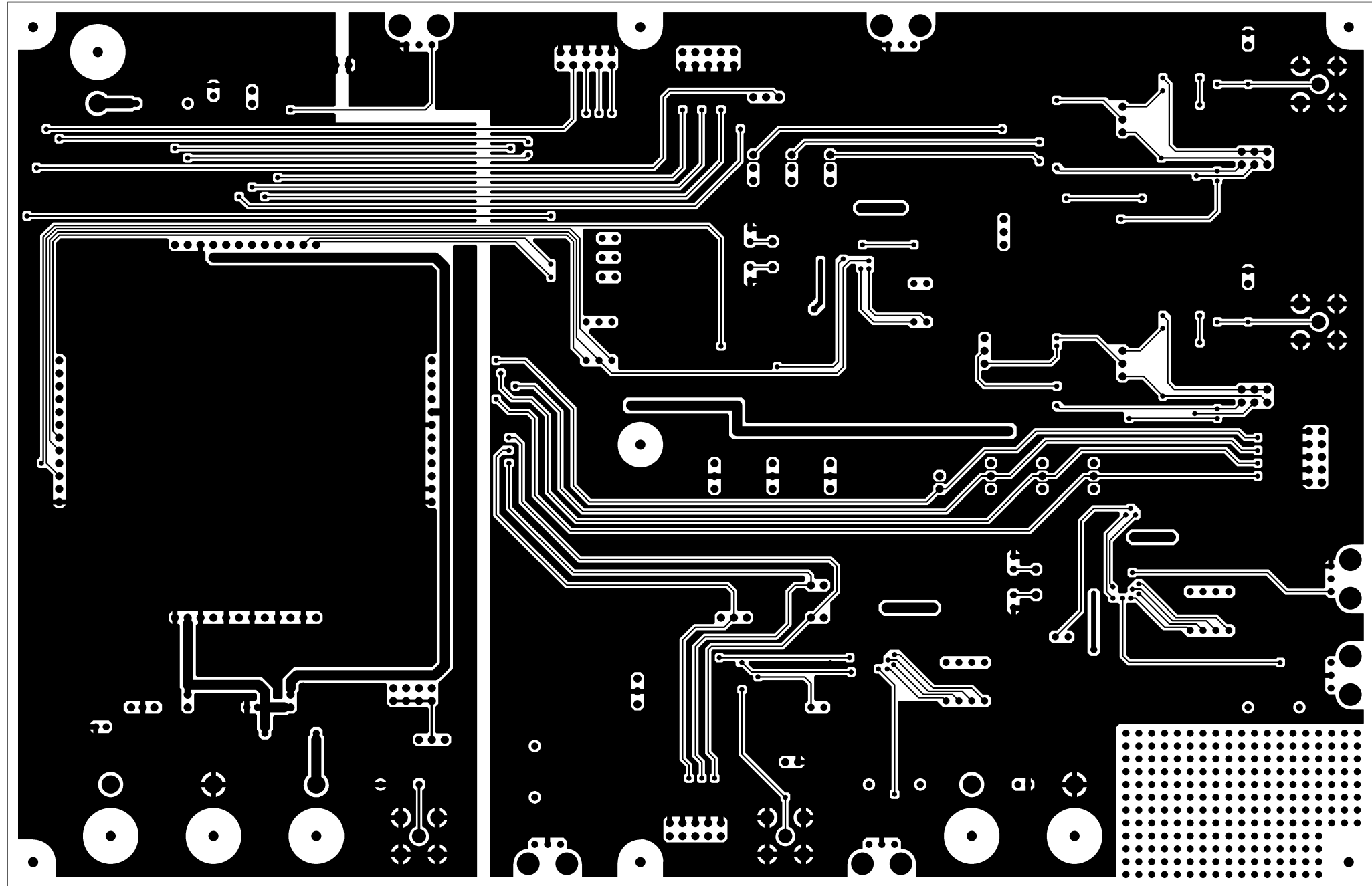


AKD4122 Rev.A
Evaluation Board

AKD4122 Rev.A L1 SR SILK



AKD4122 Rev.A L1



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