AKD4352

Evaluation board Rev.A for AK4352

General Description

AKD4352 is an evaluation board for the 18bit audio D/A converter AK4352. The AKD4352 has the interface with AKM's wave generator using ROM data and with AKM's ADC evaluation boards (AKD5392, AKD5391, AKD5352, and AKD5351). Therefore, it is easy to evaluate the AK4352. The AKD4352 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4352 --- Evaluation board of AK4352

Function

- ☐ On-board 2nd order LPF
- ☐ On-board clock generator
- ☐ Compatible with the following 3 types of interface
  1) Direct interface with AKM's A/D converter, and direct interface with ROM board.
  2) Direct interface with signal generator(AKD43XX)
  3) On-board CS8412 as DIR which accepts optical input
- ☐ A BNC connector for an external clock input

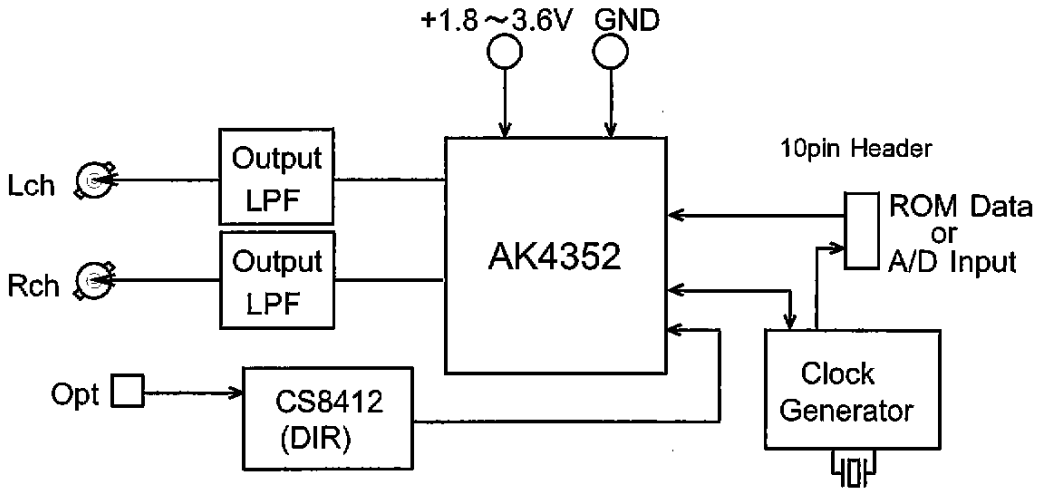
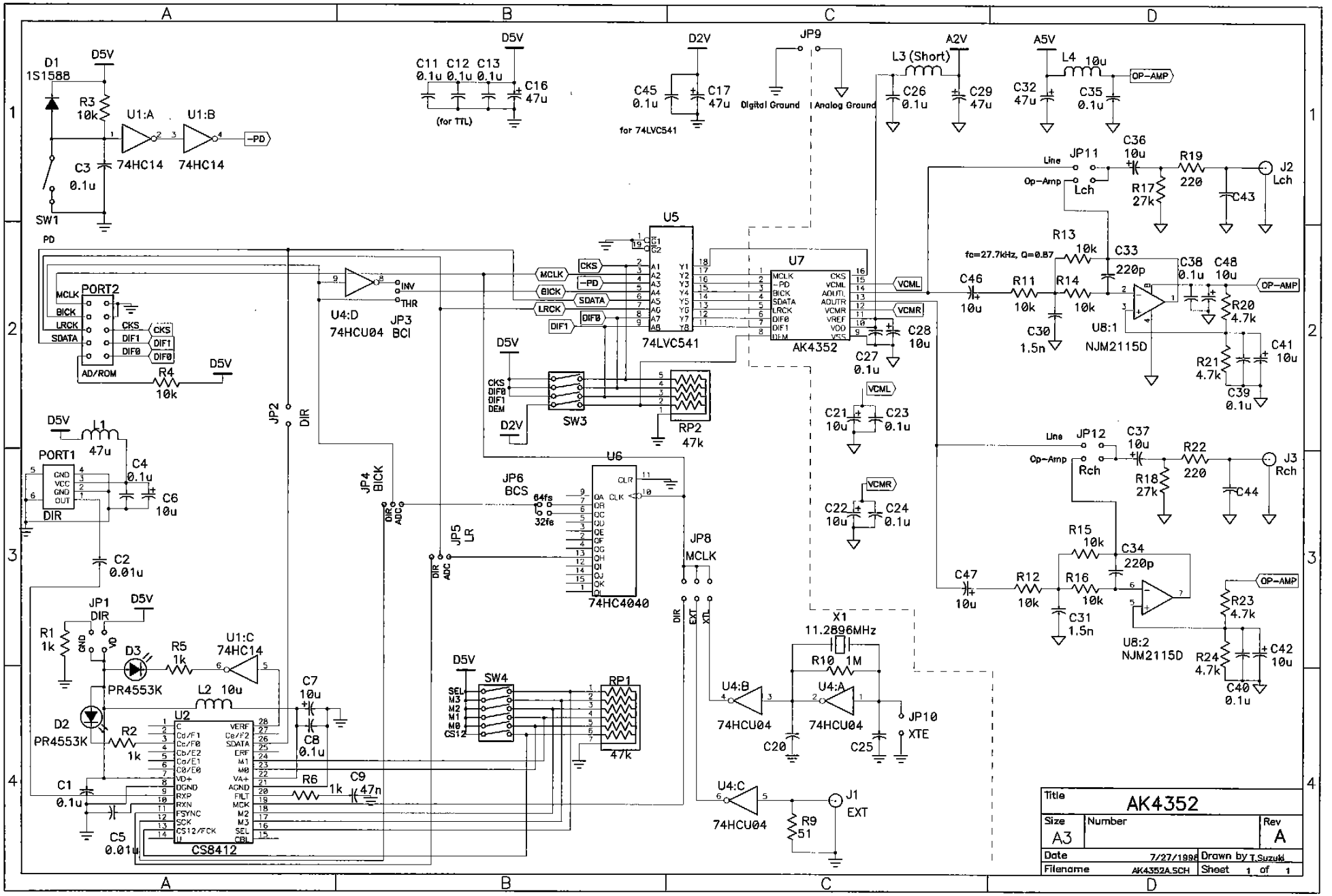


Figure 1. AKD4352 Block Diagram


Title
AK4352
Size
A3
Number
Rev
A
Date
7/27/1998
Drawn by T.Suzuki
Filename
AK4352A.SCH
Sheet 1 of 1
D1
1S1588
D5V
R3
10k
U1:A
U1:B
74HC14
74HC14
C3
0.1u
SW1
PD
C11 C12 C13
0.1u 0.1u 0.1u
C16
47u
(for TTL)
D2V
C45
0.1u
C17
47u
for 74LVC541
JP9
Digital Ground
Analog Ground
A2V
L3 (Short)
C26
0.1u
C29
47u
A5V
L4 10u
C32
47u
C35
0.1u
OP-AMP
C36
10u
JP11
Line
Op-Amp
Lch
R19
220
J2
Lch
R17
27k
C43
R13
10k
fc=27.7kHz, Q=0.87
C33
220p
C38
0.1u
C48
10u
C46
10u
R11
10k
R14
10k
C30
1.5n
U8:1
NJM2115D
R20
4.7k
R21
4.7k
C41
10u
C39
0.1u
U5
74LVC541
U7
AK4352
VCML
VCMR
C28
10u
C27
0.1u
C21
10u
C23
0.1u
C22
10u
C24
0.1u
PORT2
AD/ROM
R4
10k
U4:D
74HCU04
JP3
BCI
JP2
DIR
SW3
RP2
47k
L1
47u
PORT1
DIR
C4
0.1u
C6
10u
C2
0.01u
JP4
BICK
JP5
LR
JP6
BCS
64fs
32fs
U6
74HC4040
JP8
MCLK
JP12
Line
Op-Amp
Rch
C37
10u
R22
220
J3
Rch
R18
27k
C44
R15
10k
C34
220p
C47
10u
R12
10k
R16
10k
C31
1.5n
U8:2
NJM2115D
R23
4.7k
R24
4.7k
C42
10u
C40
0.1u
JP1
DIR
R1
1k
D3
PR4553K
R5
1k
U1:C
74HC14
L2 10u
C7
10u
C8
0.1u
D2
PR4553K
R2
1k
U2
CS8412
C1
0.1u
C5
0.01u
R6
1k
C9
47n
SW4
RP1
47k
X1
11.2896MHz
R10 1M
U4:B
U4:A
74HCU04
74HCU04
JP10
XTE
C20
C25
U4:C
74HCU04
R9
51
J1
EXT

■ Analog Output

Analog signals are output through BNC connectors on the board and the output level are typically 1.1Vpp (@ VREF=2.0V). When the attenuation of the out-band noise is needed, the 2nd order LPF(fc=27.7kHz, Q=0.87) with inverted-amp(Gain:0dB) on the board should be used(JP11,12=Op-Amp).

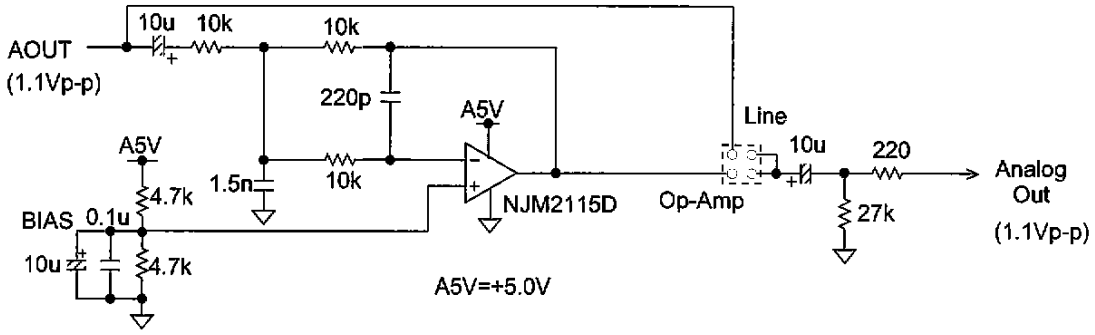


Fig.2 on-board analog filter

■ Grounding and Power Supply Decoupling

Decoupling capacitors should be connected to AK4352 as near as possible. Especially the capacitor between VDD and VSS should be connected nearest.

■ Operation Sequence

① Set up the power supply lines.
D5V=A5V= 5.0V,
D2V=A2V= 2.0V,
AGND=DGND=0V.
Each supply line should be distributed from the power supply unit.

② Set up the evaluation modes and jumper pins.
(See the next item)

③ Set up the DIP-SW.
(See the next item)

④ Power on.

⑤ Reset the AK4352 by SW1.

(The AK4352 is reset by SW1: PD = "L" during operation.)

■ Set-up of the evaluation modes and jumper pins

1. Evaluation modes

Applicable evaluation modes

① DIR (Optical Link) (default)
② Using ROM data(AK43XX)
③ Using AKM's evaluation board for ADC
④ Feeding all signals from external

① DIR (Optical Link)

PORT1 is used. All clock are supplied from CS8412 (DIR). DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT2.

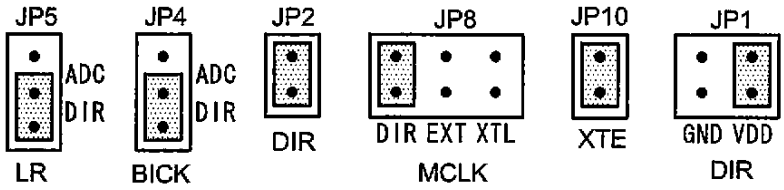


Fig.3 DIR

② Using ROM data(AK43XX)

Connect the AK43XX with PORT2.
AKD4352 sends MCLK to AKD43XX, and receives LRCK,BICK and SDATA.
※ In case of using external master clock through a BNC connector, set JP8(MCLK) EXT and short JP10(XTE).

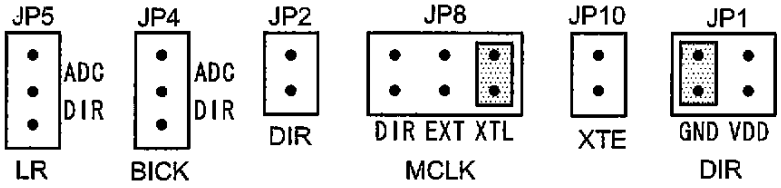


Fig.4 ROM data

③ Using AKM's evaluation board for ADC

To evaluate AK4352 with analog input, The AKM's evaluation board for ADC can be used.
MCLK, BICK and LRCK are supplied from clock generator on the AKD4352, and analog signal is A/D converted and send to AKD4352 through PORT2.
※ In case of using external master clock through a BNC connector, set JP8(MCLK) EXT and short JP10(XTE).

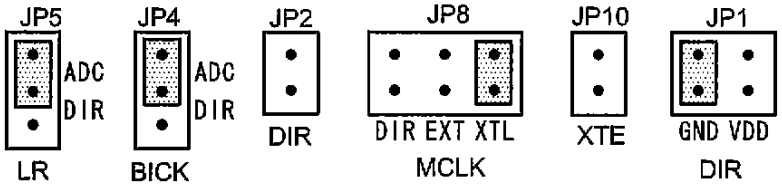


Fig.5 A/D data

④ Feeding all signals from external

Under the following set-up, all external signals could be fed through PORT2.

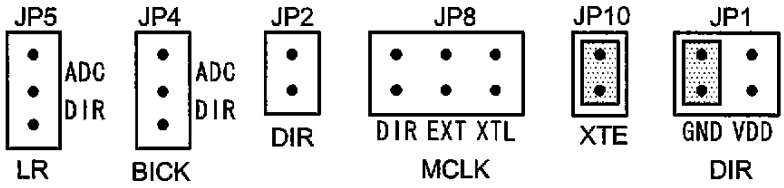


Fig.6 External signal

2. BICK frequency (JP6)

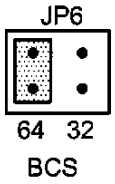


Fig.7

When BICK is fed from 74HC4040 on board, its frequency is selected with JP6.

64 : BICK = 64fs (Fig.7)

32 : BICK = 32fs

3. MCLK frequency (SW3-1)

Following the MCLK frequency, set up the SW3-1(CKS)

MCLK = 256fs : CKS = OFF

MCLK = 384fs : CKS = ON

※ In case of mode ① and ③, set SW3-1 OFF(256fs).

4. De-emphasis filter (SW3-4)

Set the De-emphasis filter of AK4352 with SW3-4(DEM).

5. Serial data format (SW3-2,3)

Set serial data format of AK4352 with SW3-2,3(DIF0,1).

※ In case of mode ①, adjust the data format between DIR and AK4352 with SW4.

Table 1 Serial data format of AK4352

DIF1	DIF0	Mode	BICK
0	0	16bit LSB justified	≧ 32fs
0	1	18bit LSB justified	≧ 36fs
1	0	18bit MSB justified	≧ 36fs
1	1	I^2S (IIS)	≧ 32fs or ≧ 36fs

6. CS8412(DIR) Set-up (SW4, JP3)

Set the data format of CS8412(DIR) with SW4 and JP3. This format must be fitted to AK4352, which is set with DIF0 and DIF1.
(For more detailed configurations, please refer to the CS8412 data-sheet.)

Table 2-1 (SW4)

No.	pin name	ON	OFF	
1	SEL	normally ON		※ 1
2	M 3	see Table 2-2		
3	M 2			
4	M 1			
5	M 0			
6	CS12	Rch	Lch	※ 2

Table 2-2 CS8412 data format ※ 3

M 3	M 2	M 1	M 0	mode	JP3
0	0	0	0	0: 18bit MSB justified	INV
0	0	1	0	2: I^2S	THR
0	1	0	1	5: 16bit LSB justified	THR
0	1	1	0	6: 18bit LSB justified	THR

1:ON, 0:OFF

※ 1 When "ON", LED shows the pre-emphasis status.
(LED turns on when the data is pre-emphasized.)
※ 2 Select the channel whose set up of CS8412.
※ 3 JP3 fits the BICK phase of CS8412 to AK4352s.

■ Switch list

[SW1] Reset switch for AK4352. The reset state is "L".
[SW3] Set-up switch of CKS,DEM,DIF1,DIF0.
[SW4] Set-up switch of CS8412.

[D1] "Pre-emphasis"-monitor. LED turns on when the data is pre-emphasized.
[D2] "VERF pin"-monitor for the CS8412.
LED turns on when some error has occurred to CS8412.

AK4352 Measurement Results

■ No.1 (Audio Precision, System Two)

[Measurement condition]

- Measurement unit: Audio Precision, System Two (RMS mode)
- MCLK: 256fs
- BICK: 64fs
- Bit: 18bit
- fs: 44.148kHz
- Power Supply: D5V=5.0V, A2V=1.8/2.0/3.3/3.6V
- Interface: DIR
- temp: Room temp

1. D/A Output

- fs=44.1kHz

Parameter	Input signal	Measurement Filter	Results				
			1.8V	2.0V	3.0V	3.3V	3.6V
S/(N+D)	1kHz, 0dB	20kLPF	80.8dB	82.7dB	89.0dB	90.4dB	91.2dB
		22kLPF, A-weight	79.9dB	82.0dB	89.2dB	90.8dB	91.6dB
Dynamic Range	1kHz, -60dB	20kLPF	89.7dB	90.4dB	93.1dB	93.8dB	94.1dB
		22kLPF, A-weight	92.4dB	93.2dB	95.8dB	96.3dB	96.8dB
S/N	1kHz, 0dB/"0"data IN	20kLPF	90.2dB	91.2dB	94.8dB	95.5dB	96.2dB
		22kLPF, A-weight	93.2dB	94.1dB	97.5dB	98.3dB	99.0dB

2. D/A Output

・A2V=2.0V

Parameter	Input signal	Measurement Filter	Results		
			32kHz	44.1kHz	48kHz
S/(N+D)	1kHz, 0dB	20kLPF	83.0dB	82.3dB	81.3dB
		22kLPF	65.0dB	82.0dB	81.1dB
		30kLPF	53.8dB	76.8dB	78.9dB
		80kLPF	49.5dB	63.3dB	65.8dB
		500kLPF	48.3dB	57.3dB	58.8dB
		A-weight	66.1dB	80.6dB	80.1dB
		22kLPF, A-weight	78.7dB	81.4dB	80.4dB
Dynamic Range	1kHz, -60dB	20kLPF	90.5dB	90.8dB	90.8dB
		22kLPF	88.8dB	90.3dB	90.4dB
		30kLPF	79.1dB	86.1dB	87.2dB
		80kLPF	61.9dB	69.3dB	71.3dB
		500kLPF	54.6dB	59.8dB	61.3dB
		A-weight	87.1dB	91.7dB	92.4dB
		22kLPF, A-weight	93.3dB	93.6dB	93.6dB
S/N	1kHz, 0dB/"0"data IN	20kLPF	90.7dB	90.8dB	90.9dB
		22kLPF	88.9dB	90.4dB	90.5dB
		30kLPF	79.3dB	85.7dB	87.4dB
		80kLPF	62.2dB	68.7dB	71.5dB
		500kLPF	55.0dB	59.4dB	61.3dB
		A-weight	87.3dB	91.7dB	92.7dB
		22kLPF, A-weight	93.5dB	93.8dB	93.8dB

■ No.2 (Shibasoku AD725C)

[Measurement condition]

- Measurement unit: Shibasoku AD725C (RMS/AVG mode)
- MCLK: 256fs
- BICK: 64fs
- Bit: 18bit
- fs: 44.1kHz
- Power Supply: D5V=5.0V, A2V=2.0V
- Interface: DIR
- temp : Room temp

1. D/A Output

Parameter	Input signal	Measurement Filter	Results	
			RMS	AVG
S/(N+D)	1kHz, 0dB	20kLPF	83.3dB	83.5dB
Dynamic Range	1kHz, -10dB	20kLPF, A-weight	93.6dB	94.6dB
S/N	1kHz, 0dB/"0" data IN	20kLPF, A-weight	93.2dB	94.3dB

■ No.3 (ROHDE & SCHWARZ UPD)

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ UPD (RMS mode)
- MCLK: 256fs
- BICK: 64fs
- Bit: 18bit
- fs: 44.1kHz
- Power Supply: D5V=5.0V, A2V=2.0V
- Interface: DIR
- temp : Room temp

1. D/A Output

Parameter	Input signal	Measurement Filter	Results
S/(N+D)	1kHz, 0dB	20kLPF	82.3dB
Dynamic Range	1kHz, -60dB	20kLPF, A-weight	94.2dB
S/N	1kHz, 0dB/"0" data IN	20kLPF, A-weight	94.4dB

■ No.4 (Graph)

・[Common Measurement condition]

- ・Measurement unit: Audio Precision, System Two (RMS mode)
- ・MCLK: 256fs
- ・BICK: 64fs
- ・fs: 44.1kHz
- ・Power Supply: D5V=5.0V, A2V=2.0V
- ・Interface: DIR
- ・temp: Room temp

① THD+N vs. Input Level (Fig1)

- ・Measuremnet Filter: 20kHzLPF
- ・fin: 1kHz

② THD+N vs. Input Frequency (Fig2)

- ・Measurement Filter: 20kHzLPF
- ・Level: 0dB (Full Scale)

③ Linearity (Fig3)

- ・fin: 1kHz

④ Frequency Response(Fig4)

- ・Reference: 1kHz, 0dBr

⑤ Crosstalk (Fig5)

⑥ FFT PLOT

- ・Point: 16384
- ・Average: 16
- ・Digital input data: 18bit
- ・fin: 1kHz
- ・Level: Out-of-band Noise (input "0" data, Fig6),
  0dB (Full Scale, Fig7), -20dB (Fig8), -60dB (Fig9),
  Noise floor (input "0" data, Fig10)

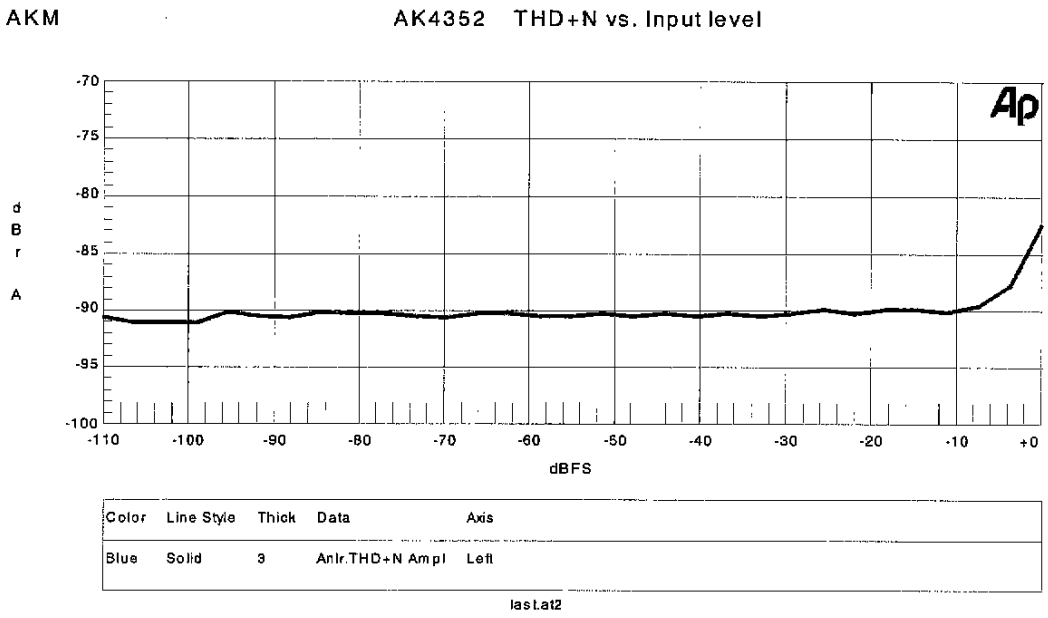


Fig1 : THD+N vs. Input level

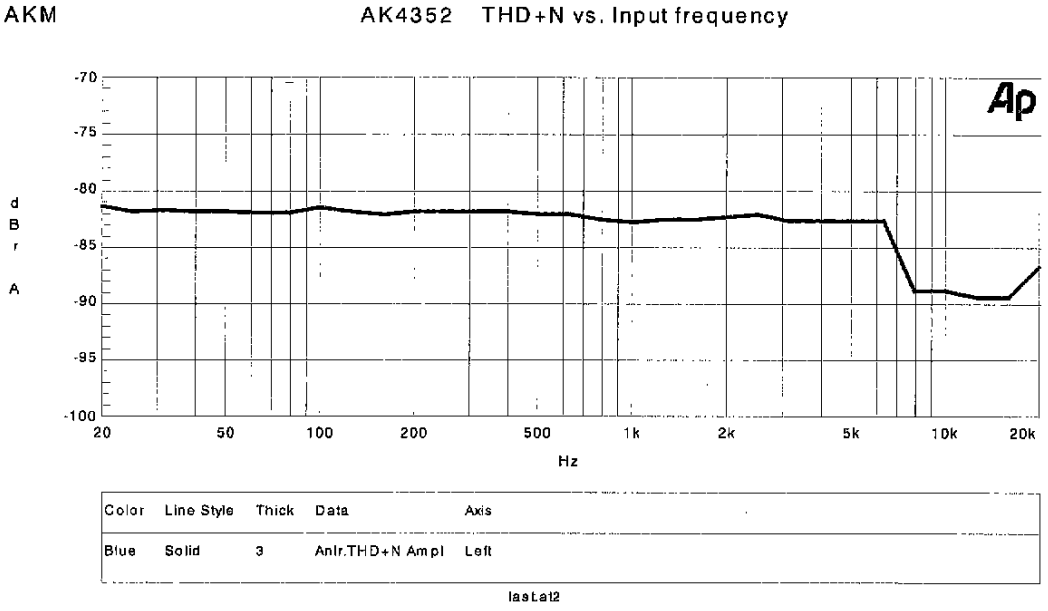


Fig2 : THD+N vs. Input Frequency

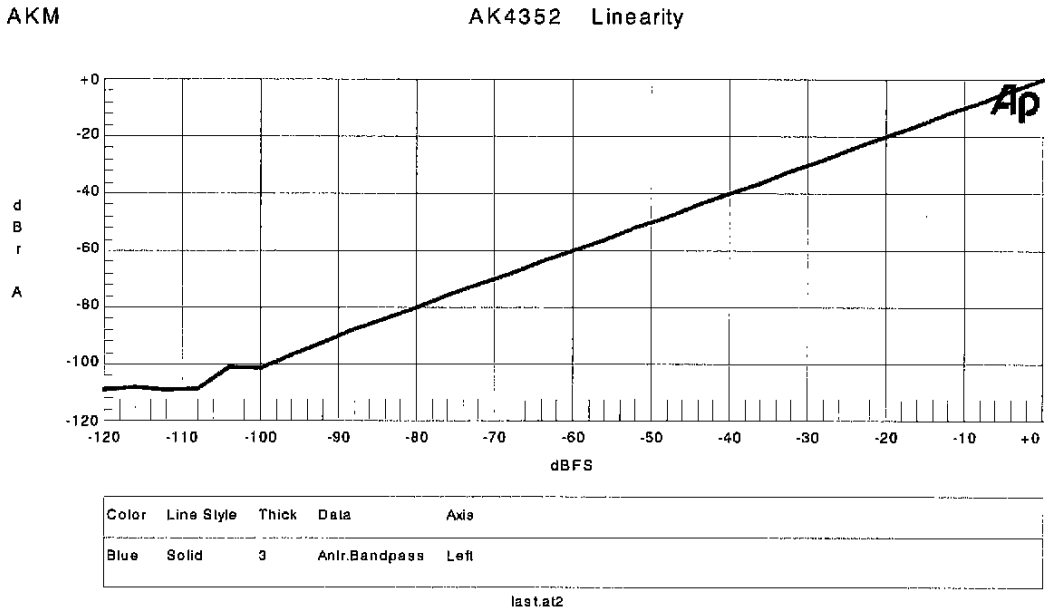


Fig3 : Linearity

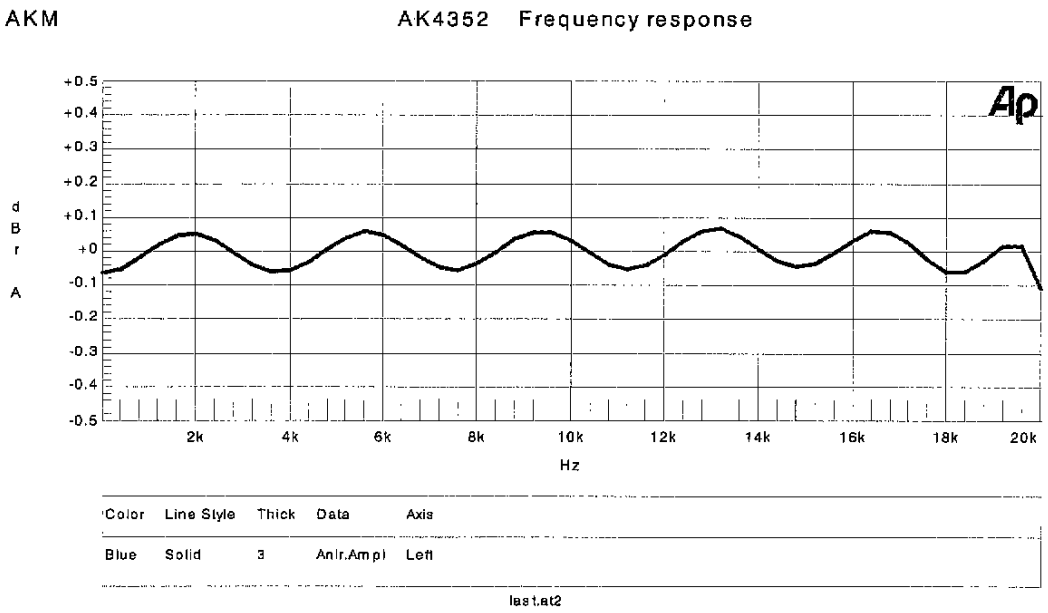


Fig4 : Frequency response

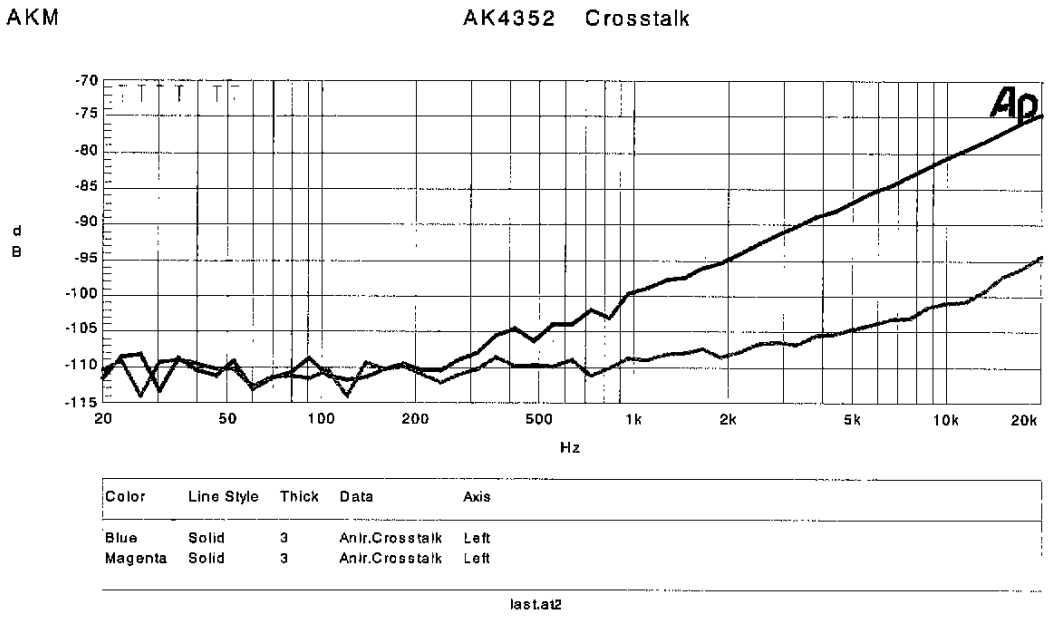


Fig5 : Crosstalk

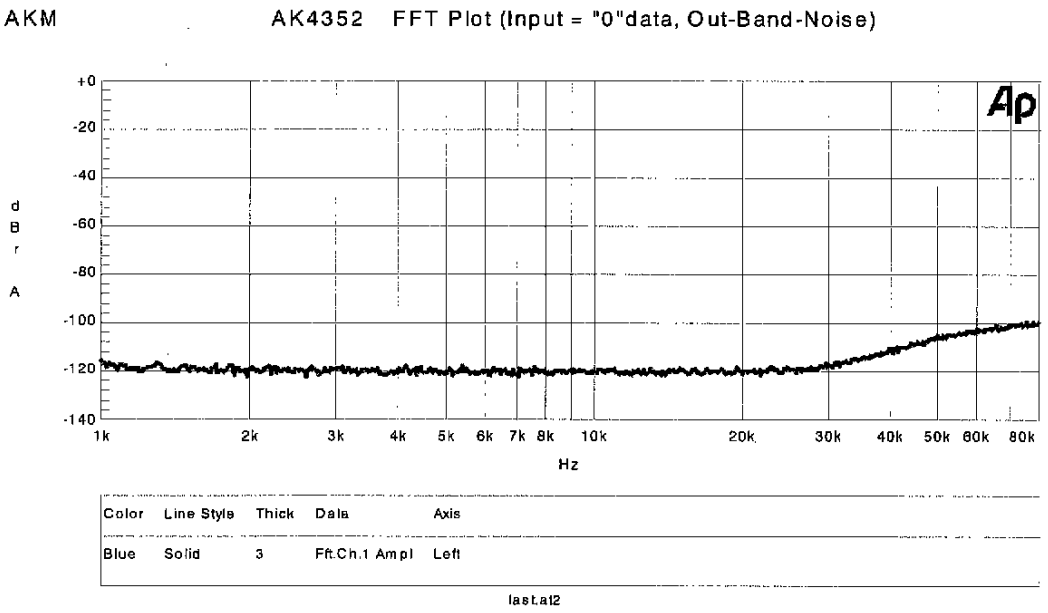


Fig6 : FFT Plot(Out-of-band Noise, Input="0" data)

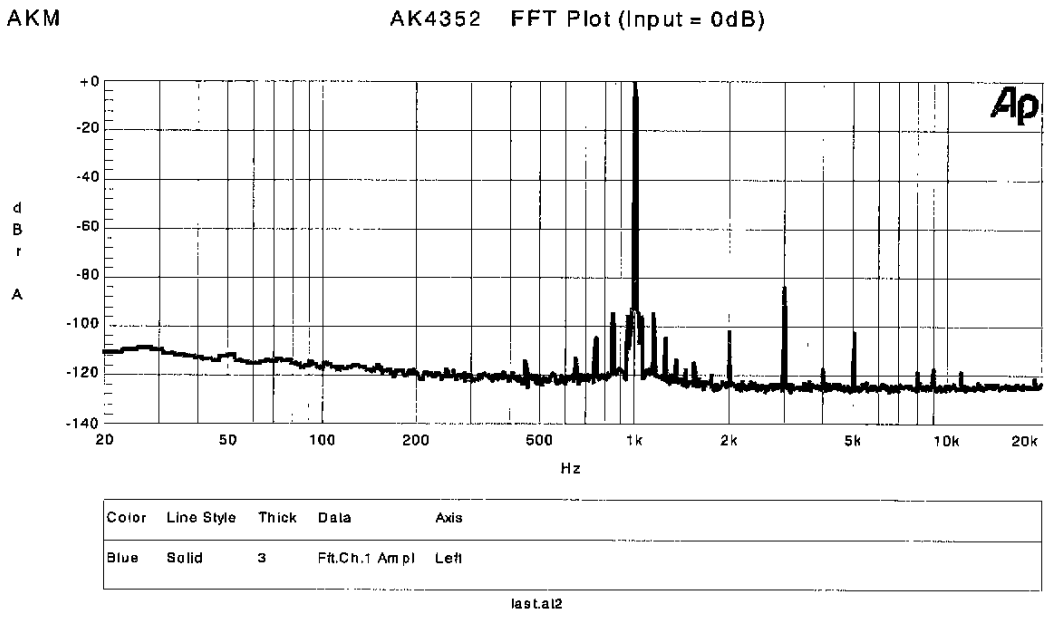


Fig7 : FFT Plot (Input=0dB)

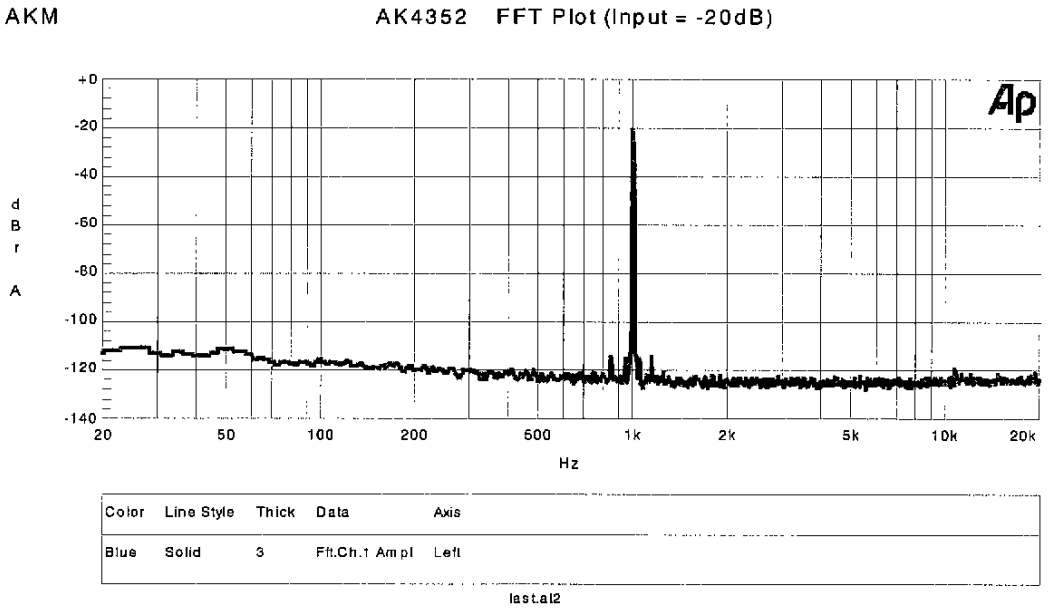


Fig8 : FFT Plot (Input=-20dB)

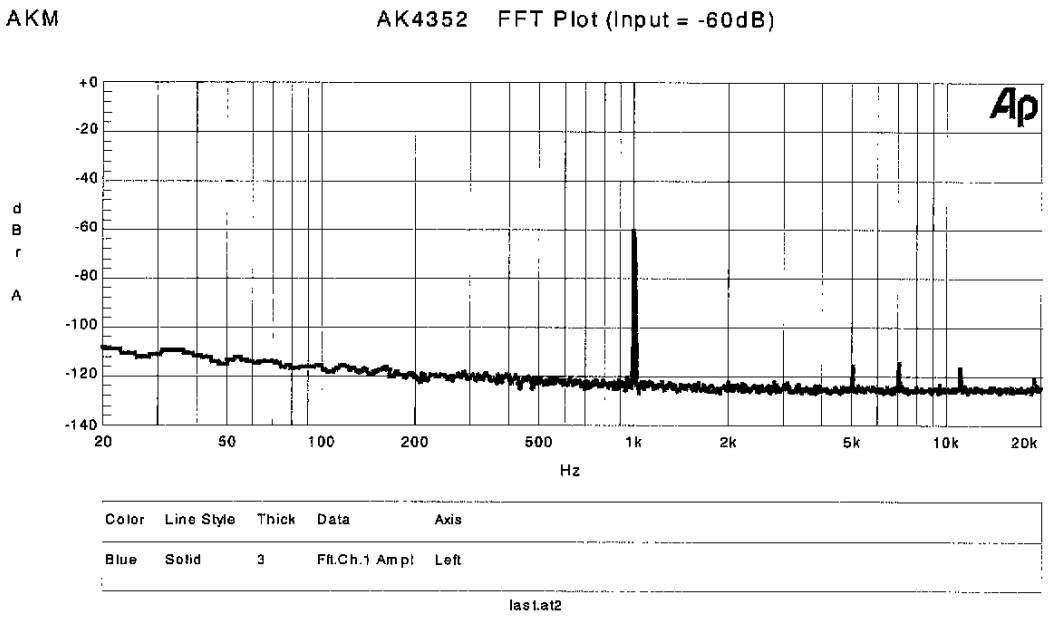


Fig9 : FFT Plot (Input=-60dB)

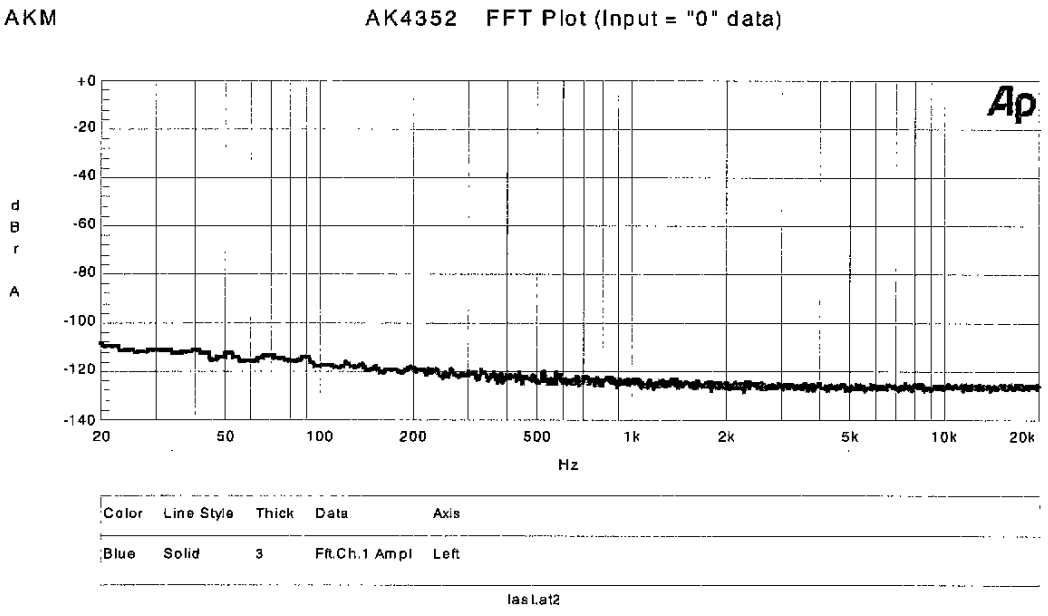
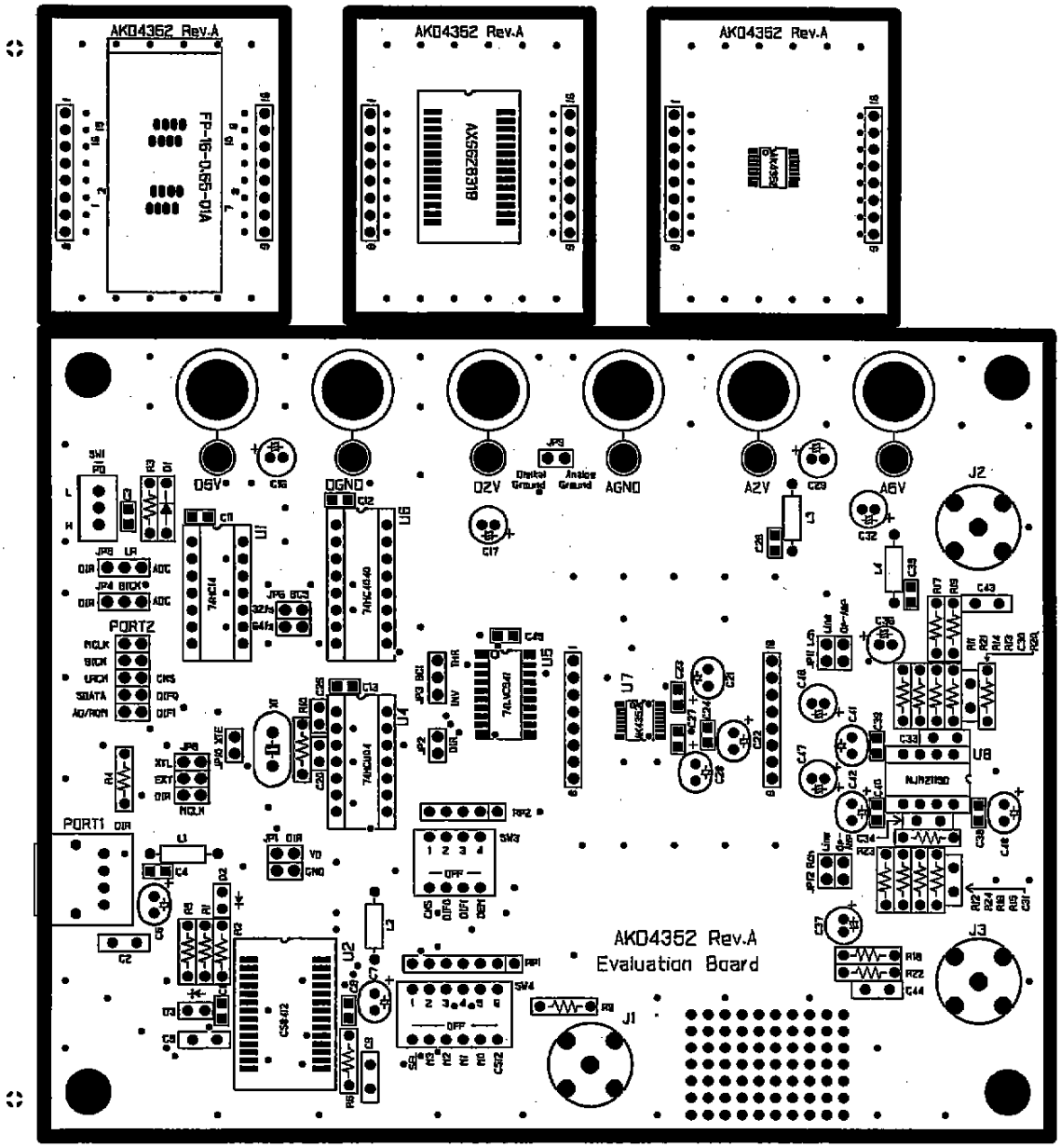
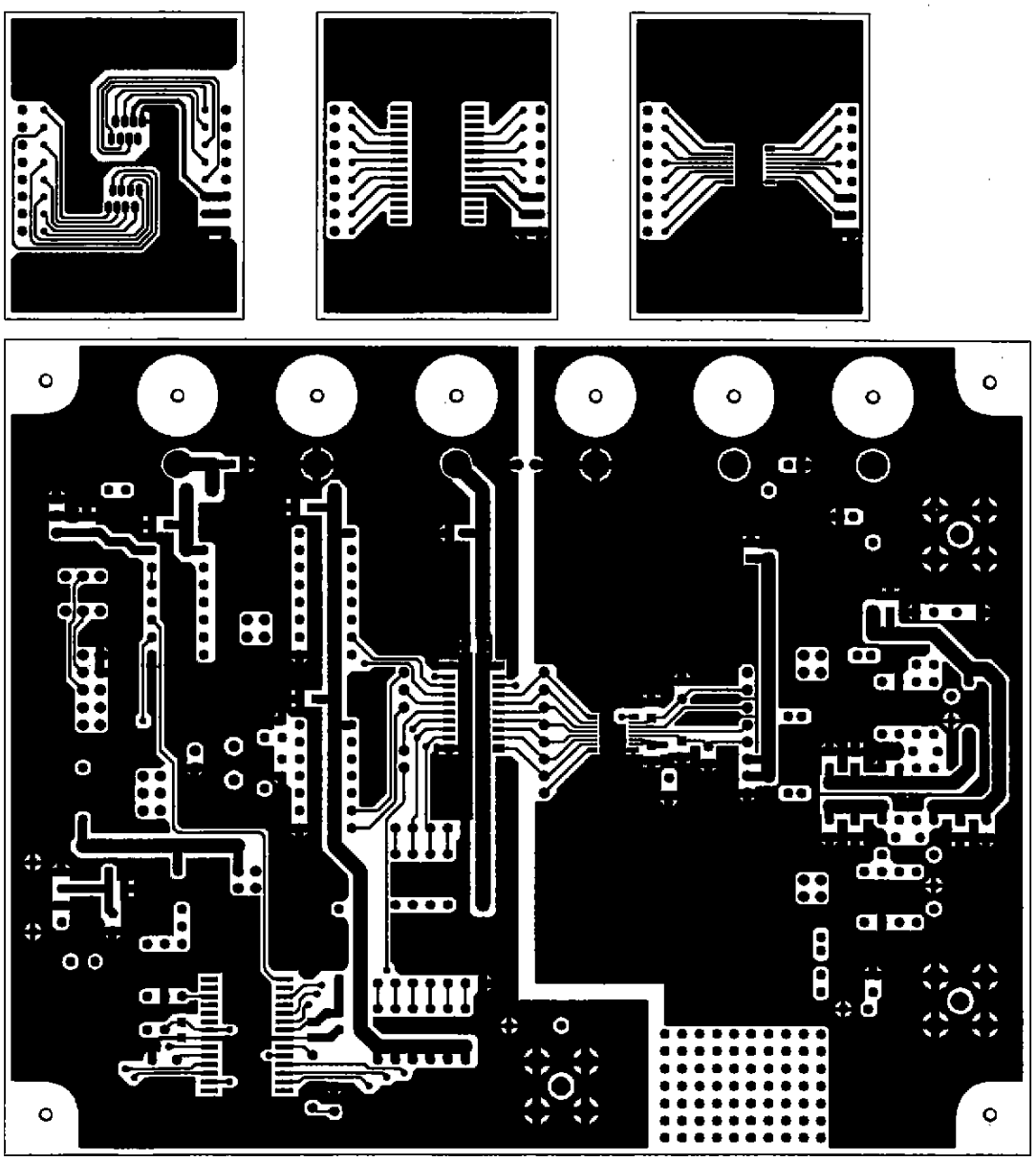


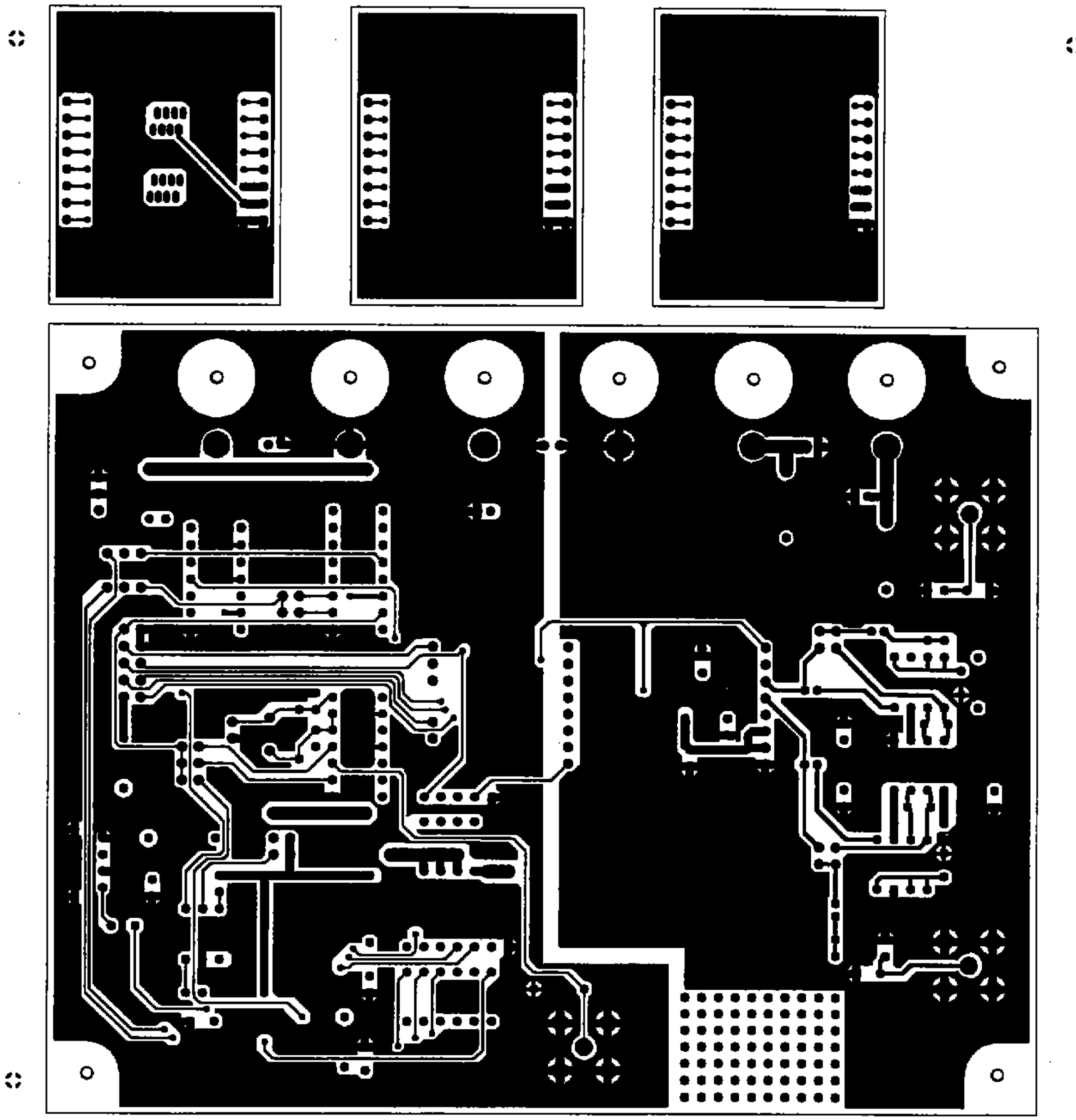
Fig10 : FFT Plot (Input="0" data)



L1 レイアウト AKD4352



L1 パターン AKD4352



AKD4352 パターン L2