AsahiKASEI
ASAHI KASEI EMD

AKD4373-B

AK4373 Evaluation Board Rev.2

GENERAL DESCRIPTION

The AKD4373 is an evaluation board for 24bit DAC with Headphone Amplifier and a monaural speaker driver. The ADK4373 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4373-B --- Evaluation board for AK4373
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- **Compatible with 2 types of interface**
  - **Audio serial I/F input (port2)**
  - **On-board AK4116 as DIR which accepts optical input(Port1)**
- **10pin header for serial control interface**
- **Mini-jack for external Stereo HP and a monaural speaker**

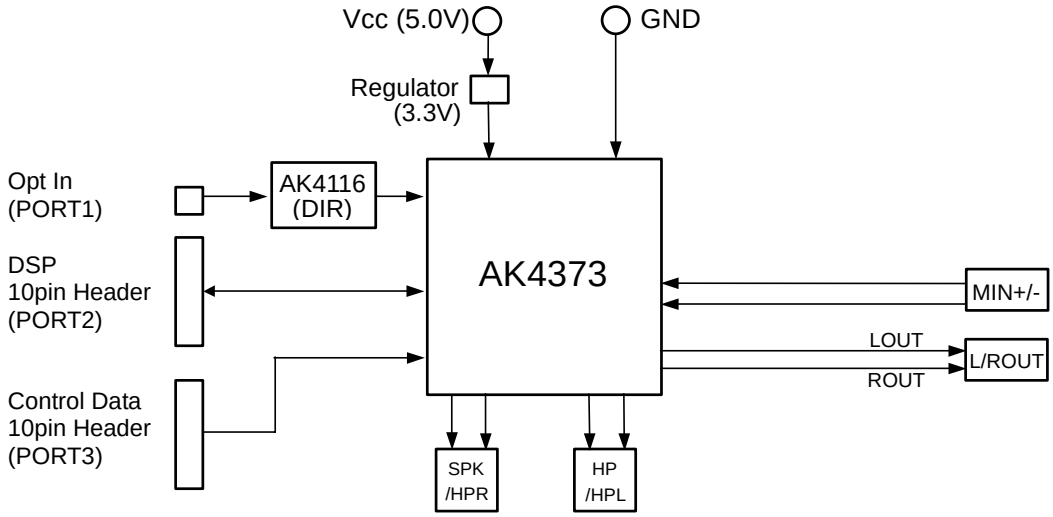


Figure 1. AKD4373 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Board Outline Chart

■ Outline Chart

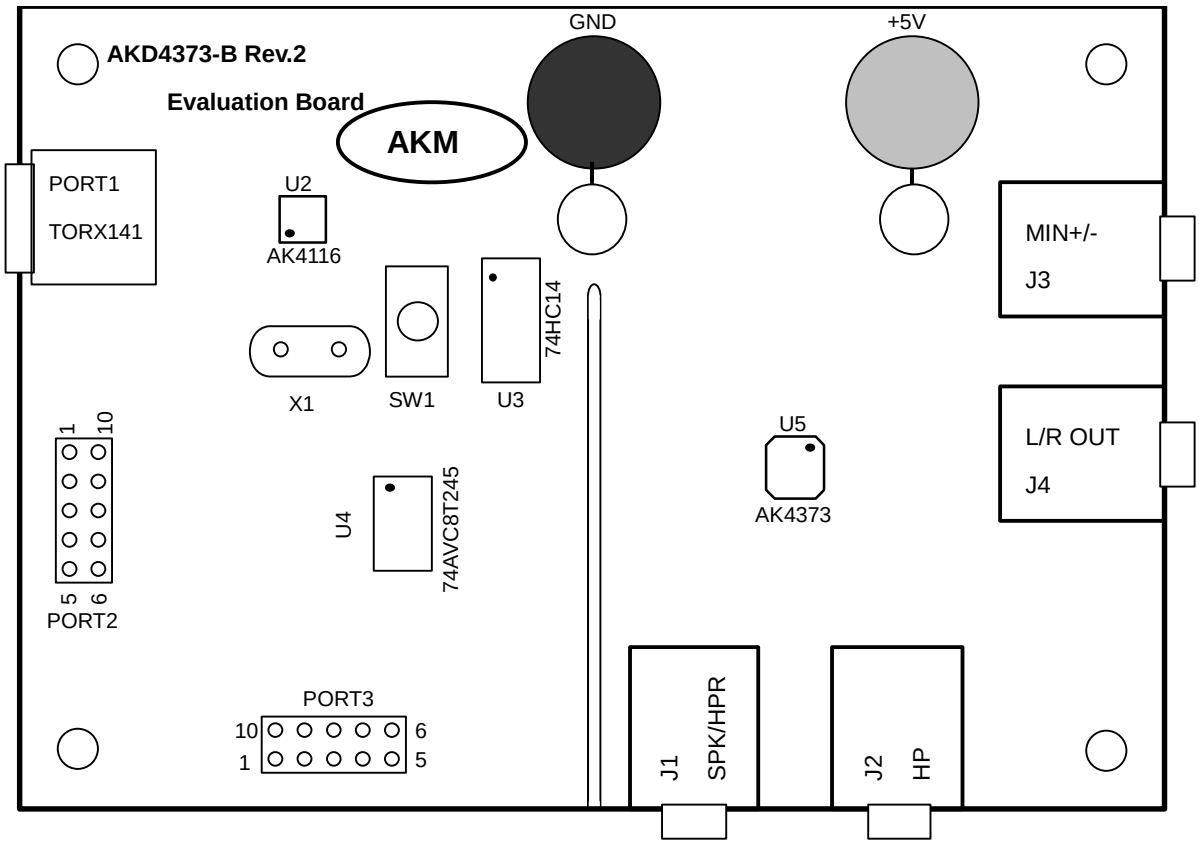


Figure 2. AKD4373-B Outline Chart

■ Comment

(1) J1, J2, J3, J4 (MINI-JACK)
J1 (SPK/HPR-JACK): An analog signal output Jack. The signal is output to SPK or HPR pin.
J2 (HP-JACK): An analog signal output Jack. The signal is output to HP or HPL pin.
J3 (MIN-JACK): An analog signal input Jack. The signal is input to MIN+/- pin.
J4 (L/ROUT-JACK): An analog signal output Jack. The signal is output to L/ROUT pin.

(2) +5V, GND
+5V-JACK: The power supply connector.
GND-JACK: The ground connector.

(3) PORT1 (Optical Connecter)
PORT1 (Input): Optical digital signal (SPDIF, Fs: 32~48kHz) is input to the AK4116.

(4) PORT2, PORT3 (10 pin header)
PORT2 (10 pin header): The clock and data can be input and output with this connector.
PORT3 (10 pin header): Control port. Connect the bundled cable into this port.

■ Operation sequence

1) Set up the power supply lines.

Name	Color	Voltage	Comments	Attention
+5V	Red	+5V	Input to regulator	This jack is always needed. Power line
GND	Black	0V	For ground	This jack is always needed.

Table 1. Set up power supply lines

* Setting of Power Supply "DVDD": JP10 (DVDD-REG)
Open: It supplies "DVDD" from the outside to right pin.
Short: It supplies "DVDD" from the Regulator (3.3V) <default>.

Each supply line should be distributed from the power supply unit.
3.3V is supplied to AK4373 via the regulator.

2) Set up the evaluation mode, jumper pins. (See the followings.)

3) Power on.
The AK4373 and AK4116 should be resets once bringing SW1 (DAC/DIR-PDN) "L" upon power-up.

■ Evaluation mode

When evaluating the AK4373 using the PORT1 (AK4116), it is possible to use the initial setting of the audio interface format (24bit MSB justified). The AK4116 operates at fs of 32kHz or more. If the fs is slower than 32kHz, any other evaluation mode should be used.
When inputting the data from the PORT2, the AK4373's audio interface format should be set to correspond the input data's audio interface format. Refer to the AK4373's datasheet.

Applicable Evaluation Mode

(1) PLL Master Mode
(2) PLL Slave Mode
  (2-1) PLL Reference Clock: MCKI pin
  (2-2) PLL Reference Clock: BICK or LRCK pin
(3) External Slave Mode
  (3-1) Evaluation using DIR (Optical Link) of AK4116 <default>
  (3-2) Evaluation connecting AKD4373 with external DSP
(4) External Master Mode

(1) PLL Master Mode

PORT2 (DSP) is used. Nothing should be connected to PORT1 (DIR). BICK and LRCK are supplied from PORT2. It is possible to evaluate at various sampling frequencies using built-in the AK4373's PLL.

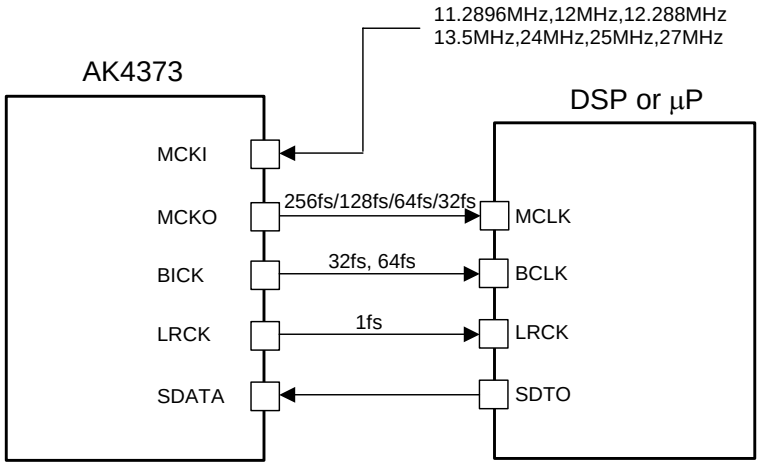
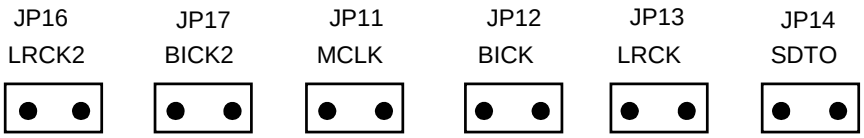


Figure 3. PLL Master Mode

The system clock should be connected to MCLK of PORT2. SDTI of PORT2 should be connected to SDTO of DSP. The JP16 (LRCK2) and JP17 (BICK2)'s right side should be connected to LRCK and BICK of DSP. In case of supplying MCKO to DSP, the test pin (MCKO) should be connected to MCLK of DSP.

Set up the jumper pins.



(2) PLL Slave Mode

(2-1) PLL Reference Clock: MCKI pin

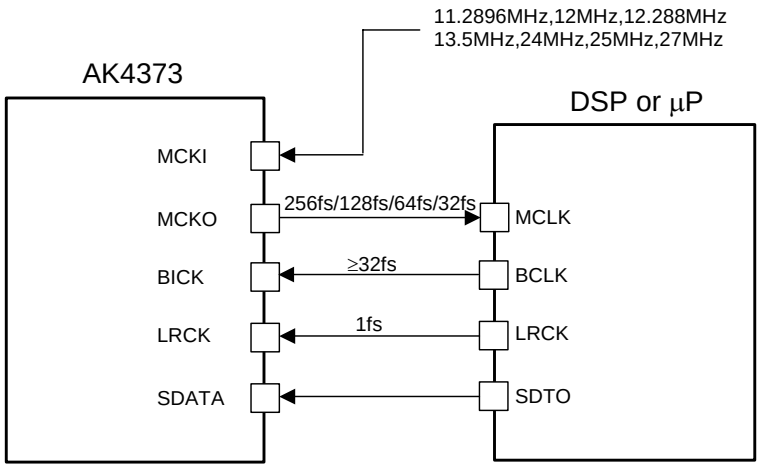
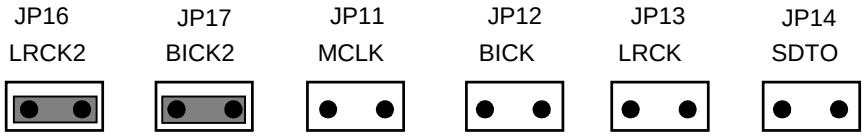


Figure 4. PLL Slave Mode (PLL Reference Clock: MCKI pin)

PORT2 (DSP) is used. Nothing should be connected to PORT1 (DIR).
MCKO is needed for a synchronous signal of BICK and LRCK.
MCLK, BICK, LRCK and SDATA are supplied from PORT2. The test pin (MCKO) should be connected to MCLK of DSP.

Set up the jumper pins.



(2-2) PLL Reference Clock: BICK or LRCK pin

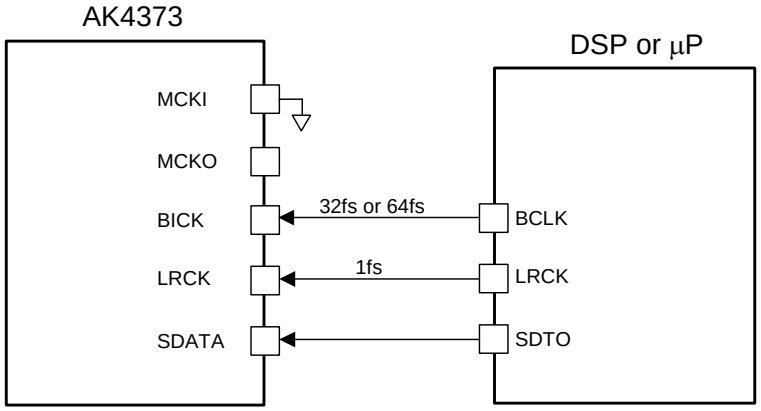
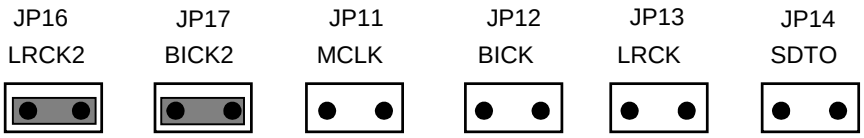


Figure 5. PLL Master Mode (PLL Reference Clock : BICK or LRCK pin)

PORT2 (DSP) is used. Nothing should be connected to PORT1 (DIR).
BICK, LRCK and SDATA are supplied from PORT2.

Set up the jumper pins.



(3) External Slave Mode

The AK4373's register should be set to EXT Slave Mode. MCKI frequency should be set to the same as the specification of DSP or DIR. About the AK4373's register definitions, refer to datasheet of the AK4373.

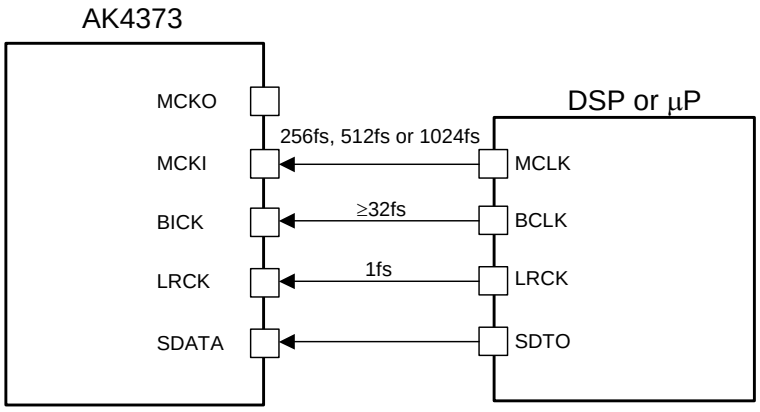
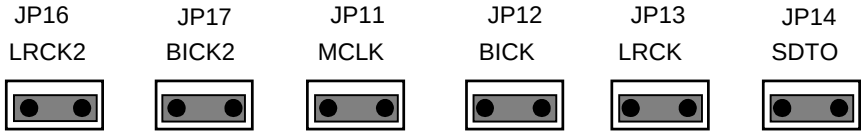


Figure 6. External Slave Mode

(3-1) Evaluation using DIR (Optical Link) of AK4116 <default>

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DSP).

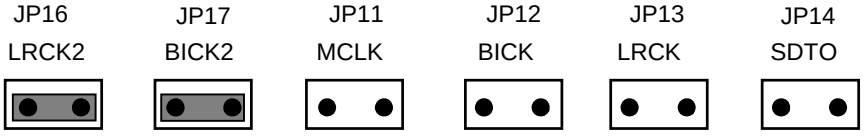
Set up the jumper pins.



(3-2) Evaluation connecting AKD4373 with external DSP

PORT2 (DSP) is used. Nothing should be connected to PORT1 (DIR).

Set up the jumper pins.



(4) External Master Mode

The AK4373's register should be set to EXT Master Mode. MCKI frequency should be set to the same as DSP's specification. About the AK4373's register definitions, refer to datasheet of the AK4373.

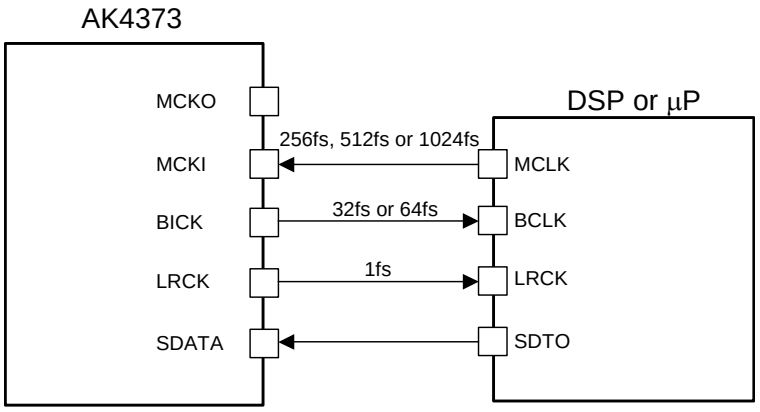
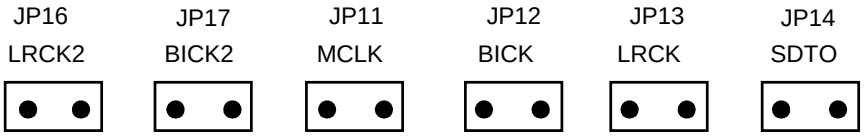


Figure 7. EXT Master Mode

PORT2 (DSP) is used. Nothing should be connected to PORT1 (DIR).
The system clock should be connected to MCLK of PORT2. SDTI of PORT2 should be connected to SDTO of DSP. The JP16 (LRCK2) and JP17 (BICK2)'s right side should be connected to LRCK and BICK of DSP.

Set up the jumper pins.



■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (DAC/DIR_PDN): Power down of AK4373 and AK4116. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4116. LED turns on when some error has occurred to AK4116.

■ Serial Control

The AK4373 can be controlled via the printer port (parallel port) of IBM-AT compatible PC.
Connect PORT3 (uP -IF) with PC by 10 wire flat cable packed with the AKD4373.

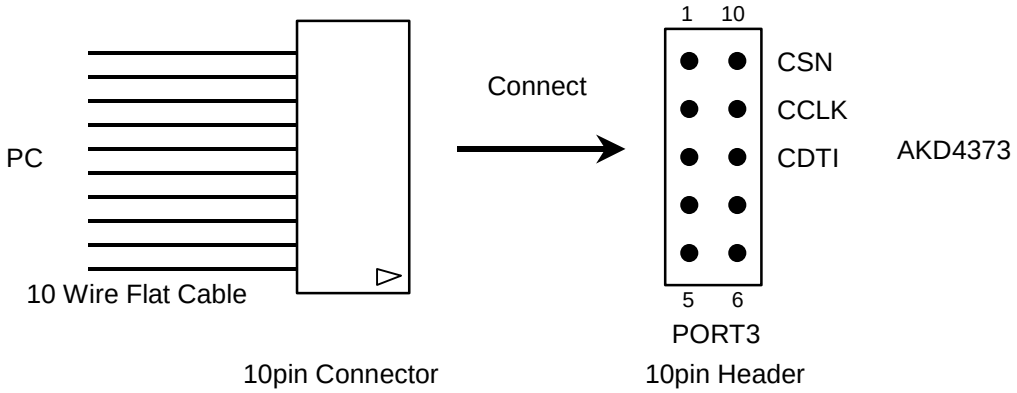
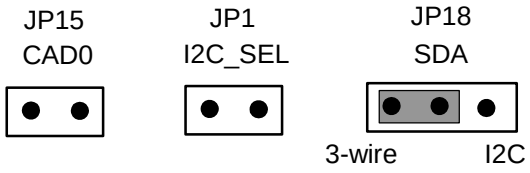


Figure 8. Connect of 10 wire flat cable

(1) 3-wire Serial Control Mode <Default>

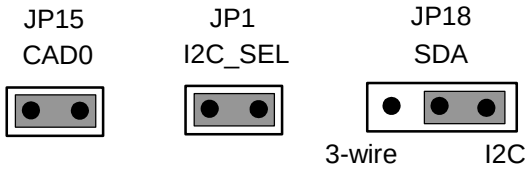
The jumper pins should be set to the followings.



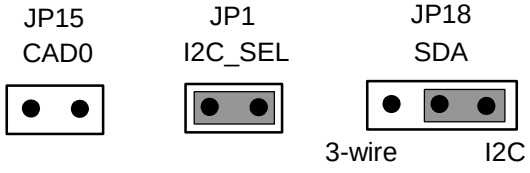
(2) I²C-bus Control Mode

The jumper pins should be set to the followings.

(2-1) In case of using CAD0=0 (device address bit).



(2-2) In case of using CAD0=1 (device address bit).



■ Input / Output circuit

(1) Input Circuit

MIN+/- Circuits

Figure 9. MIN+/- Input Circuits

(2)Output Circuit

1) LOUT/ROUT Output Circuit

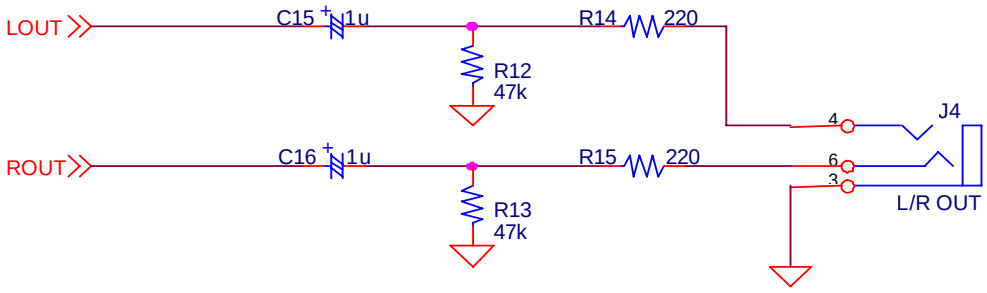


Figure 10. LOUT/ROUT Output Circuits

2) HP Output Circuits

a. Single-ended mode <default>

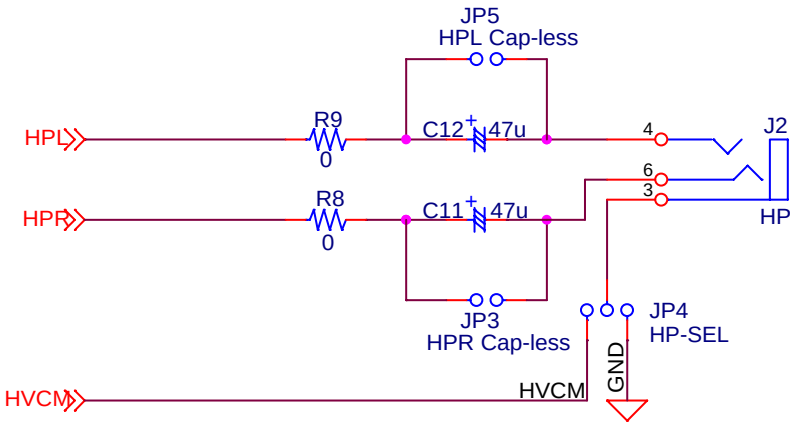
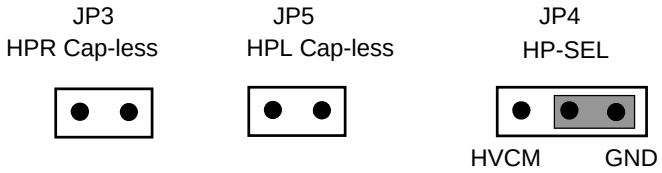


Figure 11. HP Output Circuit (Single-ended mode)

Set up the jumper pins.



b. Differential mode

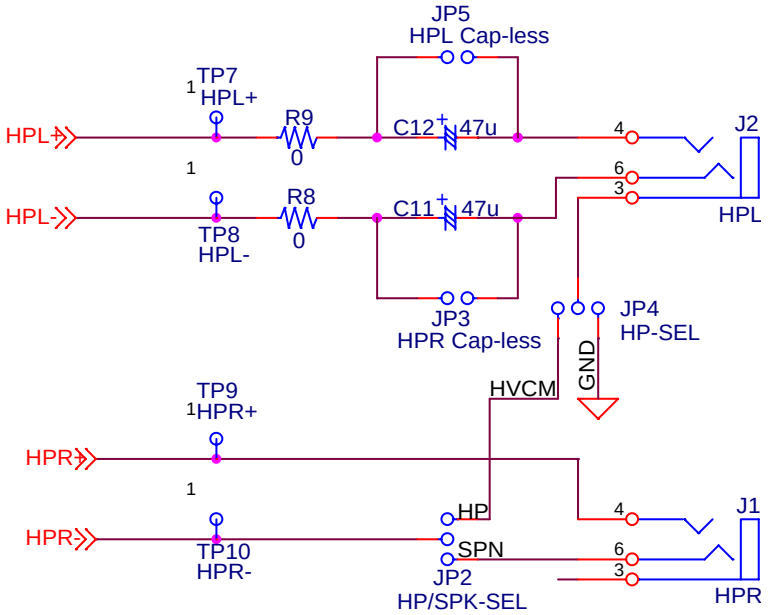
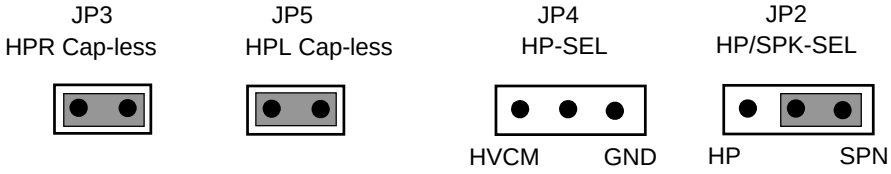


Figure 12. HP Output Circuit (Differential mode)

Set up the jumper pins.



c. Pseudo cap-less mode

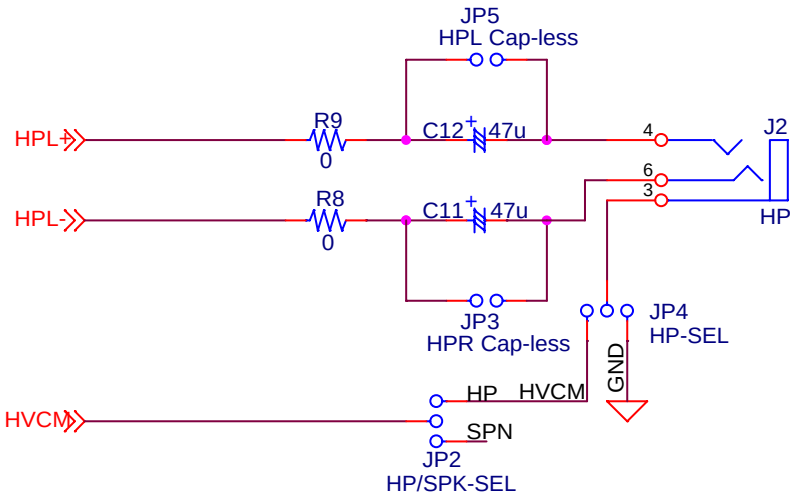
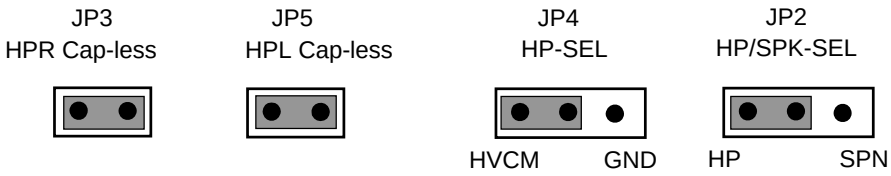


Figure 13. HP Output Circuit (Pseudo cap-less mode)

Set up the jumper pins.



3) Speaker Output Circuit <default>

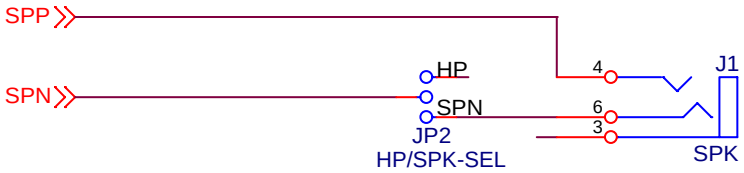
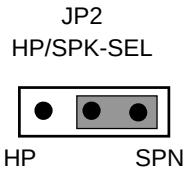


Figure 14. Speaker Output Circuit

Set up the jumper pins.



∗ AKEMD assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4373 according to previous term.

2. Connect IBM-AT compatible PC with AKD4373 by 10-line type flat cable (packed with AKD4373). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4373 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4373.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button.

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default]: Initialize the register of AK4373.
3. [All Write]: Write all registers that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4373 click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4373 click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate Digital Volume.

There are dialogs corresponding to register of 09h, 0Ah, 0Ch and 0Dh.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4373 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4373 click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4373. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button. The default setting sequence DAC->HP (3D=OFF) is displayed. Jump to (3) below if the default setting sequence is used. Go to (2) if the other setting sequence is required.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval = "-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

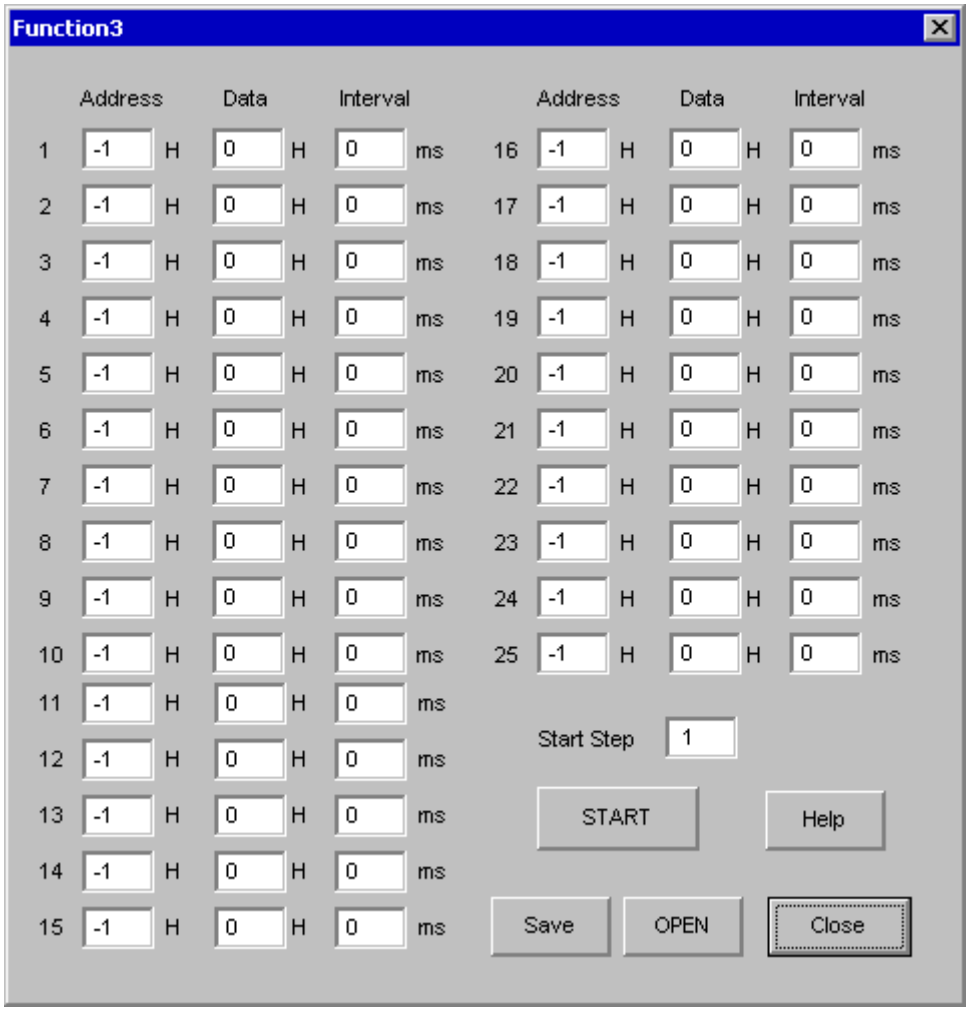


Figure 15. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 16 opens.

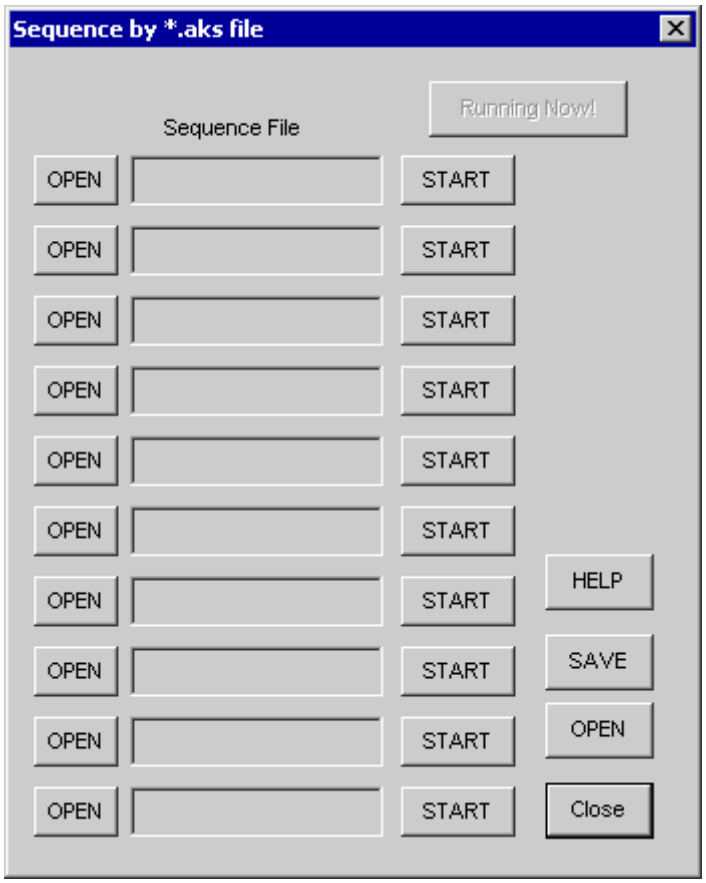


Figure 16. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 17. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

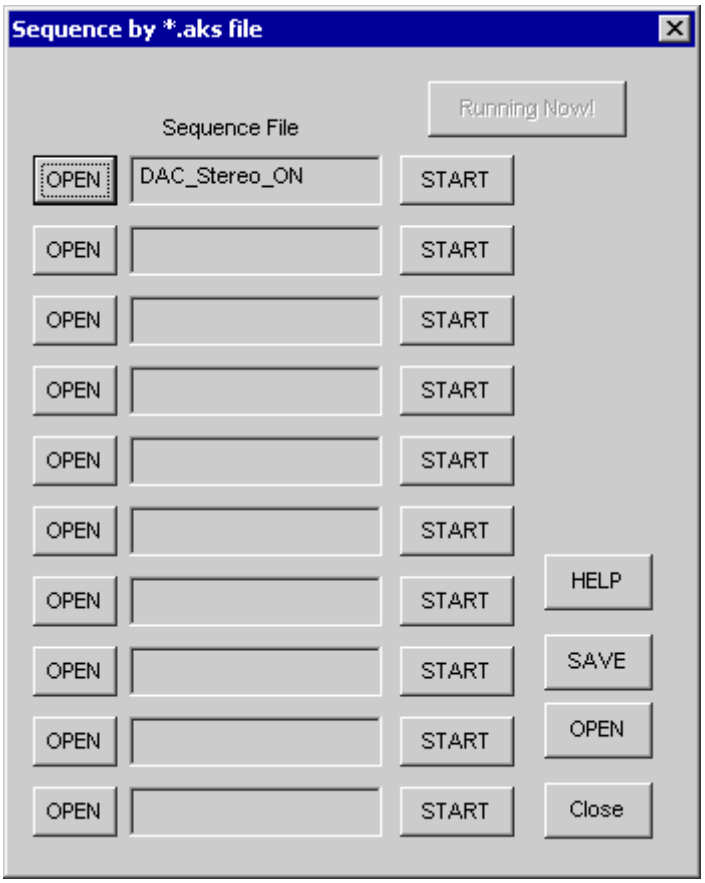


Figure 17. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN]: The name assign of sequence file (*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file (*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 18 opens.

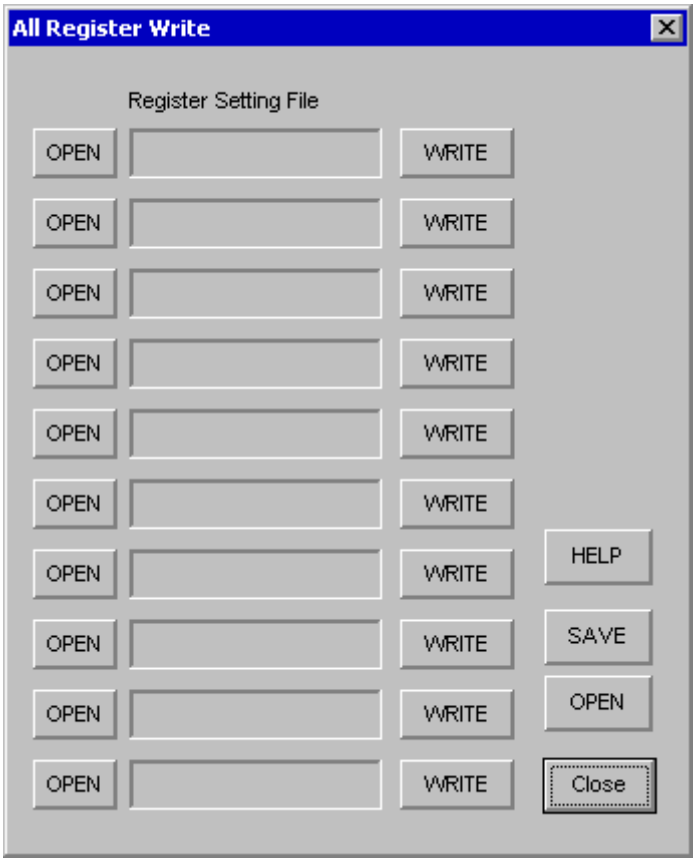


Figure 18. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 19. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

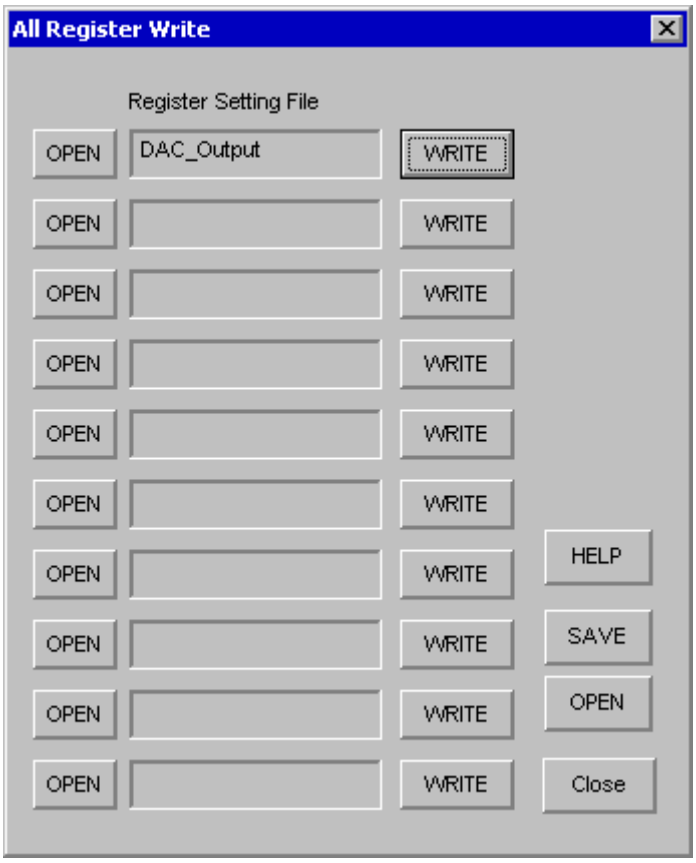


Figure 19. [F5] window (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN]: The name assign of register setting file (*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

8. [Filter Dialog]

This dialog can easily set the AK4373's programmable filter.
A calculation of a coefficient of Digital Programmable Filter such as HPF, EQ filter ,a write to a register and check frequency response.
Window to show to Figure 20 opens when push a [Filter] button.

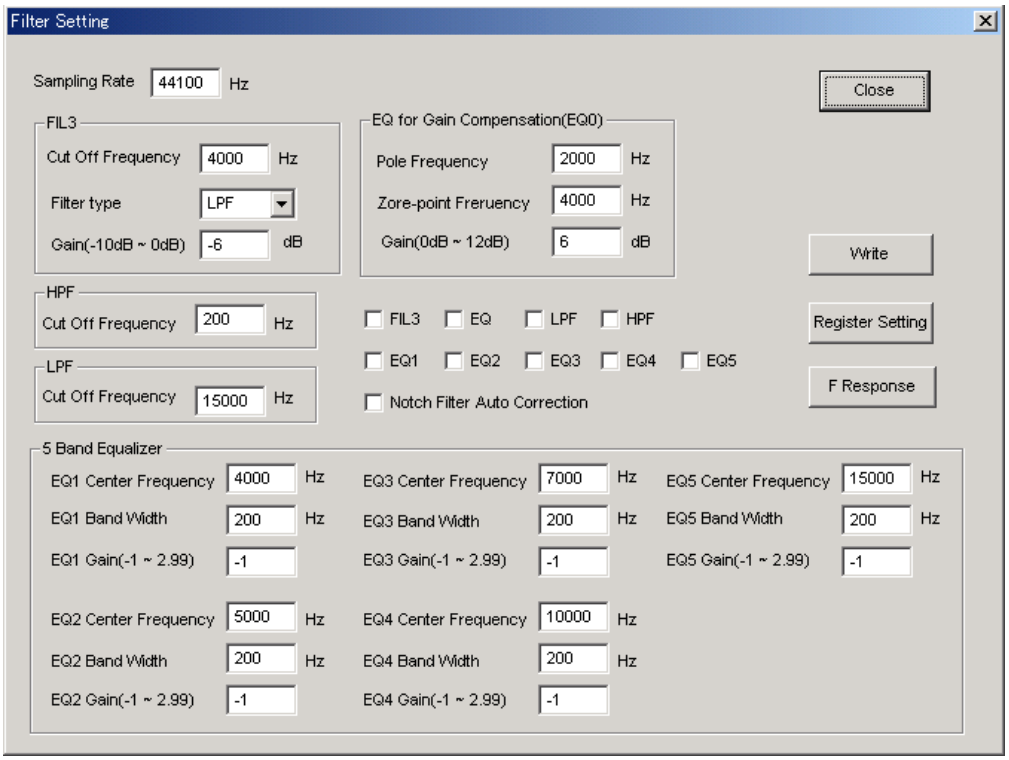


Figure 20. [Filter] window

8-1. Setting of a parameter

(1) Please set a parameter of each Filter.

Item	Contents	Setting range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
FIL3		
Cut Off Frequency	Stereo separation emphasis filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Filter type	Type of stereo separation emphasis filter	LPF or HPF
Gain	Gain of stereo separation emphasis filter	–10dB ≤ Gain ≤ 0dB
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
LPF		
Cut Off Frequency	Low pass filter cut off frequency	fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs)
EQ for Gain Compensation (EQ)		
Pole Frequency	Pole Frequency	fs/10000 ≤ Pole Frequency ≤ (0.497 * fs)
Zero-point Frequency	Zero-point Frequency	fs/10000 ≤ Zero-point Frequency ≤ (0.497 * fs)
Gain	Gain	0dB ≤ Gain ≤ +12dB
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-5 Band Width	EQ1-5 Band Width (Note 1)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-5 Gain	EQ1-5 Gain (Note 2)	-1≤ Gain < 3

Note 1. Bandwidth where the gain gap is 3dB compared with center frequency.
Note 2. When a gain is smaller than “0”, EQ1-5 becomes a notch filter.

(2) Please set ON/OFF of Filter with check buttons of “FIL3”, “EQ”, “LPF”, “HPF”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5”. When the button is checked, Filter becomes ON. When “Notch Filter Auto Correction” is checked, automatic compensation is executed for center frequency of notch filter.
(“Cf. 8-4. automatic compensation for center frequency of a notch filter”)

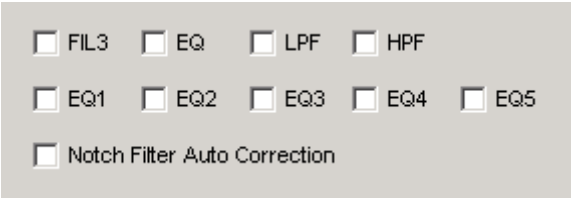


Figure 21. Filter ON/OFF setting button

8-2. A calculation of a register

A register setting values are displayed when [Register Setting] button is clicked. When any value is set to out or range, error message is displayed, and a calculation of register setting is not executed.

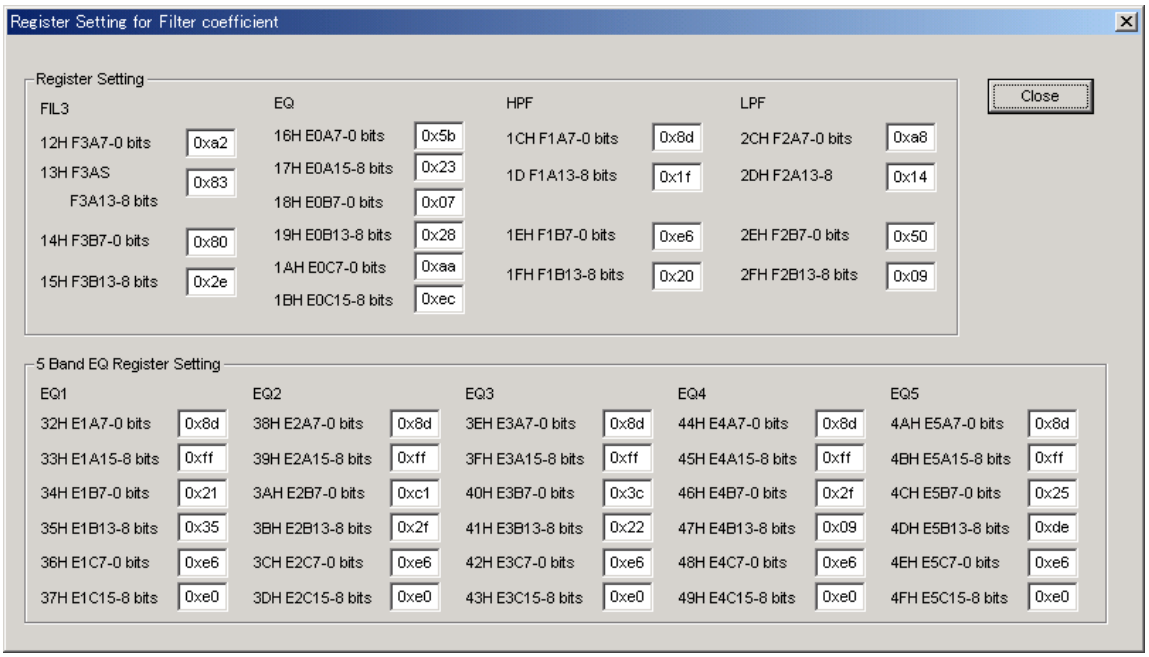


Figure 22. A register setting calculation result

In the following cases, a register set values are updated.

(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”.

8-3.Indication of a frequency characteristic

A frequency characteristic is displayed when [Frequency Response] button is clicked. The register values are updated at the same time.
If "Frequency Range" is changed, and [UpDate] button is clicked, indication of a frequency characteristic is updated.

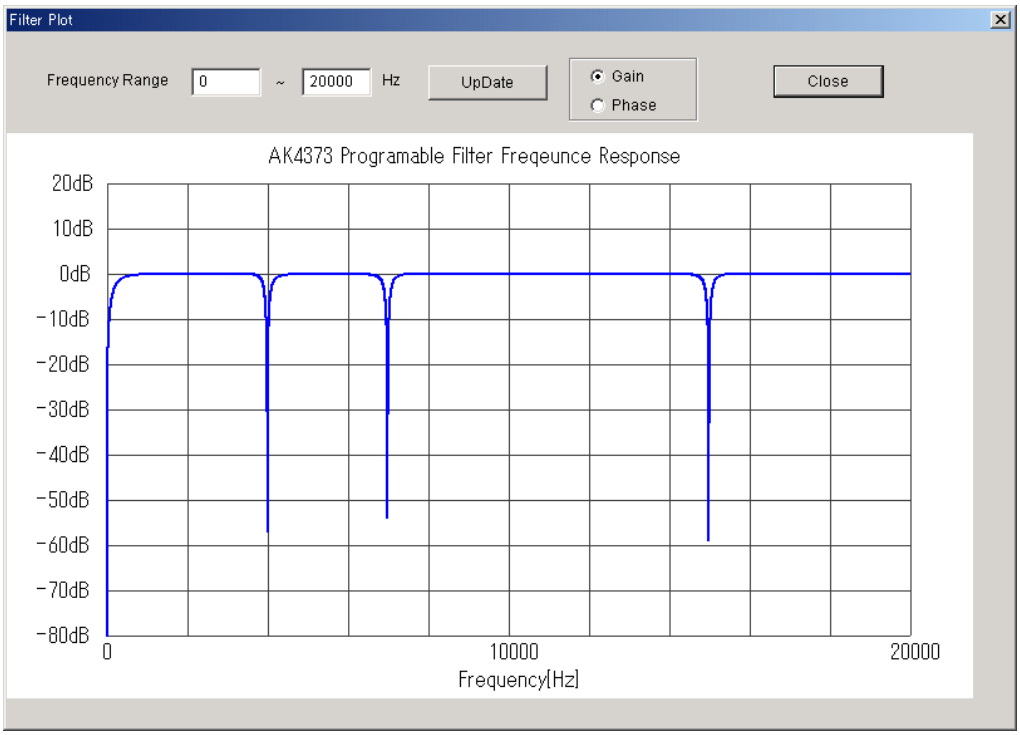


Figure 23. A frequency characteristic indication result

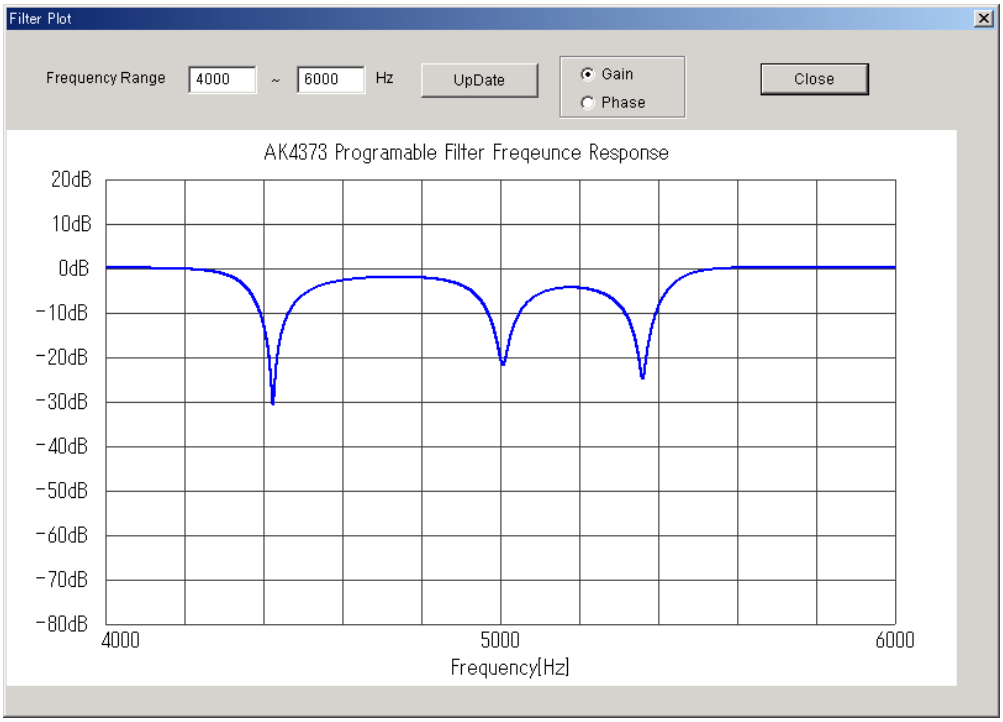
In the following cases, a register set values are updated.

(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button "Notch Filter Auto Correction".

8-4. Automatic compensation for center frequency of a notch filter

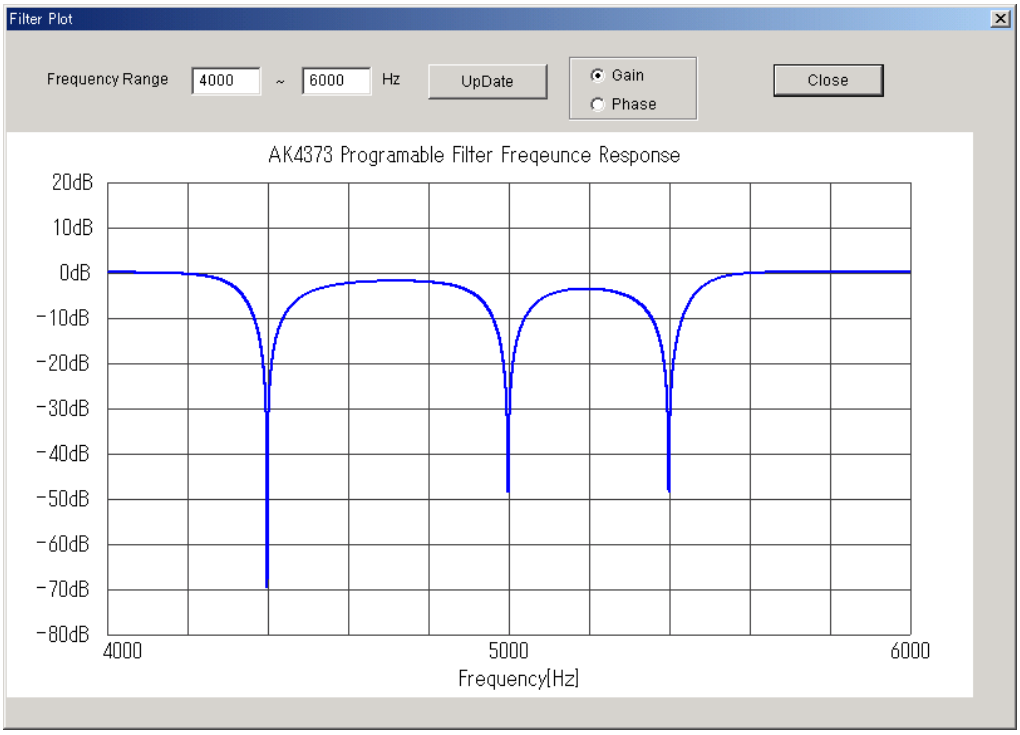
When a gain of 5 band Equalizer is set to "-1", Equalizer becomes a notch filter. When center frequency of several notch filters are near frequency each other, center frequency error occurs (Figure 24).
When "Notch Filter Auto Correction" button is checked, automatic compensation is executed for center frequency of a notch filter.
Register setting and frequency characteristics are displayed after automatic compensation (Figure 25).
This automatic compensation is available for Equalizer Band where a gain is set to "-1".

(Note) When distance among center frequencies is smaller than band width, there is a possibility that automatic compensation does not operate normally. Please confirm a compensation result by indication of a frequency characteristic.



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width: 200Hz (3 band common)

Figure 24. When there is no compensation of center frequency

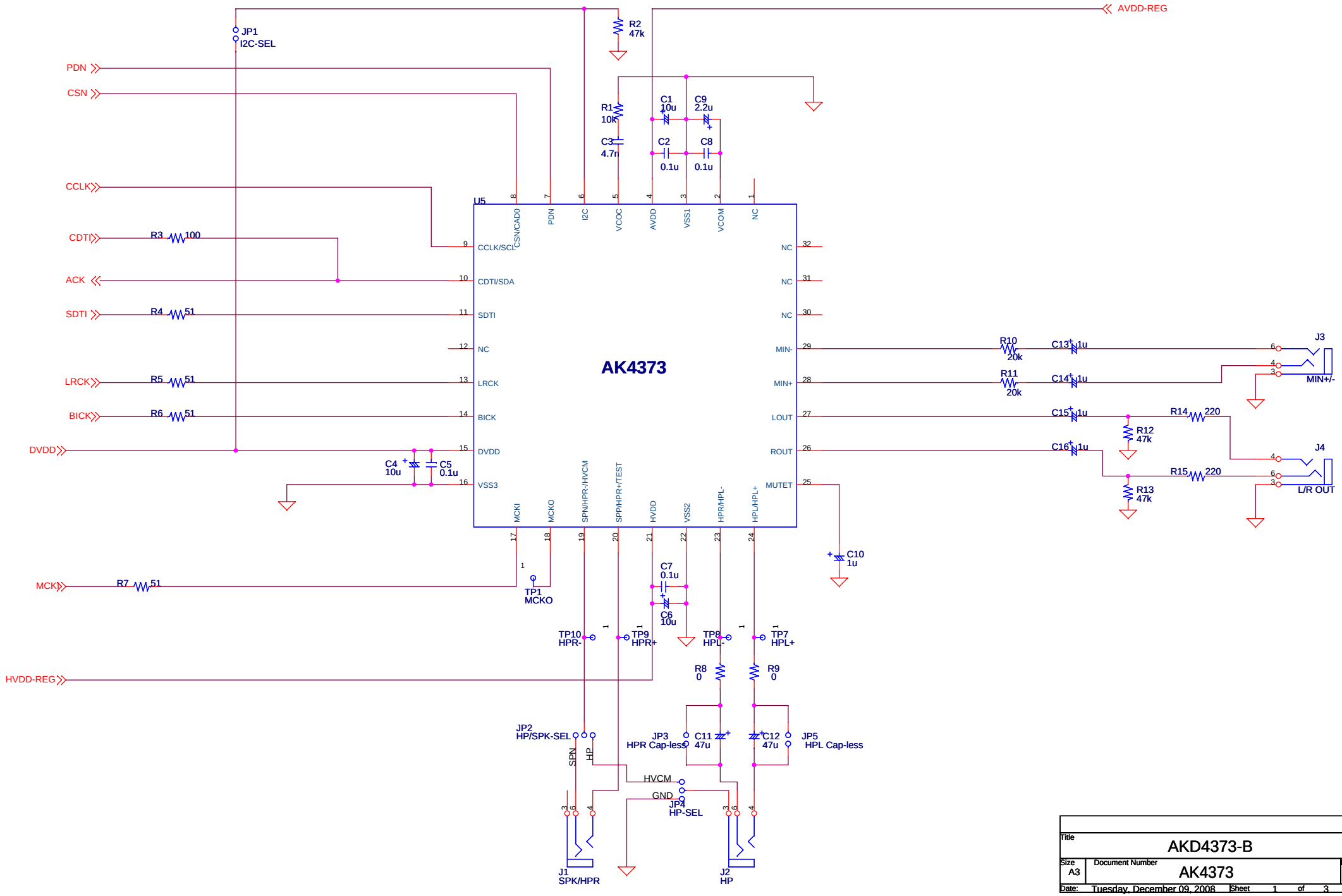


Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width: 200Hz (3 band common)

Figure 25. When there is compensation of center frequency

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
08/01/18	KM091600	0	First Edition		
08/06/20	KM091601	1	Parts Change	1	Board Revision: Rev.0 → Rev.1 AK4373: Rev. A → Rev. B
08/06/25			Error Correction	11	Figure 9 was changed. R10, R11: 0Ω → 20kΩ
08/07/01	KM091602		Error Correction	2	PORT2 and PORT3 were exchanged.
08/12/09	KM091603	2	Parts Change	1	Board Revision: Rev.1 → Rev.2
			Error Correction	5	Figure 26. PLL Master Mode (PLL Reference Clock: MCKI pin) →Figure 27. PLL Slave Mode
			Error Correction	10	Change in 3-wire Serial Control Mode,I^2C-bus Control Mode


AK4373
U5
JP1
I2C-SEL
R2
47k
AVDD-REG
PDN
CSN
CCLK
CDTI
ACK
SDTI
LRCK
BICK
DVDD
MCKI
R1
10k
C1
10u
C9
2.2u
C3
4.7n
C2
0.1u
C8
0.1u
R3
100
R4
51
R5
51
R6
51
R7
51
C4
10u
C5
0.1u
TP1
MCKO
C7
0.1u
C6
10u
C10
1u
R10
20k
R11
20k
C13
1u
C14
1u
C15
1u
C16
1u
R12
47k
R13
47k
R14
220
R15
220
J3
MIN+/-
J4
L/R OUT
TP10
HPR-
TP9
HPR+
TP8
HPL-
TP7
HPL+
R8
0
R9
0
HVDD-REG
JP2
HP/SPK-SEL
JP3
HPR Cap-less
C11
47u
C12
47u
JP5
HPL Cap-less
HVCM
GND
JP4
HP-SEL
J1
SPK/HPR
J2
HP
Title
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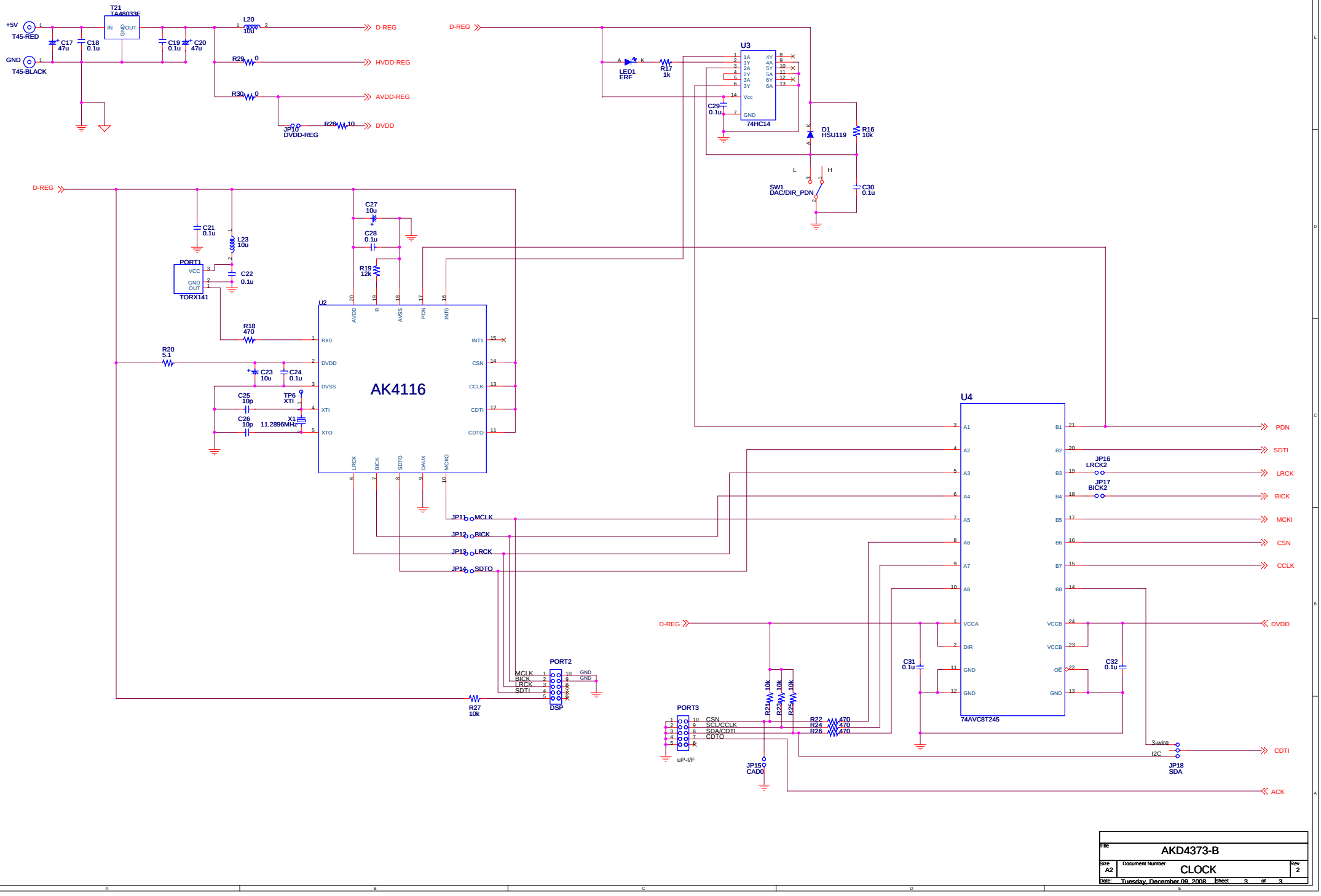

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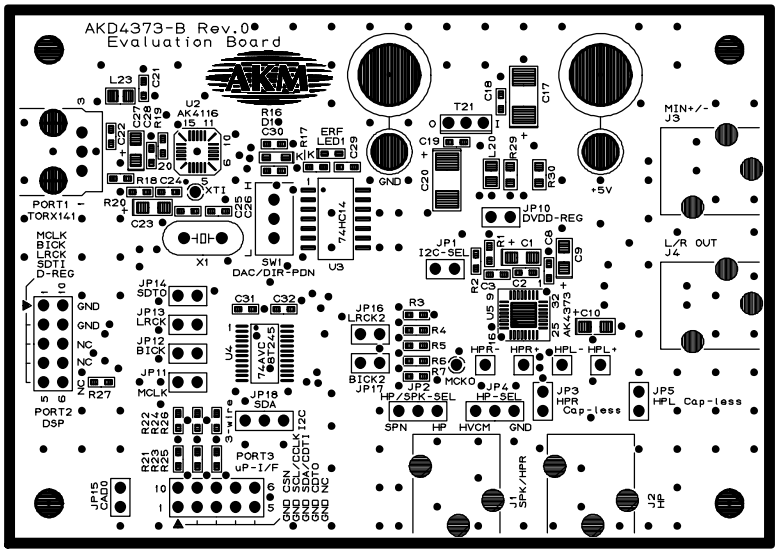
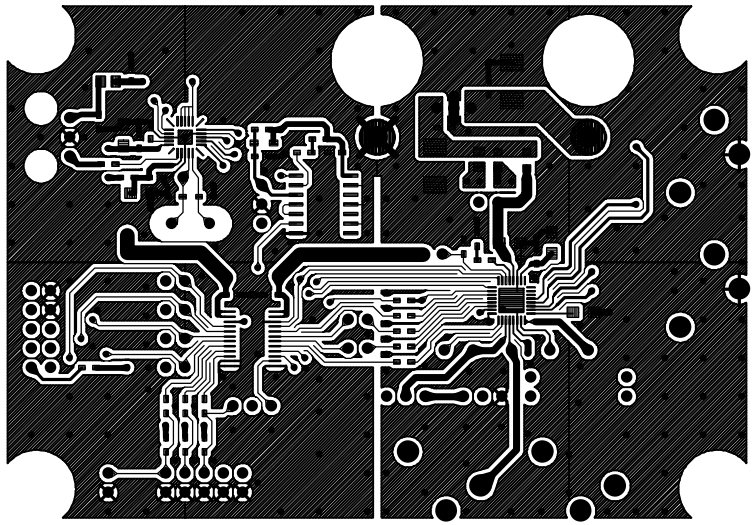


AKD4373-B MAIN L1 SILK

AKD4373-B MAIN L2 SILK



AKD4373-B MAIN L1

AKD4373-B MAIN L2