AKD5397-SB

AK5397 Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD5397-SB is an evaluation board for AK5397, which is 32bit,768kHz,2ch ADC.
The AKD5397-SB is includes the the analog input circuit and also has a digital interface transmitter.
Further, the AKD5397-SB can achieve the interface with digital audio systems via BNC-connector.

■ **Ordering guide**

AKD5397-SB -- Evaluation board for AK5397

FUNCTION

- **DIT with BNC digital output**
- **BNC connector for an external clock input**

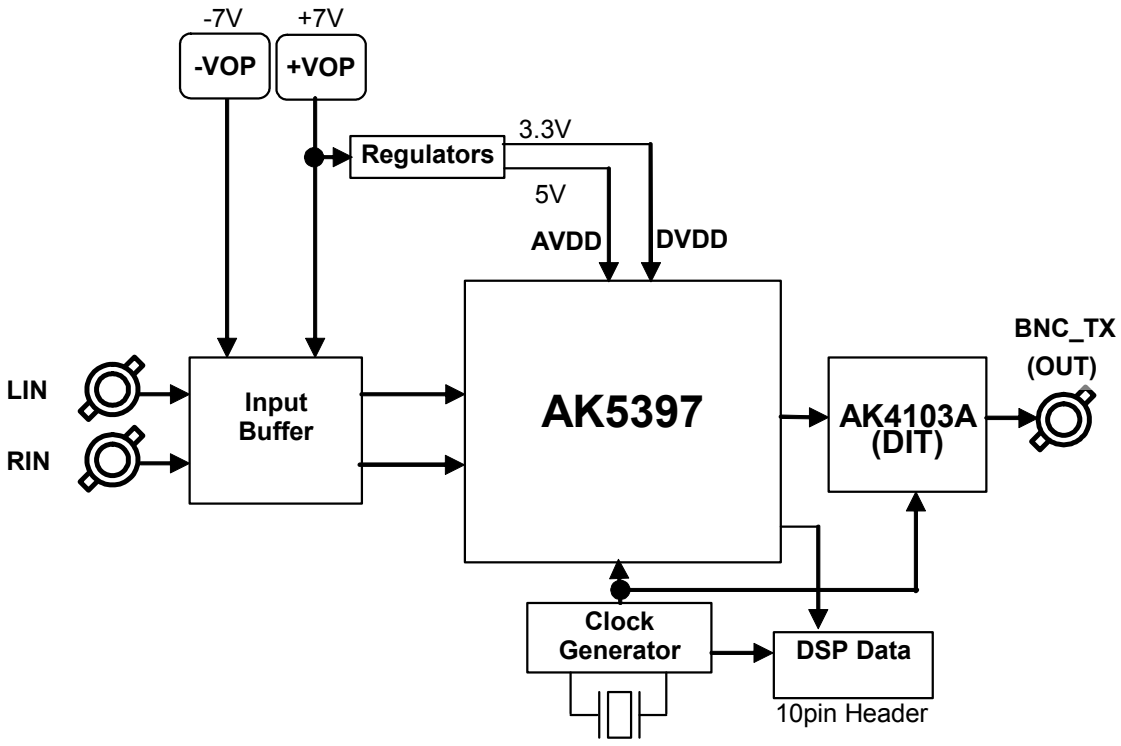

Figure 1. AKD5397-SB Block Diagram

Evaluation Board Diagram

■ **Board Diagram**

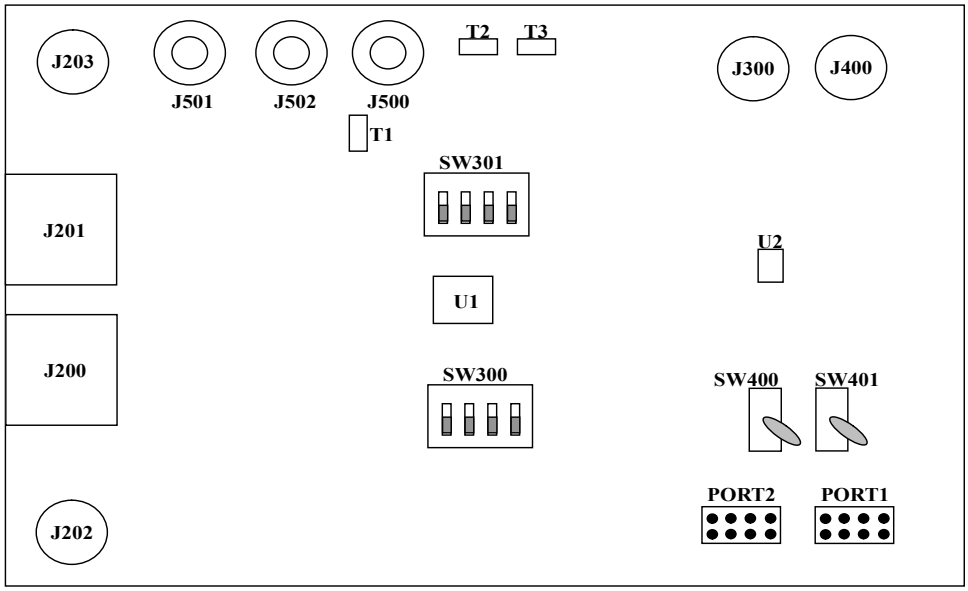

Figure 2. AKD5397-SA Board Diagram

■ **Description**

(1) U1 (AK5397)
32bit,768kHz,2ch A/D Converter.

(2) J200,J201 (Analog data)
Cannon connector : Differential Analog Input

(3) J300 (Digital data)
BNC Connector : Digital Output.

(4) J500, J501, J502 (Power supply)
Power Supply Connector.

(5) PORT1 (pin header)
Pin header for evaluation (MCLK, BICK, LRCK).

(6) PORT2 (Digital Data)
Pin header for evaluation (SDTO1,SDTO2,TDMIN1,TDMIN2).

(7) U2 (AK4103A)
AK4103A has DIT. Transports output data from AK5397.

(8) SW400 (Toggle switch)
Toggle type-switch PDN for AK5397.
"H" : PDN = High
"L" : PDN = Low

(9) SW401 (Toggle switch)
Toggle type-switch PDN for AK4103A.
"H" : PDN = High
"L" : PDN = Low

(10) SW300,SW301 (Dip switch)
DIP type-switch for AK5397, AK4103A. (Table2.-Table6.)
(11) J203,J202 (Analog data)
BNC Connector : Single-ended Analog Input.
(12) J400 (MCLK external input)
BNC Connector : External Clock Input (MCLK).
(13) T1, T2, T3
Regulator for AK5397, AK4103A, Logic Circuit.

Evaluation Board Manual

■ **Operation sequence**

[1] Power supply line settings

[2] Evaluation modes

[2-1] Slave Mode

(2-1-1) A/D evaluation using DIT function of AK4103A

(2-1-2) Feeding all clocks from PORT1 (CLOCK)

(2-1-3) Input/Output digital data from PORT2 (DATA)

[2-2] Master Mode

(2-2-1) A/D evaluation using DIT function of AK4103A

(2-2-2) Feeding all clocks from PORT1 (CLOCK)

(2-2-3) Input/Output digital data from PORT2 (DATA)

[3] DIP switches settings

[4] Clock / Data format settings

[5] Toggle switches settings

[6] Analog input Circuit

[1] Power supply line settings

(1) Power supply settings : Used the regulator (T1,T2,T3) <Default>

Set up the power supplied lines :

* Each supply line should be distributed from the power supply unit.

Name	Color	Setting (Typ)	Comments
J500(+7V)	Green	+7V	For Op-amp and Regulator
J501(-7V)	Blue	-7V	For Op-amp and Regulator
J502(VSS)	Black	0V	Ground

Table 1-1. Power supply line setting (default : used the regulator)

(2) About short resistance for power supply :

The roles of the short resistance for each power supply supplied from the regulator are as follows.

Connection of the short resistance for power supply :

Name (Resistance)	Processing	Name (power supply)	Comments
R510	Short	AVDD1	AVDD for AK5397
R500	Short	VBIAS	Bias for Op-amp
R511	Short	VCC1	VCC for AK4103A and Logic IC
R501	Short	VCC2	Spare terminal VCC
R512	Short	DVDD1	VDD for AK5397 and Logic IC
R502	Short	DVDD2	VDD for DIP SW

Table 1-2. Short resistance for power supply (Default : Short)

[2] Evaluation modes

[2-1] Slave Mode

(2-1-1) A/D evaluation using DIT function of AK4103A

*J300 (BNC_TX) used. DIT generates audio bi-phase signal from received data and which is output throurh BNC connector (BNC_TX). It is possible to connect AKM's D/A converter evaluation boards and the digital-amplifier through the BNC connector.

*Nothing should be connected to PORT1 (CLOCK), PORT2 (DATA).

*In case of using external clock (MCLK) through a BNC connector (J400), short R423(EXT) and R422 by 0ohm resistance, and open R421 (XTL).

*In case of default setting, SDTO1 of AK5397 output data is output through J300 (BNC_TX).
In case of short R442(SDTO) by 0ohm resistance and open R441(SDTO), SDTO2 of AK5397 output data is output through J300 (BNC_TX).

(2-1-2) Feeding all clocks from PORT1 (CLOCK)

*Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT1 (CLOCK).
Short R440(MCLK), R438(BICK), R436(LRCK) by 0ohm resistance.
Open R439(MCLK), R437(BICK), R435(LRCK).

(2-1-3) Input/Output digital data from PORT2 (DATA)

*The A/D converted data is output from SDTO1, SDTO2 of PORT2 (DATA).

*IN case of using digital data through TDMIN1 pin, TDMIN2 pin of AK5397, digital data is input through TDMIN1 or TDMIN2 of PORT2 (DATA).

[2-2] Master Mode

(2-2-1) A/D evaluation using DIT function of AK4103A

*Signals (BICK, LRCK) output from AK5397 used.
Open R437 and R438 (BICK), R435 and R436 (LRCK).

*J300 (BNC_TX) used. DIT generates audio bi-phase signal from received data and which is output throurh BNC connector (BNC_TX). It is possible to connect AKM's D/A converter evaluation boards and the digital-amplifier through the BNC connector.

*Nothing should be connected to PORT1 (CLOCK), PORT2 (DATA).

*In case of using external clock (MCLK) through a BNC connector (J400), short R423(EXT) and R422 by 0ohm resistance, and open R421 (XTL).

*In case of default setting, SDTO1 of AK5397 output data is output through J300 (BNC_TX).
In case of short R442(SDTO) by 0ohm resistance and open R441(SDTO), SDTO2 of AK5397 output data is output through J300 (BNC_TX).

(2-2-2) Feeding all clocks from PORT1 (CLOCK)

*Under the following set-up, the external clock (MCLK) can be fed through PORT1 (CLOCK).
Short R440(MCLK) by 0ohm resistance.
Open R439(MCLK).

(2-2-3) Input/Output digital data from PORT2 (DATA)

*The A/D converted data is output from SDTO1, SDTO2 of PORT2 (DATA).

*IN case of using digital data through TDMIN1 pin, TDMIN2 pin of AK5397, digital data is input through TDMIN1 or TDMIN2 of PORT2 (DATA).

[3] DIP switches settings

[SW300] (MODE): Evaluation Mode setting for AK5397 and AK4103A

*ON="H", OFF="L"

No.	Name	OFF ("L")	ON ("H")	Default
1	HPFE	HPF OFF	HPF ON	ON ("H")
2	CKS0	Table 3-1		ON ("H")
3	CKS1			OFF ("L")
4	CKS2			OFF ("L")
5	DIT0	Table 4		ON ("H")
6	DIT1			ON ("H")
7	—	N/A	N/A	OFF ("L")
8	—	N/A	N/A	OFF ("L")

Table 2. Mode setting

M_SN	CKS2	CKS1	CKS0	MCLK	BICK	Sampling	
L	L	L	L	256fs	64fs≦BICK≦128fs	Normal Speed Mode (8kHz≦fs≦48kHz)	
	L	L	H	Table3-2		Auto Setting Mode	Default
	L	H	L	256fs	64fs	Double Speed Mode (48kHz≦fs≦96kHz)	
	L	H	H	128fs	64fs	Quad Speed Mode (96kHz≦fs≦192kHz)	
	H	L	L	64fs	64fs	Octal Speed Mode (fs=384kHz)	
	H	L	H	32fs	32fs	Hex Speed Mode (fs=768kHz)	
	H	H	L	N/A	N/A	N/A	
	H	H	H	N/A	N/A	N/A	
H	L	L	L	256fs	64fs	Normal Speed Mode (8kHz≦fs≦48kHz)	
	L	L	H	512fs	64fs		
	L	H	L	256fs	64fs	Double Speed Mode (48kHz≦fs≦96kHz)	
	L	H	H	128fs	64fs	Quad Speed Mode (96kHz≦fs≦192kHz)	
	H	L	L	64fs	64fs	Octal Speed Mode (fs=384kHz)	
	H	L	H	32fs	32fs	Hex Speed Mode (fs=768kHz)	
	H	H	L	N/A	N/A	N/A	
	H	H	H	N/A	N/A	N/A	

Table 3-1. MCLK frequency setting for AK5397

MCLK	BICK	fs
512fs	64fs≦BICK≦128fs	Normal Speed Mode (8kHz≦fs≦48kHz)
256fs	64fs	Double Speed Mode (48kHz≦fs≦96kHz)
128fs	64fs	Quad Speed Mode (96kHz≦fs≦192kHz)
64fs	64fs	Octal Speed Mode (fs = 384kHz)
32fs	32fs	Hex Speed Mode (fs = 768kHz)

Table 3-2. MCLK / BICK frequency setting for AK5397 (Auto Setting Mode: Slave Mode)

Mode	DIT1	DIT0	MCLK	fs	
0	L	L	128fs	28k ~ 216kHz	
1	L	H	256fs	28k ~ 108kHz	
2	H	L	384fs	28k ~ 54kHz	
3	H	H	512fs	28k ~ 54kHz	Default

Table 4. MCLK frequency setting for AK4103A

[SW301] (MODE): Evaluation Mode setting for AK5397 and AK4103A
*ON="H", OFF="L"

No.	Name	OFF ("L")	ON ("H")	Default
1	MONO	Stereo Mode	Mono Mode	OFF ("L")
2	TDM0	Table 6		OFF ("L")
3	TDM1			OFF ("L")
4	M_SN	Slave Mode	Master Mode	OFF ("L")
5	DIF	MSB justified	I^2S Compatible	OFF ("L")
6	SDFIL	Short Delay	Minimum Phase	OFF ("L")
7	SDM1	Normal Output	"L" output	OFF ("L")
8	SDM2	Normal Output	"L" output	OFF ("L")

Table 5. Mode setting

TDM1	TDM0	Mode	
L	L	Normal	Default
L	H	TDM256	
H	L	N/A	
H	H	TDM128	

Table 6. TDM Mode setting for AK5397

[4] Clock / Data format settings

(1) Settings of Clocks (BICK, LRCK)

Clock speed settings of BICK, LRCK can be set change by switching CLK1, CLK2.

fs	MCLK	BICK				
		R431 (MCLK/8)	R432 (MCLK/4)	R433 (MCLK/2)	R434 (MCLK/1)	
32kHz	256fs = 8.192MHz	32fs	64fs	128fs	256fs	
	512fs = 16.384MHz	64fs	128fs	256fs	512fs	
44.1kHz	256fs = 11.2896MHz	32fs	64fs	128fs	256fs	
	512fs = 22.5792MHz	64fs	128fs	256fs	512fs	
48kHz	256fs = 12.288MHz	32fs	64fs	128fs	256fs	
	512fs = 24.576MHz	64fs	128fs	256fs	512fs	Default (R431=Short)
96kHz	256fs = 24.576MHz	32fs	64fs	128fs	256fs	
192kHz	128fs = 24.576MHz	-	32fs	64fs	128fs	
384kHz	64fs = 24.576MHz	-	-	32fs	64fs	
768kHz	32fs = 24.576MHz	-	-	-	32fs	

Table 7. BICK Clock setting

fs	MCLK	LRCK					
		R426 (MCLK/512)	R427 (MCLK/256)	R428 (MCLK/128)	R429 (MCLK/64)	R430 (MCLK/32)	
32kHz	256fs = 8.192MHz	-	1fs	-	-	-	
	512fs = 16.384MHz	1fs	-	-	-	-	
44.1kHz	256fs = 11.2896MHz	-	1fs	-	-	-	
	512fs = 22.5792MHz	1fs	-	-	-	-	
48kHz	256fs = 12.288MHz	-	1fs	-	-	-	
	512fs = 24.576MHz	1fs	-	-	-	-	Default (R426=Short)
96kHz	256fs = 24.576MHz	-	1fs	-	-	-	
192kHz	128fs = 24.576MHz	-	-	1fs	-	-	
384kHz	64fs = 24.576MHz	-	-	-	1fs	-	
768kHz	32fs = 24.576MHz	-	-	-	-	1fs	

Table 8. LRCK Clock setting

(2) Settings of Data Format (SDTO)

Audio Interface Format settings of SDTO can be set change by switching TDM1, TDM0, M/SN, DIF.

Mode		TDM1	TDM0	M/SN	DIF	SDTO	LRCK		BICK		
								I/O		I/O	
0	Normal	L	L	L (Slave)	L	32bit, MSB justified	H/L	I	Table 3-1	I	Default
1					H	32bit, I2S Compatible	L/H	I		I	
2				H (Master)	L	32bit, MSB justified	H/L	O		O	
3					H	32bit, I2S Compatible	L/H	O		O	
4	TDM256	L	H	L (Slave)	L	32bit, MSB justified	↑	I	256fs	I	
5					H	32bit, I2S Compatible	↓	I	256fs	I	
6				H (Master)	L	32bit, MSB justified	↑	O	256fs	O	
7					H	32bit, I2S Compatible	↓	O	256fs	O	
8	TDM128	H	H	L (Slave)	L	32bit, MSB justified	↑	I	128fs	I	
9					H	32bit, I2S Compatible	↓	I	128fs	I	
10				H (Master)	L	32bit, MSB justified	↑	O	128fs	O	
11					H	32bit, I2S Compatible	↓	O	128fs	O	
12	N/A	H	L	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

Table 9. Audio Interface Format setting for AK5397

[5] Toggle switches settings

Up="H", Down="L"

[SW400] (Power Down (PDN) for AK5397):

Power Down (PDN) Switch for AK5397

Reset AK5397 (U1) once by brining SW400 to "L" once upon power-up.

Keep "H" when AK5397 is in use; keep "L" when AK5397 is not in use.

[SW401] (Power Down (PDN) for AK4103A):

Power Down (PDN) Switch for AK4103A

Reset AK4103A (U2) once by brining SW401 to "L" once upon power-up.

Keep "H" when AK4103A is in use; keep "L" when AK4103A is not in use.

[6] Analog input Circuit

Cannon Connectors (J200,J201) : Differential analog input signals for AK5397

1) Analog input Circuit 1 : Op-amp = LME49990

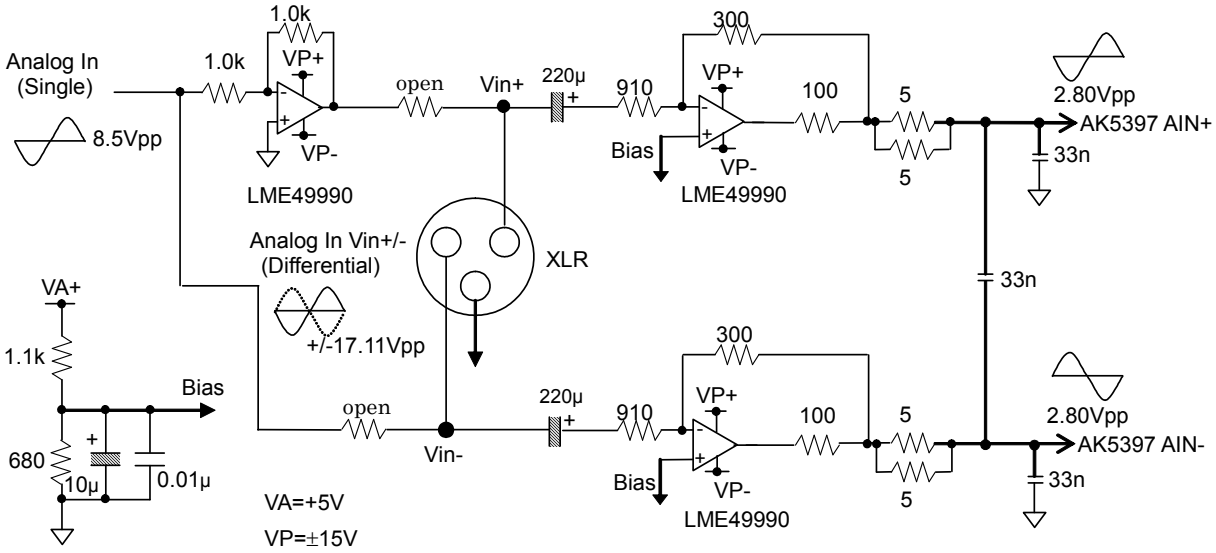

Figure 3. Analog Input Circuit 1 (Op-amp : LME49990)

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision, SYS-2722
- MCKI : 512fs/256fs/128fs (24.576MHz)
- BICK : 64fs
- fs : 48kHz / 96kHz / 192kHz
- Bit : 24bit
- Measurement Mode : ADC @ Slave Mode
- Power Supply : VOP+(15V)=7V, GND
  AVDD=5.0V (Regulator), DVDD=3.3V (Regulator)
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz @48kHz / 20～40kHz @96kHz / 20～80kHz @192kHz
- Temperature : Room

[Measurement Results]

1. Stereo ADC （Differential Inputs）

		Result		Unit
		Lch	Rch	
Stereo ADC : AINL/R => ADC => SDTO1				
S/(N+D)	fs = 48kHz (-1dBFS)	104.2	104.0	dB
	fs = 96kHz (-1dBFS)	103.8	103.7	dB
	fs = 192kHz (-1dBFS)	103.6	103.6	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	126.0	125.6	dB
S/N	fs = 48kHz (A-weighted)	126.1	126.8	dB

2. Mono ADC （Differential Inputs）

		Result		Unit
		Lch	Rch	
Mono ADC : AINL/R => ADC => SDTO1				
S/(N+D)	fs = 48kHz (-1dBFS)	103.7	103.6	dB
	fs = 96kHz (-1dBFS)	103.5	103.5	dB
	fs = 192kHz (-1dBFS)	103.4	103.4	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	128.9	128.8	dB
S/N	fs = 48kHz (A-weighted)	129.4	129.6	dB

[Plots]

fs = 48 kHz
AK5397 FFT (-1dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

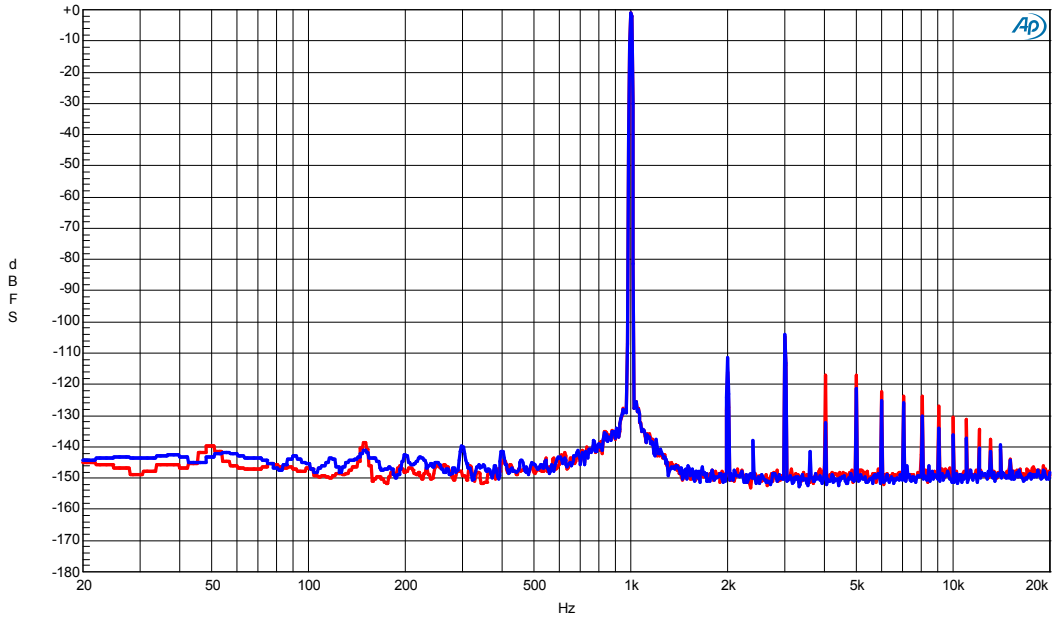

Figure 4. FFT (-1dBFS Input)

AK5397 FFT (-60dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

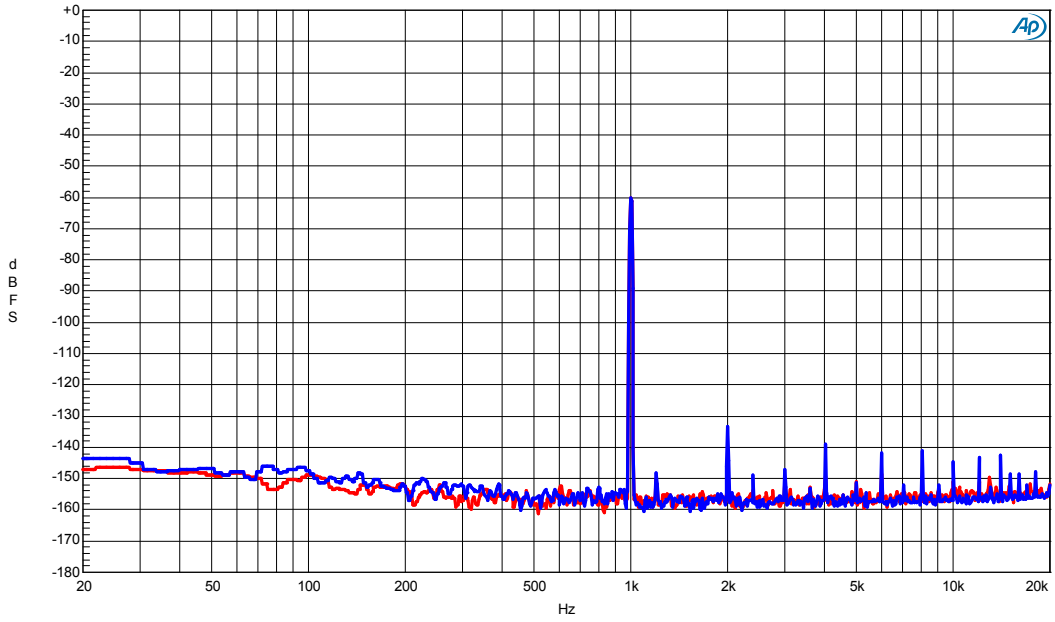

Figure 5. FFT (-60dBFS Input)

fs = 48 kHz
AK5397 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

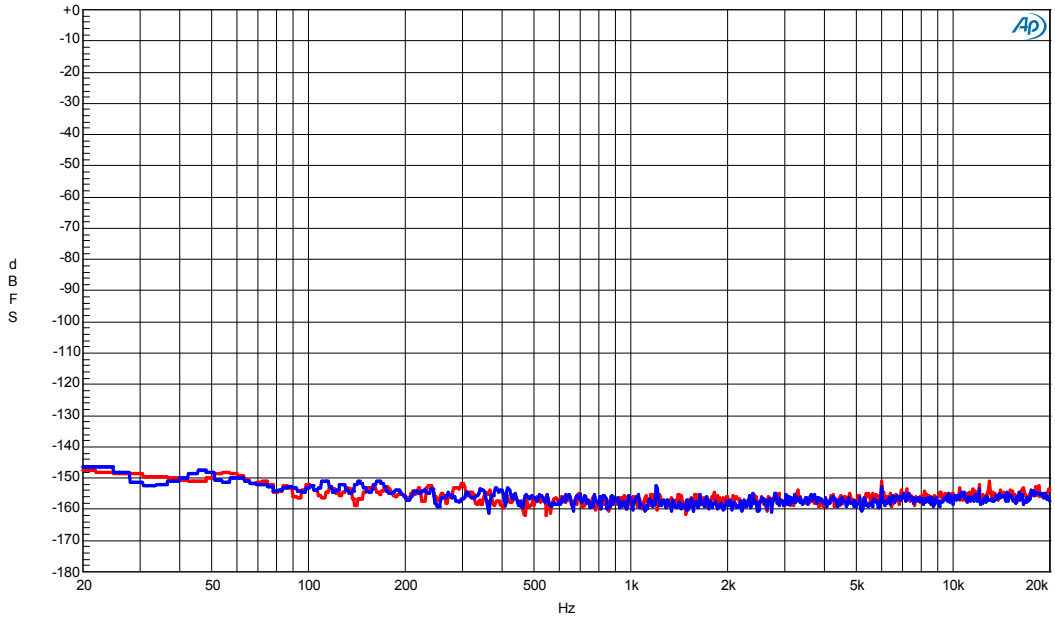

Figure 6. FFT (No Signal Input)

AK5397 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

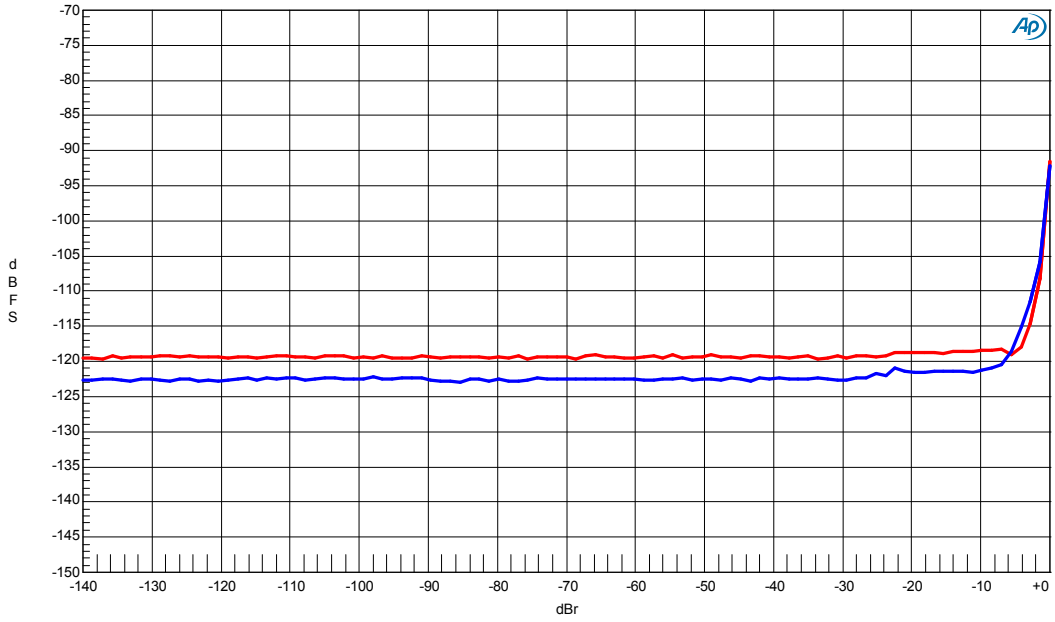

Figure 7. THD+N vs. Input Level

fs = 48 kHz
AK5397 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, -1dBFS Input

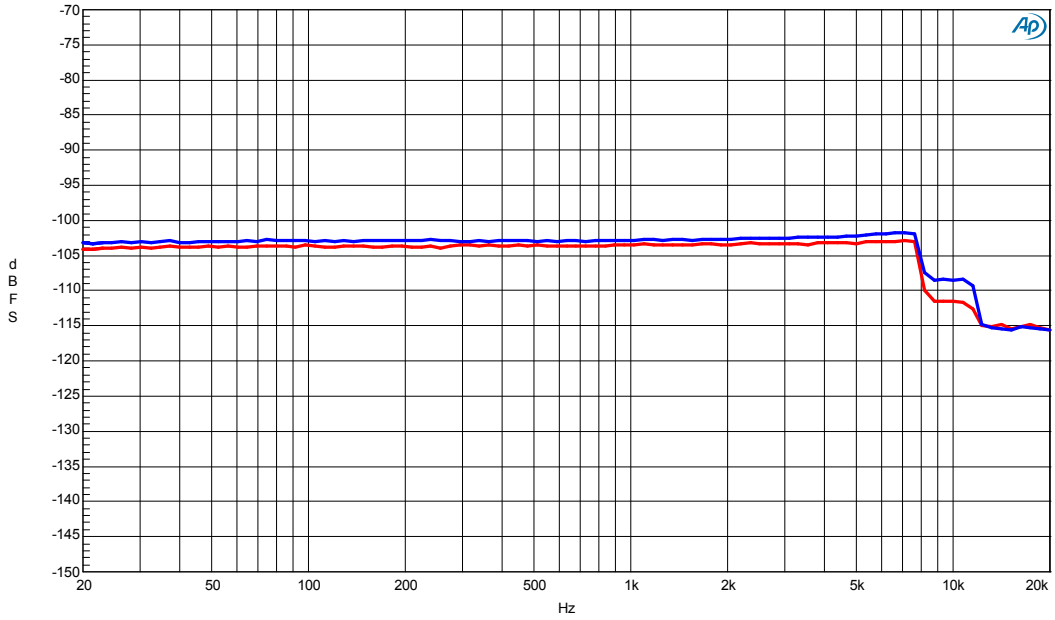

Figure 8. THD+N vs. Input Frequency

AK5397 Linearity
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

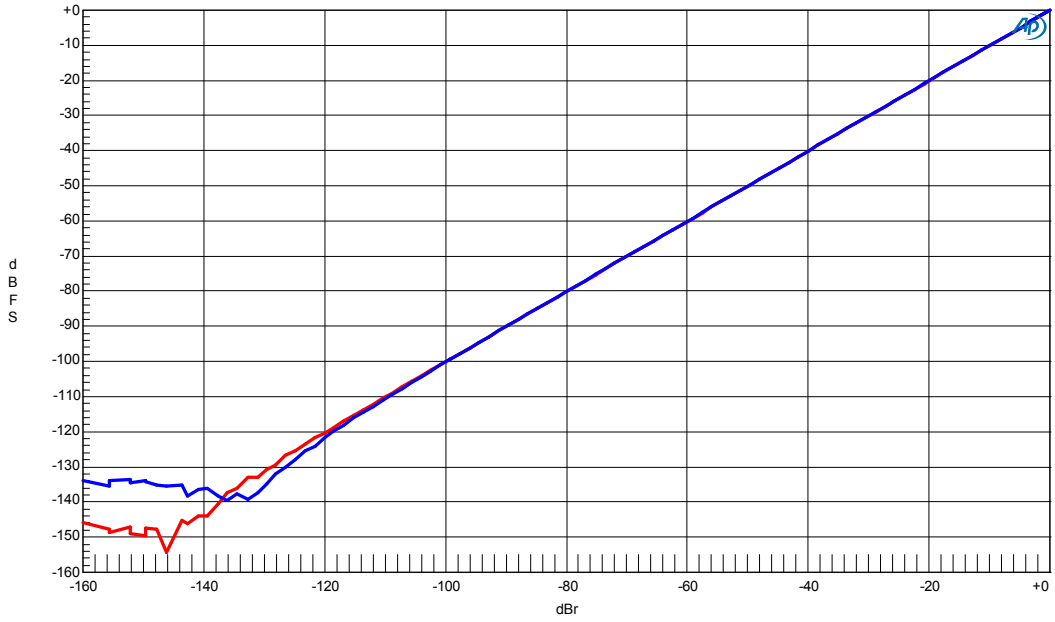

Figure 9. Linearity

fs = 48 kHz
AK5397 Frequency Response
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, -1dBFS input

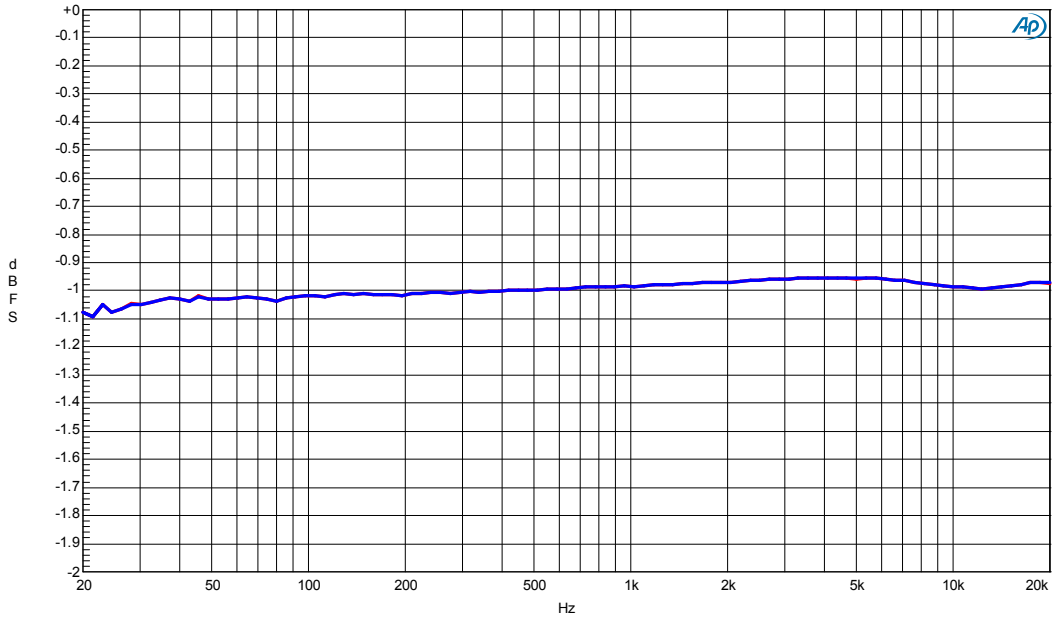

Figure 10. Frequency Response

AK5397 Crosstalk
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, -1dBFS Input

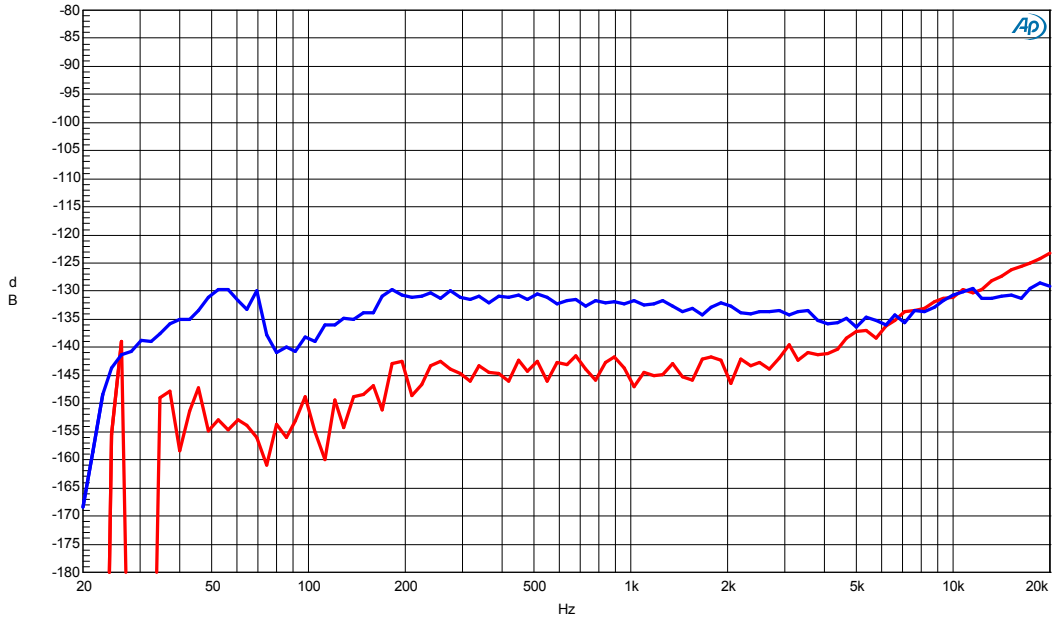

Figure 11. Crosstalk

fs = 96 kHz
AK5397 FFT (-1dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, fin=1kHz

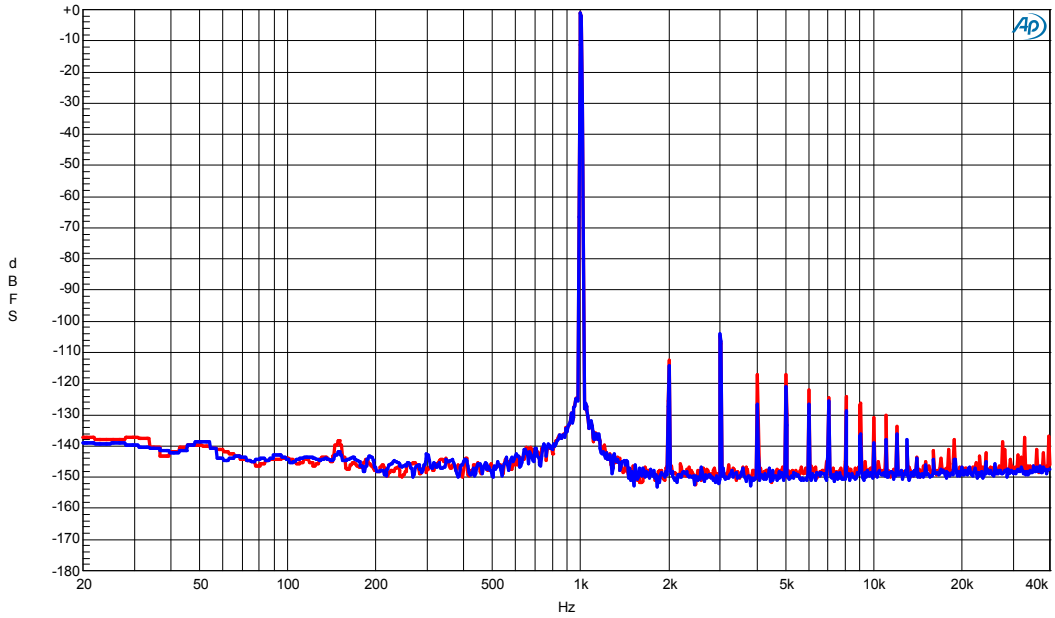

Figure 12. FFT (-1dBFS Input)

AK5397 FFT (-60dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, fin=1kHz

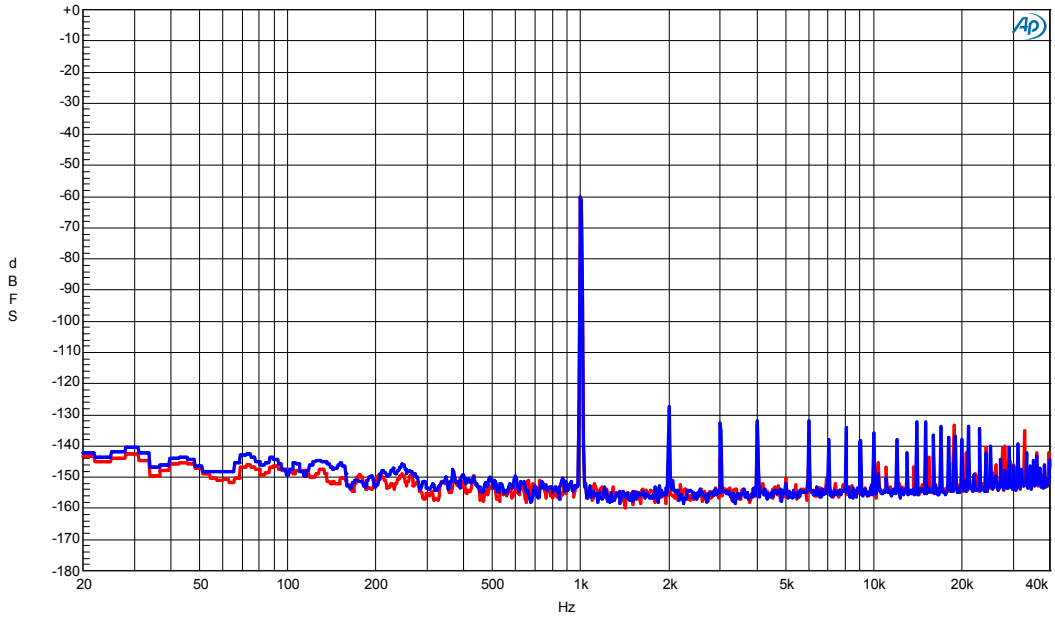

Figure 13. FFT (-60dBFS Input)

fs =96 kHz
AK5397 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, fin=1kHz

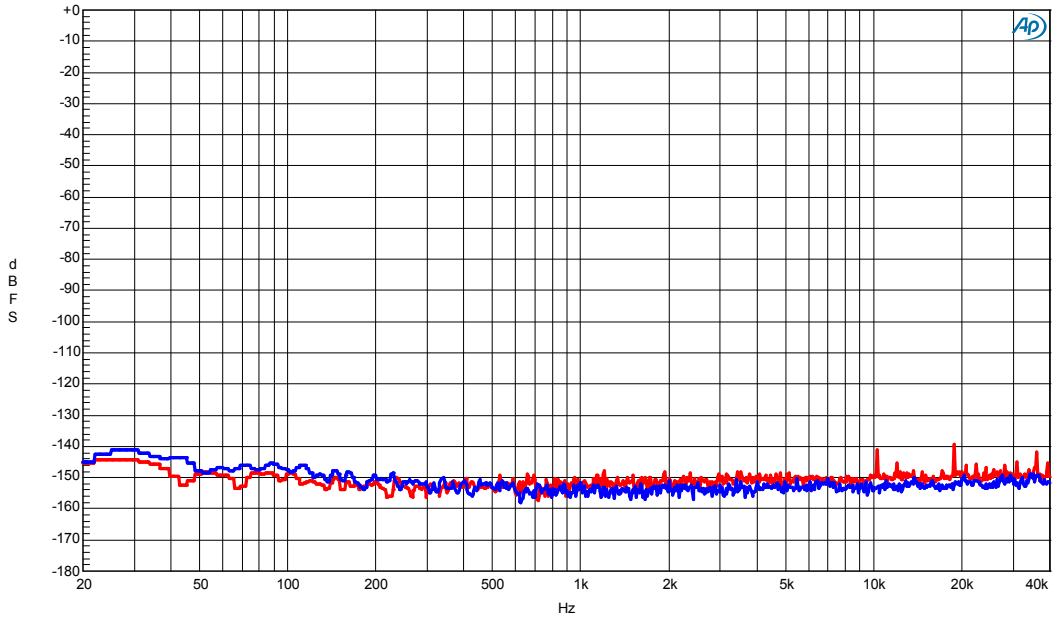

Figure 14. FFT (No Signal Input)

AK5397 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, fin=1kHz

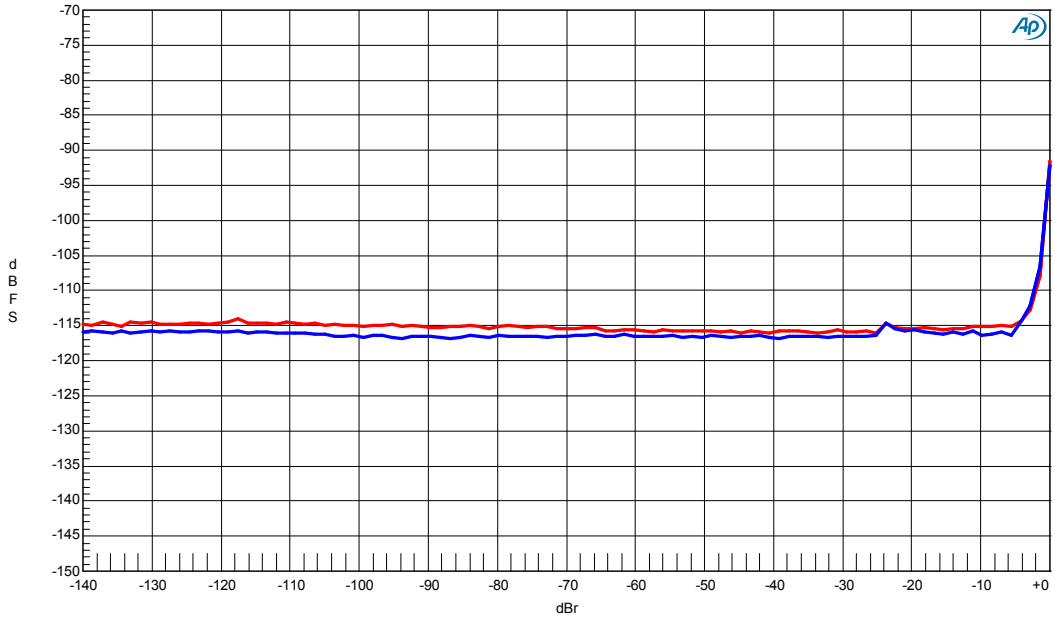

Figure 15. THD+N vs. Input Level

fs = 96 kHz
AK5397 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, -1dBFS Input

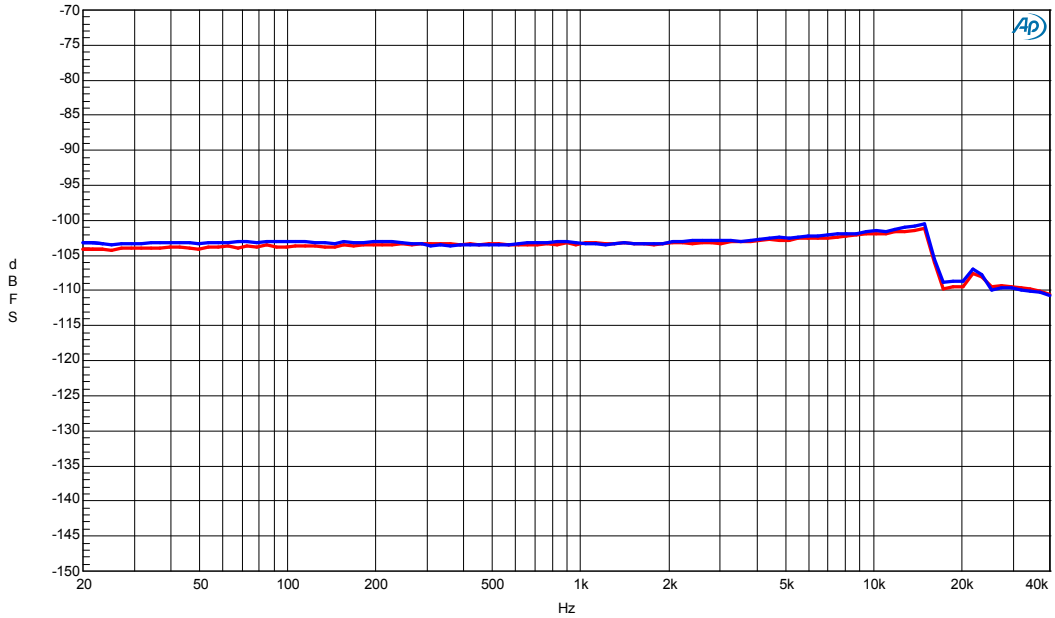

Figure 16. THD+N vs. Input Frequency

AK5397 Linearity
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, fin=1kHz

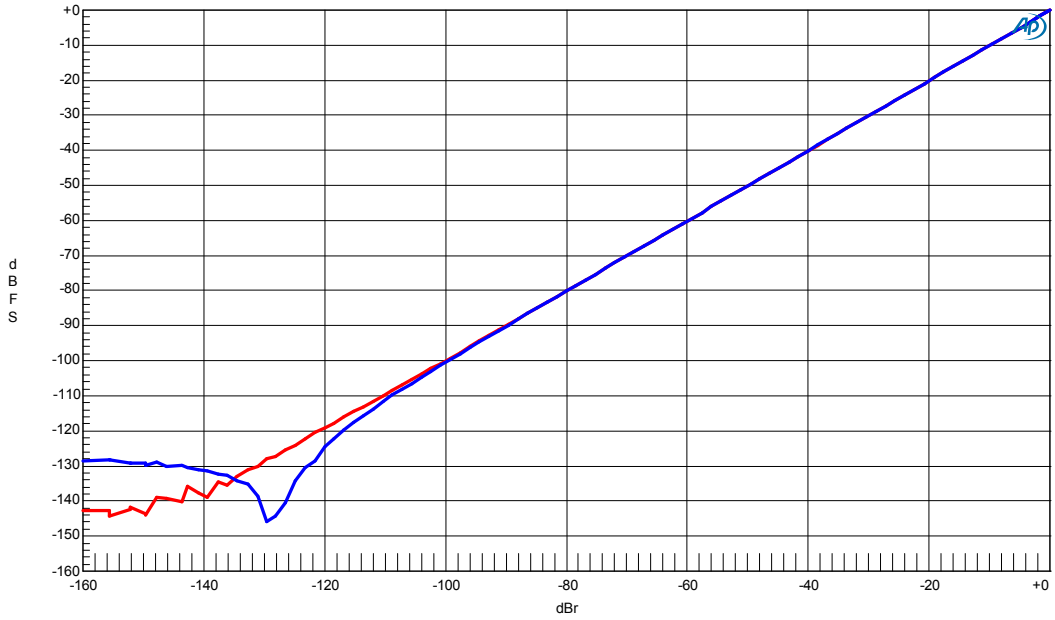

Figure 17. Linearity

fs = 96 kHz
AK5397 Frequency Response
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, -1dBFS Input

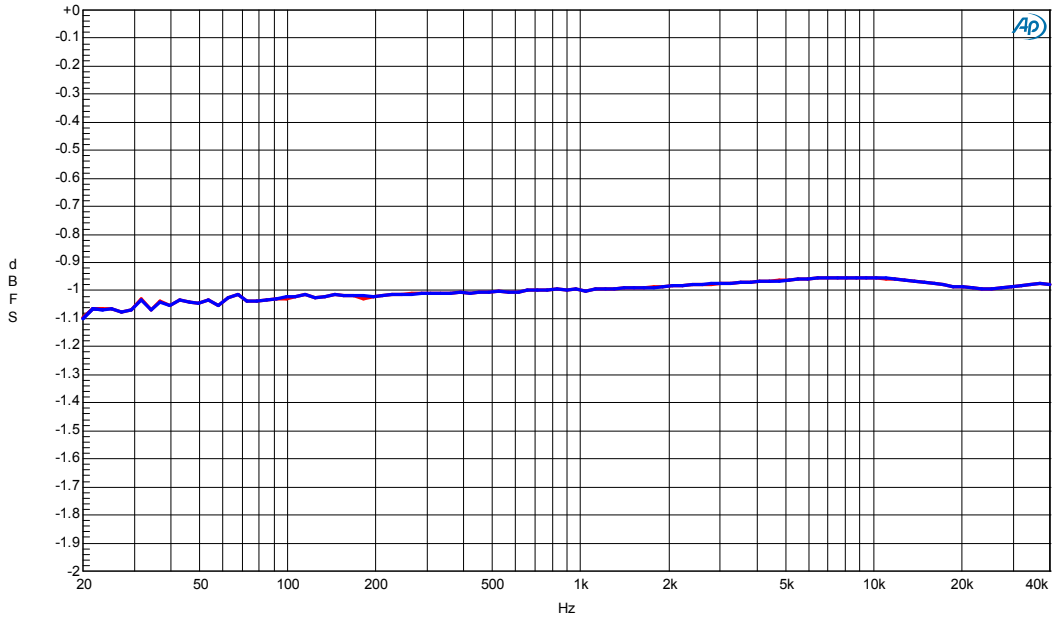

Figure 18. Frequency Response

AK5397 Crosstalk
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=256fs, -1dBFS Input

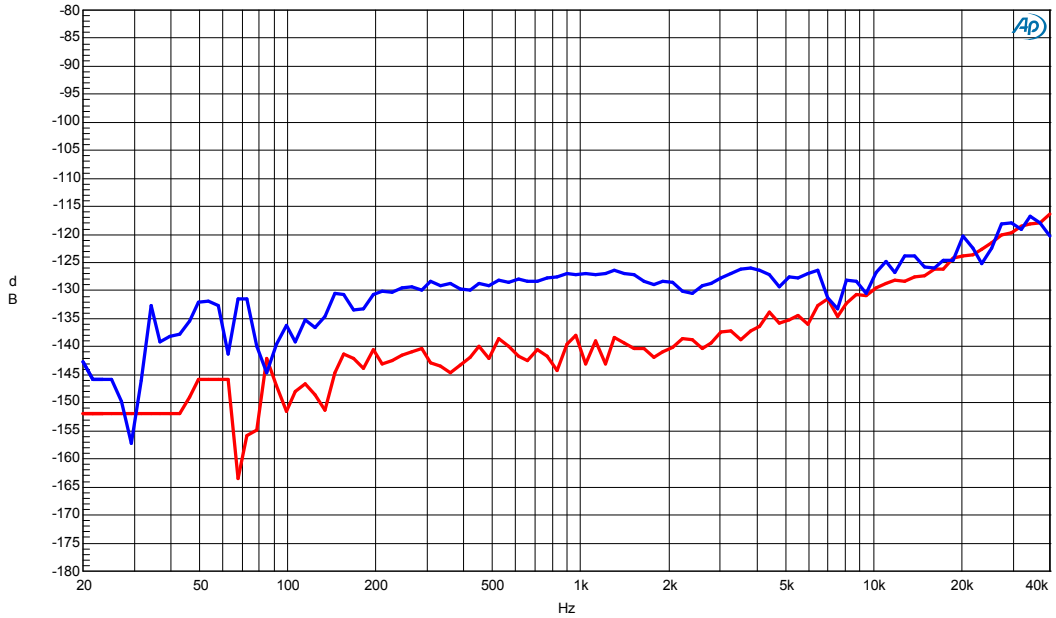

Figure 19. Crosstalk

fs = 192 kHz
AK5397 FFT (-1dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, fin=1kHz

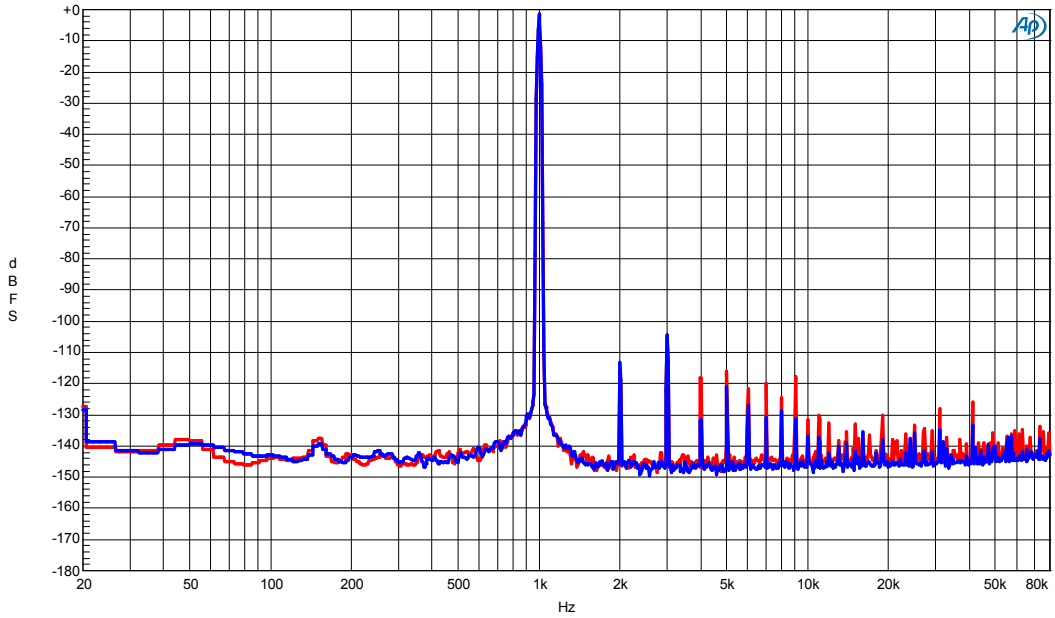

Figure 20. FFT (-1dBFS Input)

AK5397 FFT (-60dBFS Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, fin=1kHz

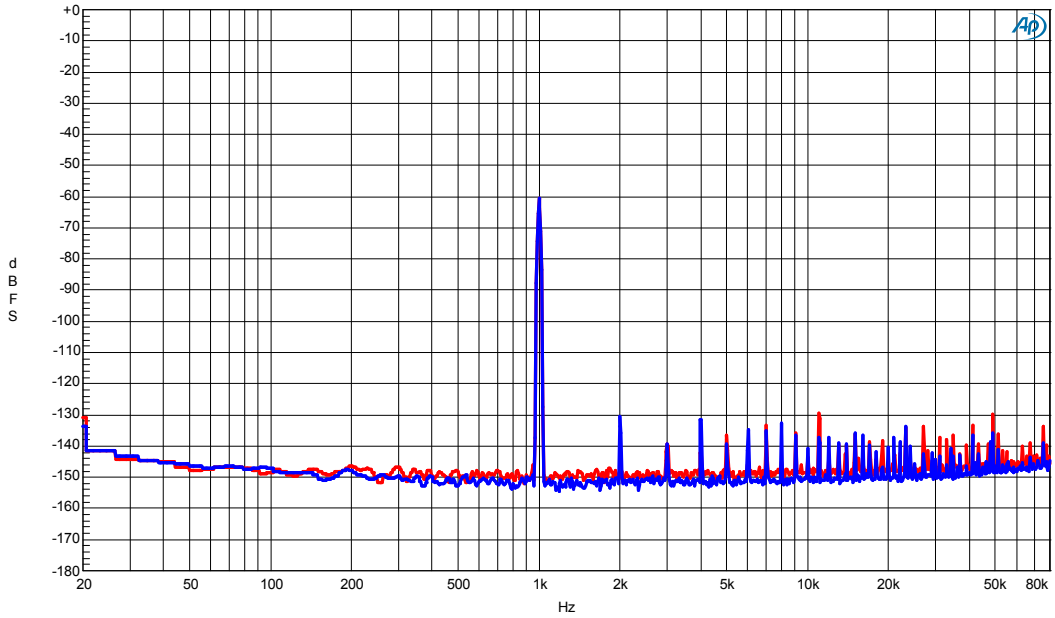

Figure 21. FFT (-60dBFS Input)

fs =192 kHz
AK5397 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, fin=1kHz

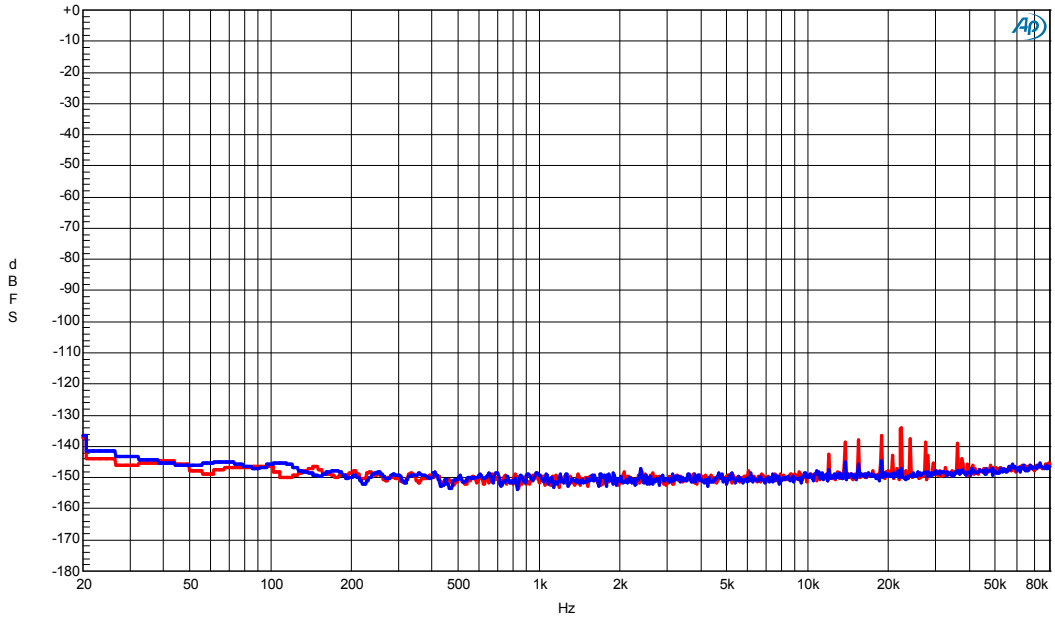

Figure 22. FFT (No Signal Input)

AK5397 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, fin=1kHz

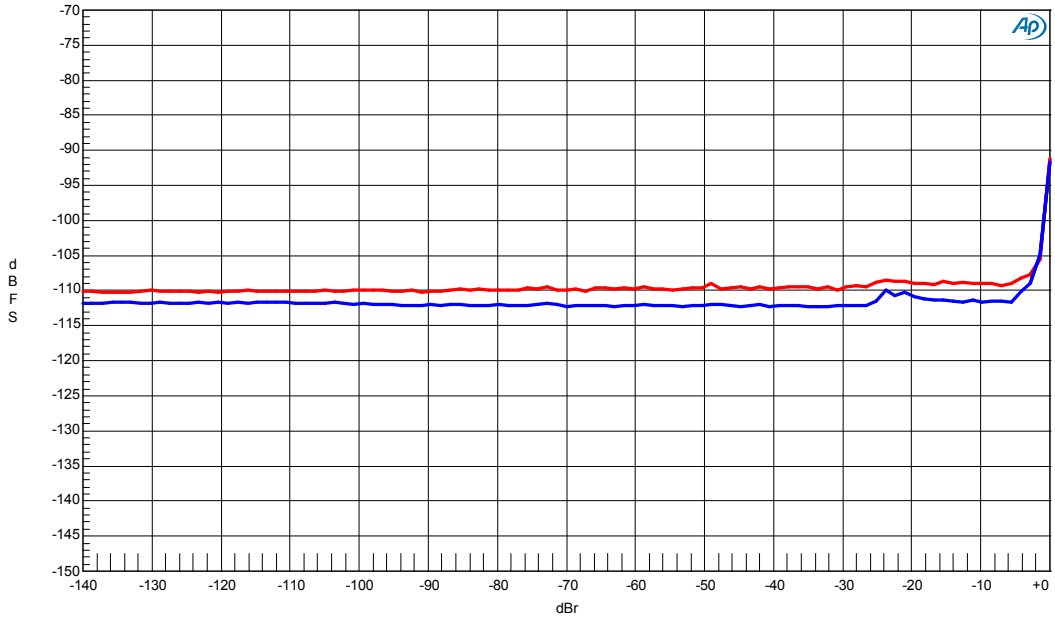

Figure 23. THD+N vs. Input Level

fs = 192 kHz
AK5397 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, -1dBFS Input

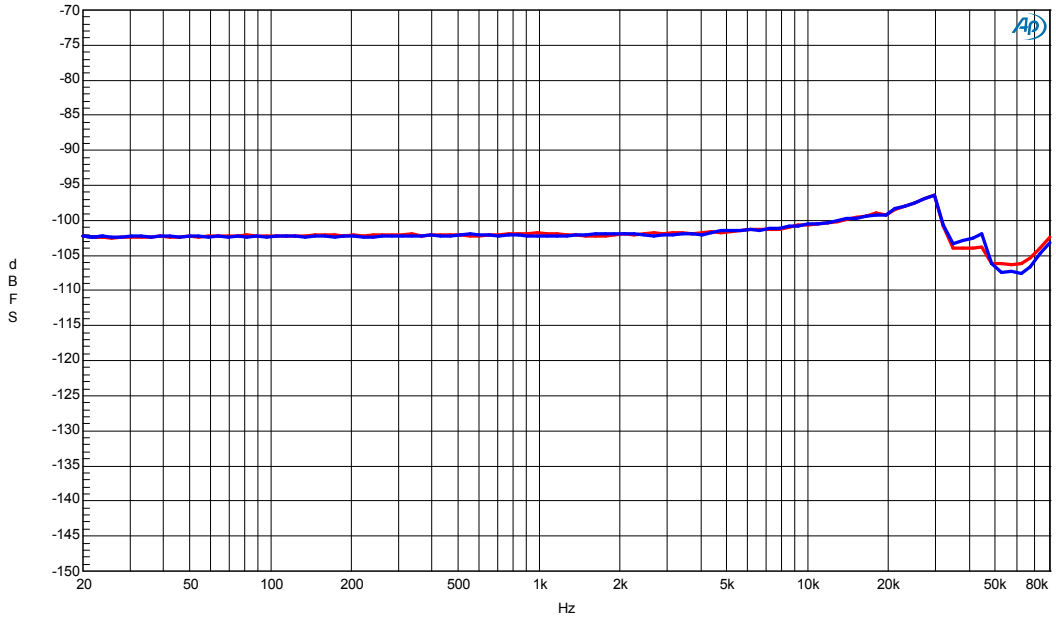

Figure 24. THD+N vs. Input Frequency

AK5397 Linearity
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, fin=1kHz

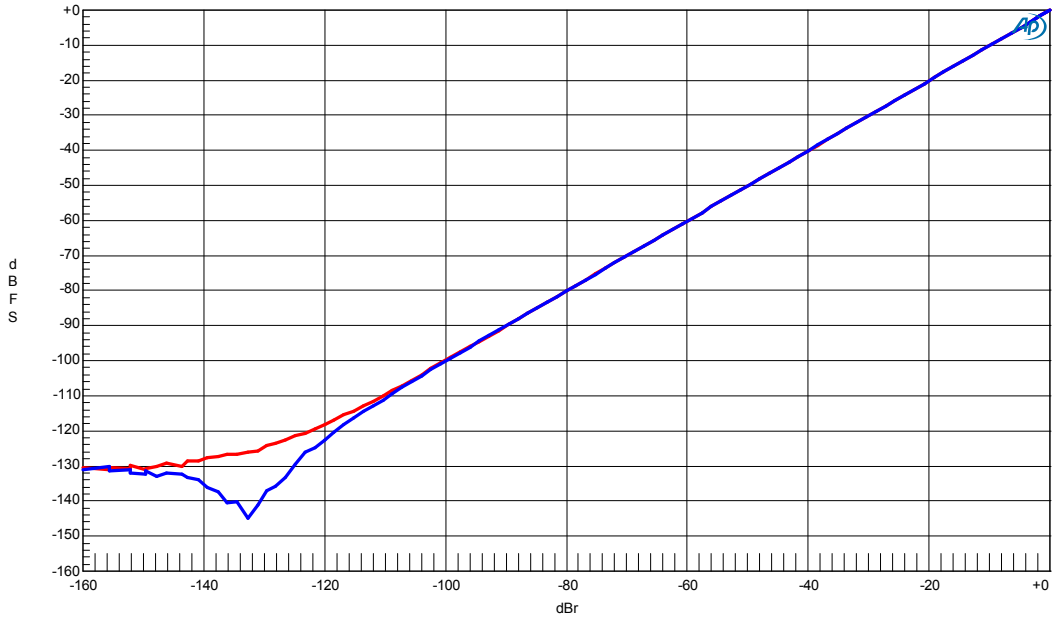

Figure 25. Linearity

fs = 192 kHz
AK5397 Frequency Response
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, -1dBFS Input

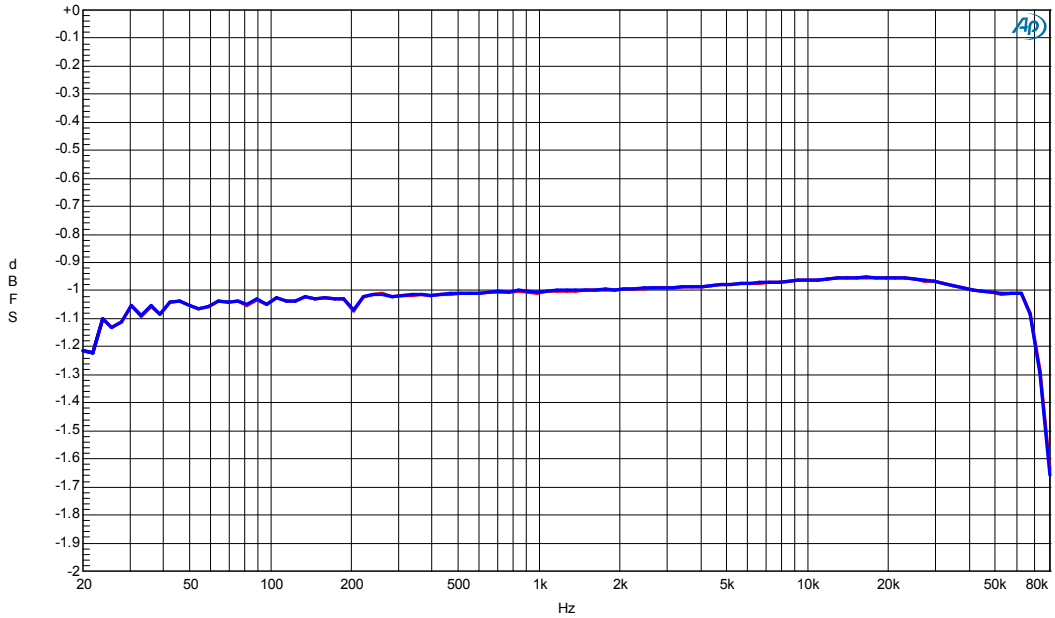

Figure 26. Frequency Response

AK5397 Crosstalk
AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=128fs, -1dBFS Input

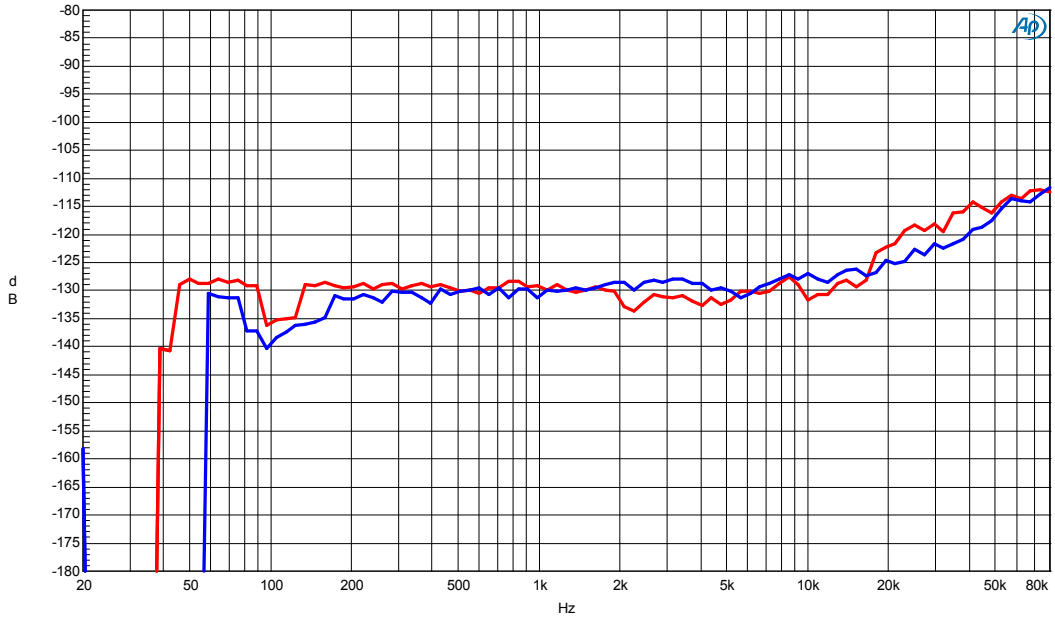

Figure 27. Crosstalk

REVISION HISTORY

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
15/06/01	KM120900	0	First edition	-	

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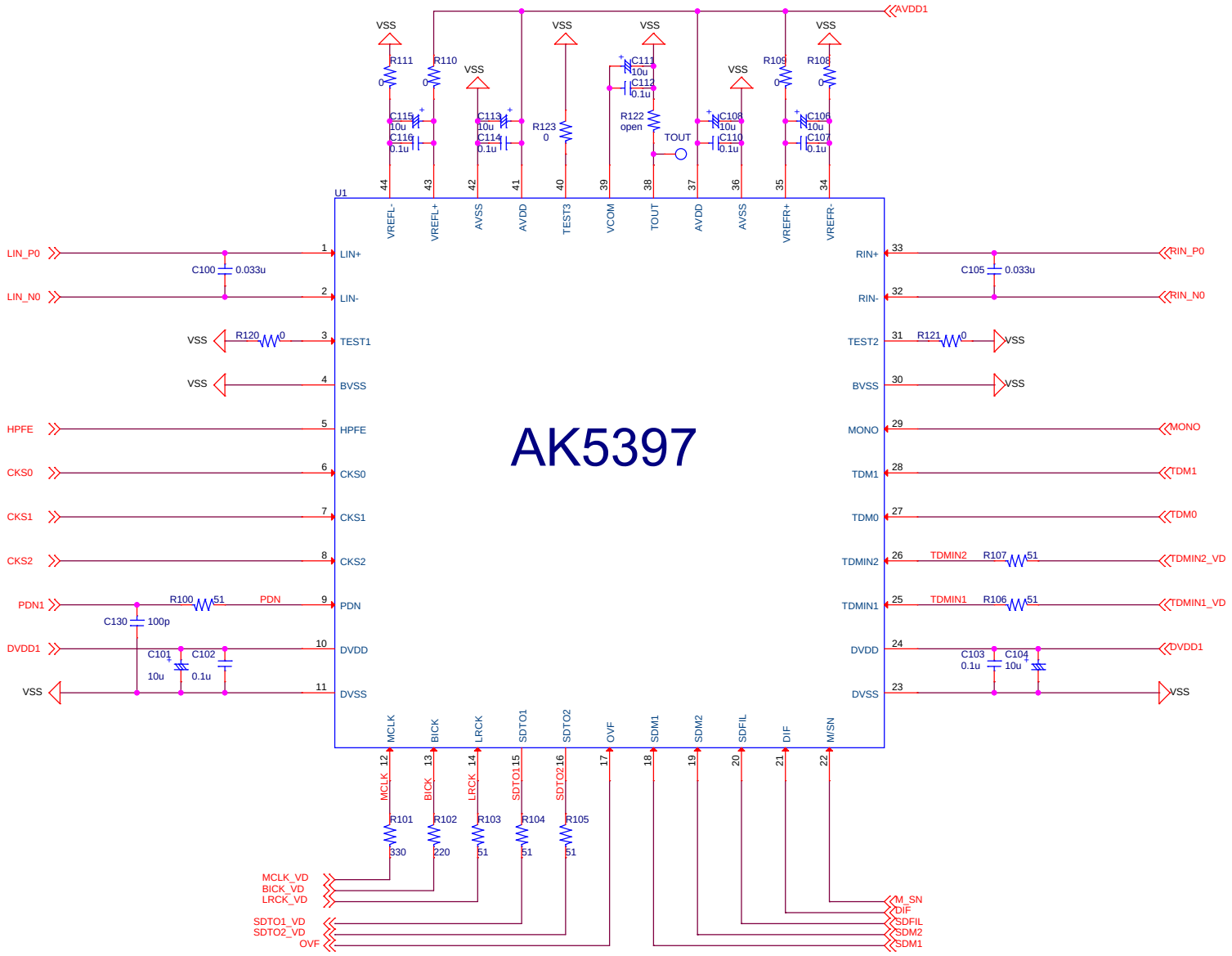

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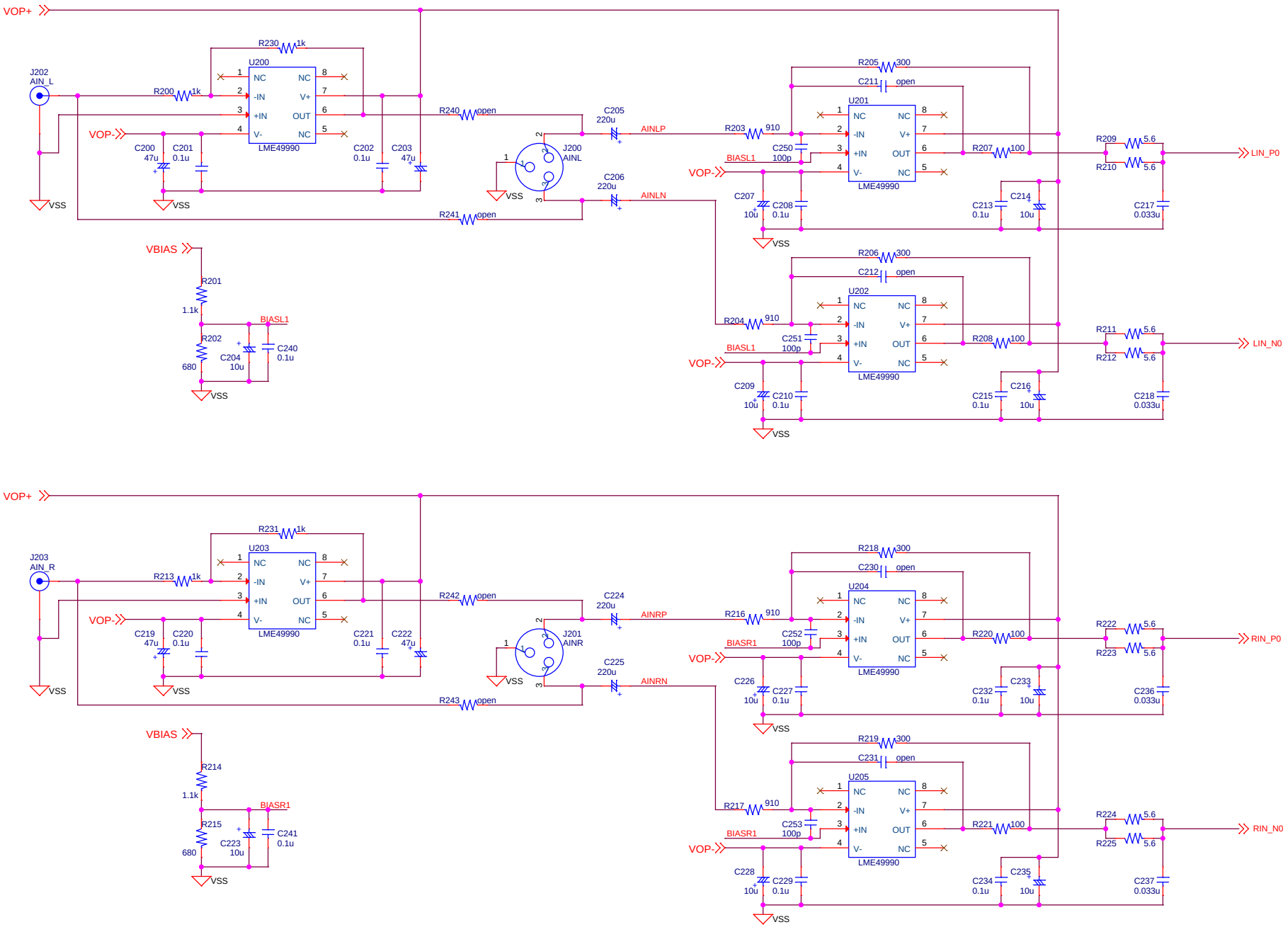

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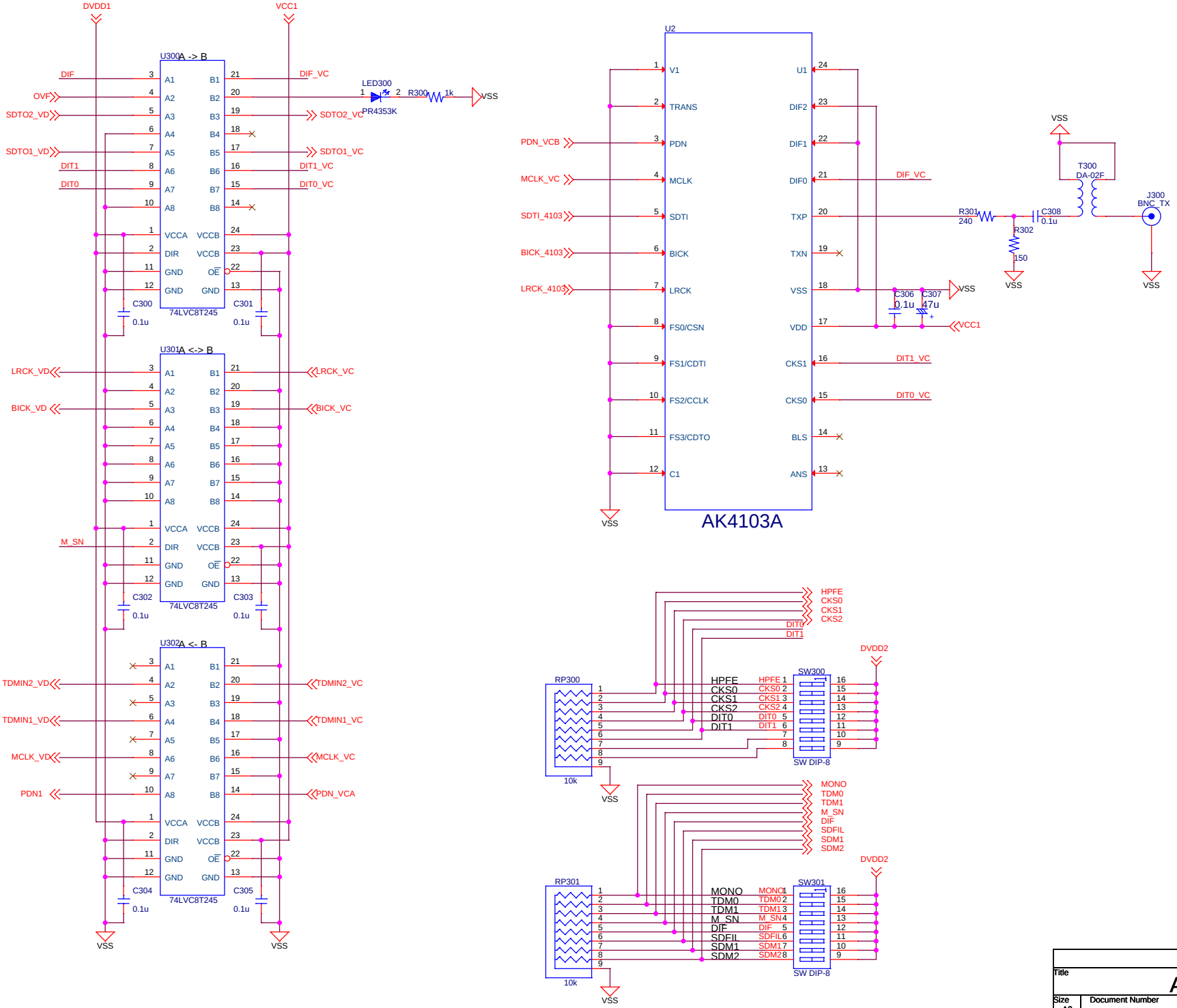

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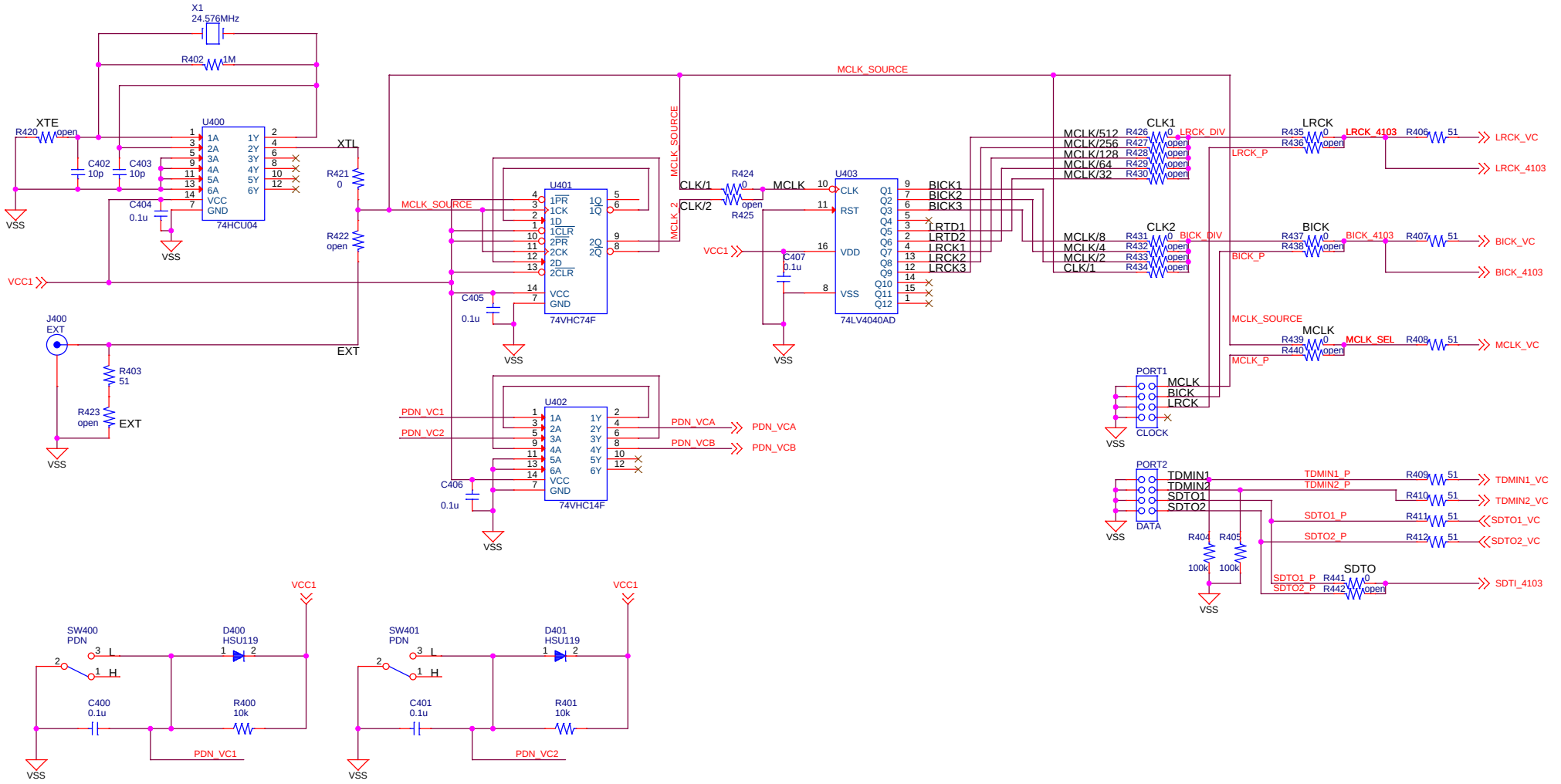

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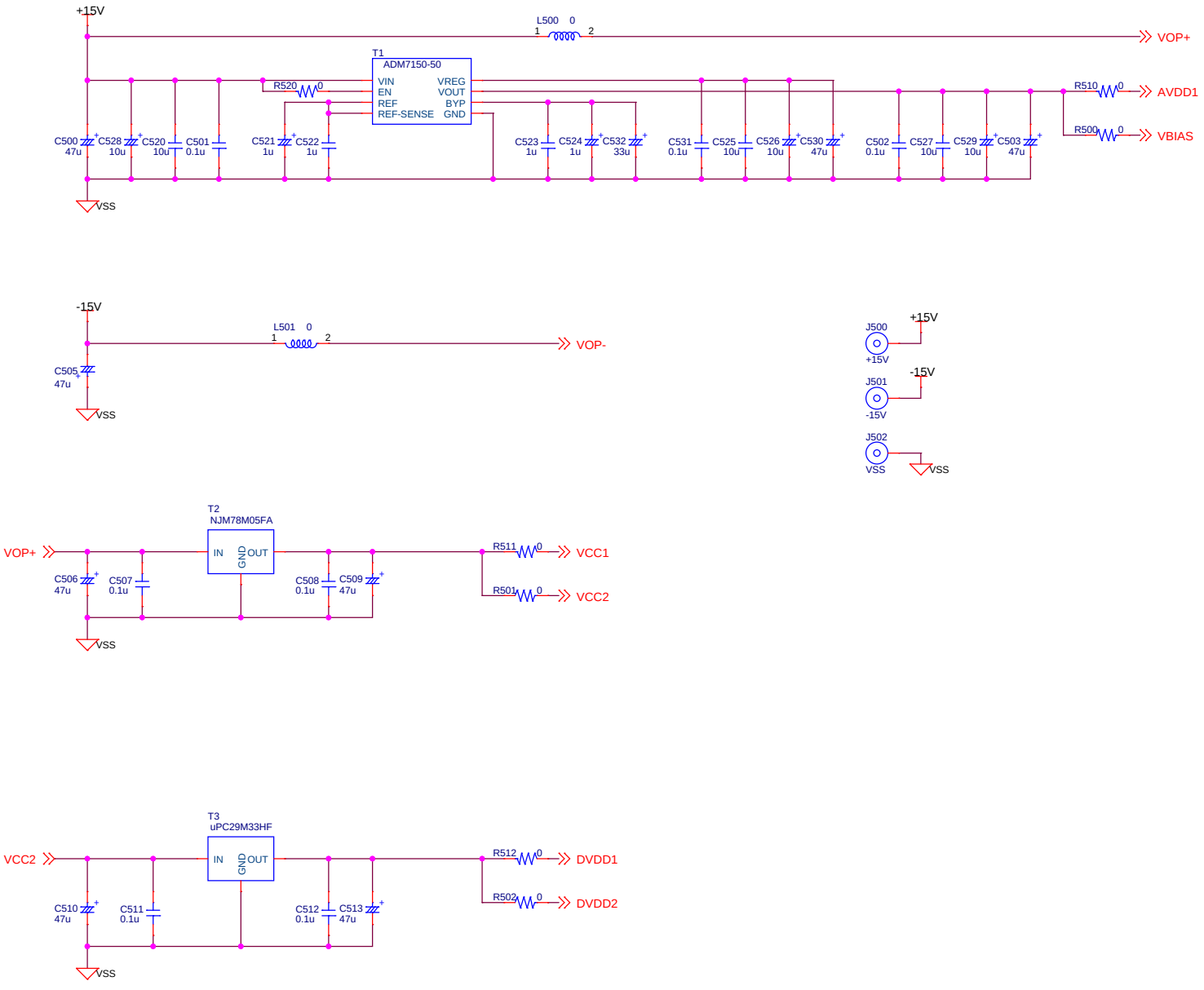

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