



Evaluation Board for AK8133

AKD8133

Description

The AKD8133 is an evaluation board for AK8133 clock generator. Therefore, it is easy to evaluate the jitters and XO performance.

4 types of boards are prepared depending on crystal foot pattern.

Ordering guide

■ AKD8133_X

X: Crystal type

N: Non Crystal

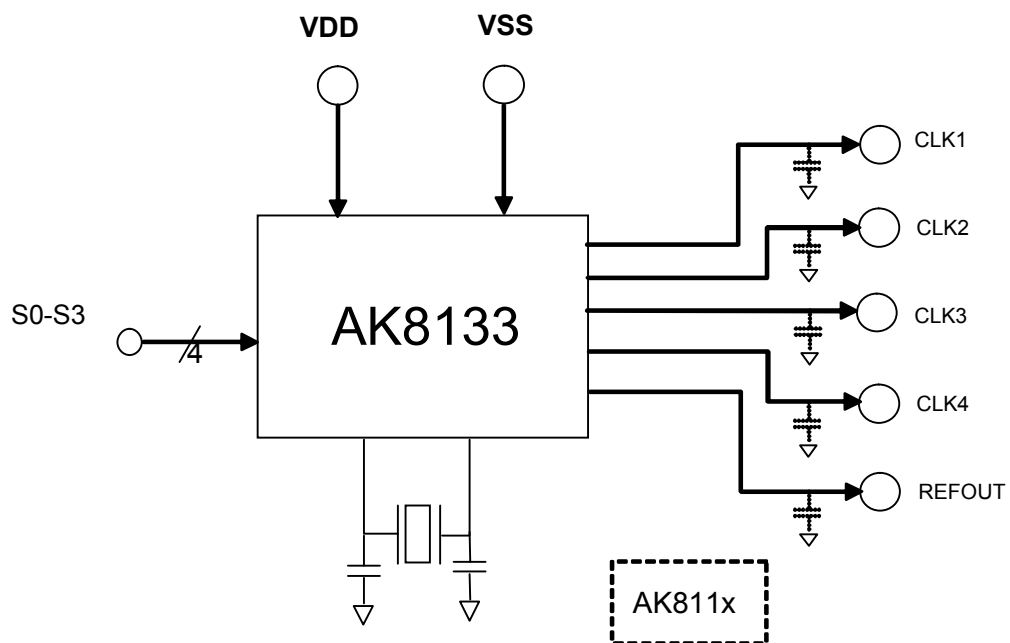
A: 49 Surface mount type

B: 5032 2 terminal

C: 3225 2 terminal

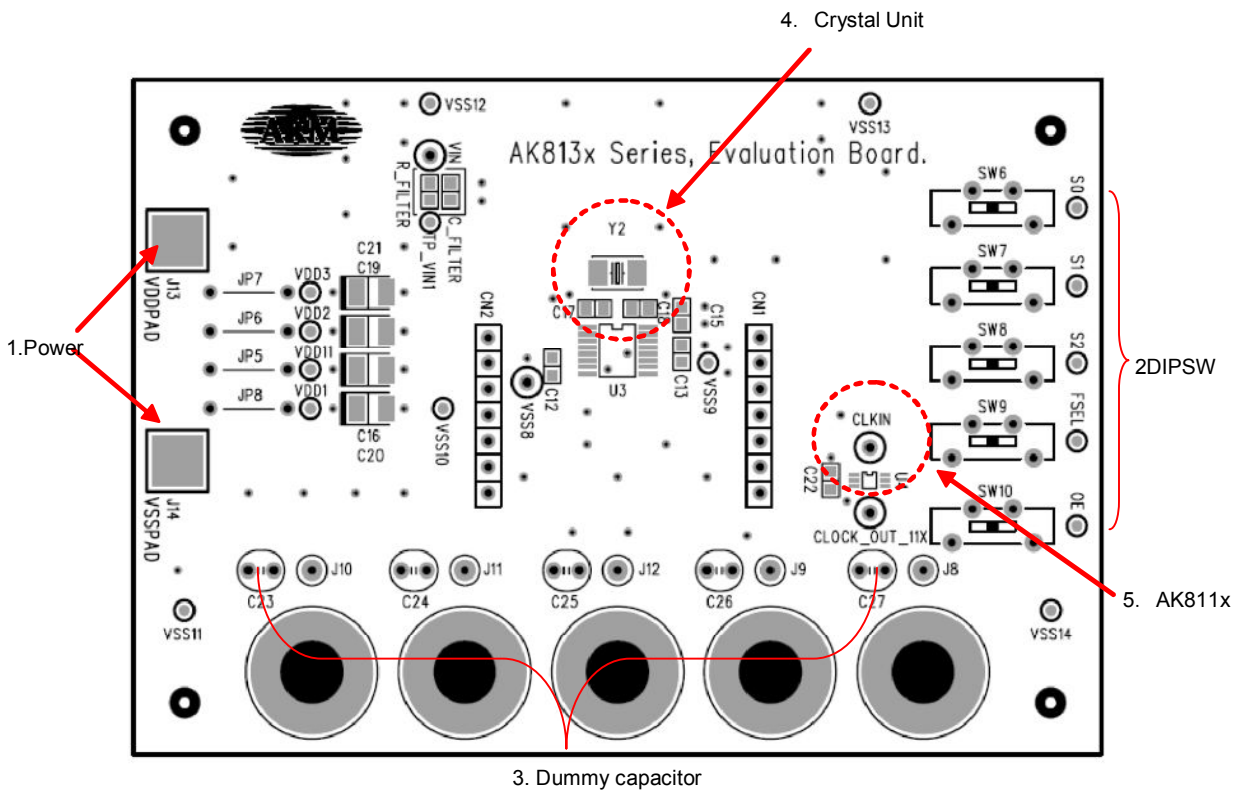
D: 3225 4 terminal

Block Diagram



AK8133 Evaluation Board

Functions



1. Power Supply

Please connect the lead line to VDDPAD (3V) and VSSPAD (GND).

2. DIPSW Setting

DISPSW6-10 are connected to the mode setting pins of AK8133 and AK811x. If these pins are controlled with general-purpose port, microprocessor or other methods, please keep these pins "open".

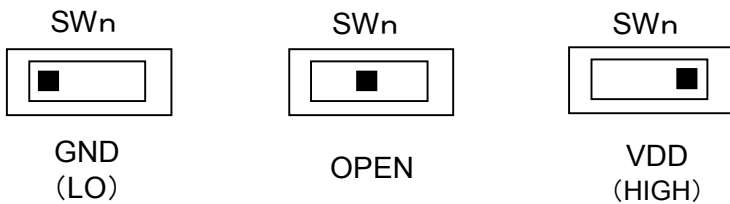


Table2.1 Dip Switch Connection

SW	Connect to:
SW6	AK8133 Pin2(S0)
SW7	AK8133 Pin3(S1)
SW8	AK8133 Pin14(S3)
SW9	AK811x Pin5
SW10	AK8133 Pin4(S2)

Table2.2 CLK1 Output Frequency

Selection Pin SW8 (S3/Pin14)	Output Frequency(MHz) J10 (CLK1/Pin 7)
L	36.864
H	24.576

Table2.3 CLK2-4 Clock output Frequency

Sampling Frequency (kHz)	Selection Pin			Clock Output Frequency (MHz)		
	SW10 (S2/Pin 4)	SW7 (S1/Pin3)	SW6 (S0/Pin 2)	J11 256fs (CLK2/Pin 8)	J9 384fs (CLK3/Pin10)	J8 (CLK4/Pin11)
48.0	L	L	L	12.288	18.432	33.8688
44.1	L	L	H	11.2896	16.9344	33.8688
32.0	L	H	L	8.192	12.288	33.8688
192.0	L	H	H	49.152	73.728	33.8688
88.2	H	L	L	22.5792	33.8688	33.8688
96.0	H	L	H	24.576	36.864	33.8688
64.0	H	H	L	16.384	24.576	33.8688
16.0/22.05	H	H	H	4.096	8.4672	16.9344

3. Dummy capacitor loads

There are several dummy capacitor loads, C23 through C27. It is useful to measure clock performance or current consumption by loading capacitor which is virtually assumed in the system. It is important to take line capacitance into account and it is approximately 5pF. Consequently if there is 25pF capacitance assumed in the system, another 20pF capacitor needs to be mounted. Each clock outputs from AK8133 lead to J8 through J12. Chassis mount test jacks for miniature probe (Tektronix 131-0258-00) are available by mounting there.

Table1.2

Jn/Cn	Connect to:
J8/C8	AK8133 Pin11
J9/C9	AK8133 Pin10
J10/C10	AK8133 Pin7
J11/C11	AK8133 Pin8
J12/C12	AK8133 Pin9

4. Quartz oscillator foot pattern

There are 4 types of boards depending on quartz oscillator. C17 and C18 are the load capacitance for crystal unit. In case of external clock input, please remove these capacitors.

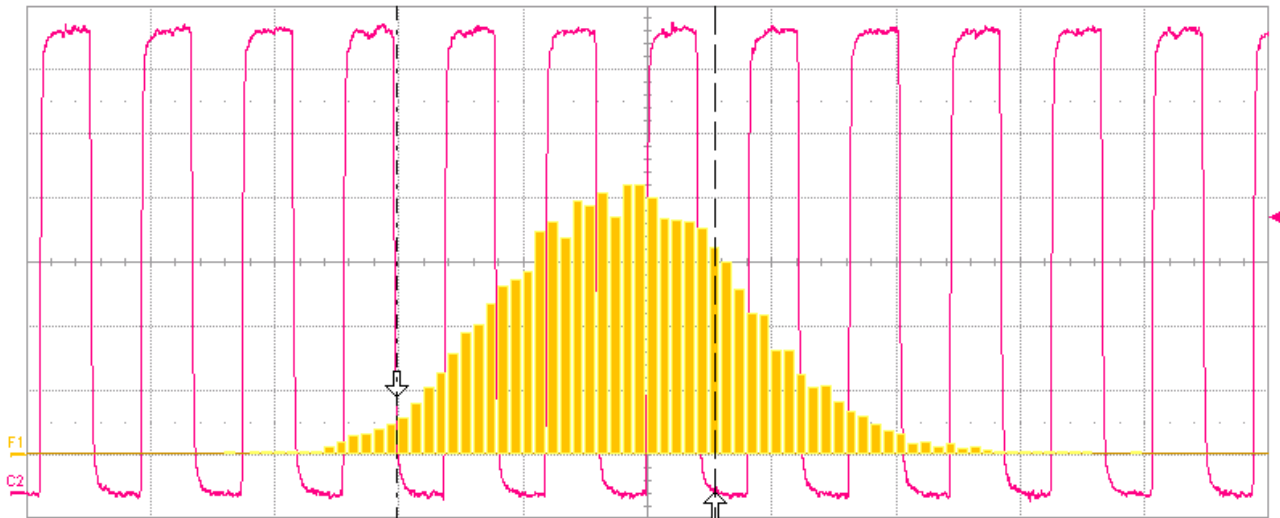
5. AK811x foot pattern

It is possible to mount AK811x series 1ch-PLL on this board.

Jitter measurement

Device:AK8133E

Condition: S2/S1/S0=HHH, Dummy capacitor=0pF



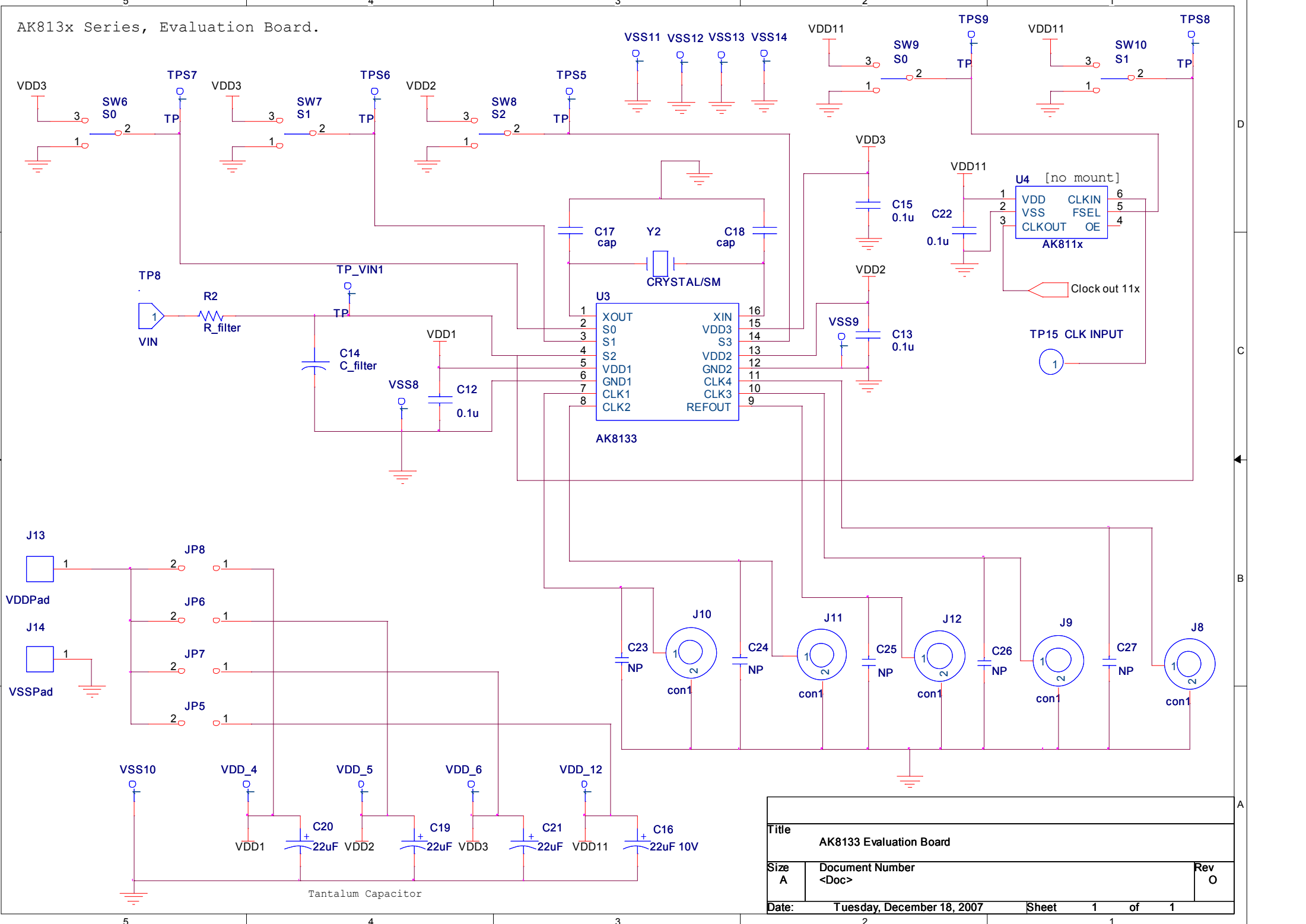
Measure	P1:freq(C2)	P2:per@lv(C2)	P3:duty@lv(C2)	P4:dper@lv(C2)	P5:TIE@lv(C2)	P6:max(C2)	P7:min(C2)	P8:mean(C2)
value	24.5654 MHz	40.708 ns	49.99 %	11 ps	28 ps	3.28 V	-50 mV	1.614 V
mean	24.576202 MHz	40.68977 ns	49.9814 %	-1 fs	6.46 ps	3.2660 V	-37.0 mV	1.61353 V
min	24.5517 MHz	40.658 ns	49.90 %	-60 ps	-79 ps	3.25 V	-57 mV	1.605 V
max	24.5956 MHz	40.730 ns	50.07 %	52 ps	99 ps	3.30 V	-22 mV	1.621 V
sdev	5.769 kHz	9.55 ps	20.8 m%	14.87 ps	18.54 ps	7.9 mV	5.1 mV	2.51 mV
num	13.812e+3	13.812e+3	13.812e+3	12.661e+3	14.963e+3	1.151e+3	1.151e+3	1.151e+3
status		✓	✓	✓	✓	✓	✓	✓

C2	DC
445 mV/div	
-1.610 V ofst	
↓ 680 mV	
↑ 0.00 V	

F1	hist(P2)
100 #/div	
10.0 ps/div	
10.006 k#	
↓ ---	
↑ ---	

Timebase	0 ns	Trigger	C2
50.0 ns/div		Stop	1.909 V
10.0 kS	20 GS/s	Edge	Positive
X1=	-101.2000 ns	ΔX=	128.2768 ns
X2=	27.0768 ns	1/ΔX=	7.795642 MHz

AK813x Series, Evaluation Board.



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AK8133 Evaluation Board		
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