



Evaluation Board for AK8136A

AKD8136A

Description

The AKD8136A is an evaluation board for AK8136A clock generator. Therefore, it is easy to evaluate the jitters and VCXO performance.

Ordering guide

- AKD8136A

Block Diagram

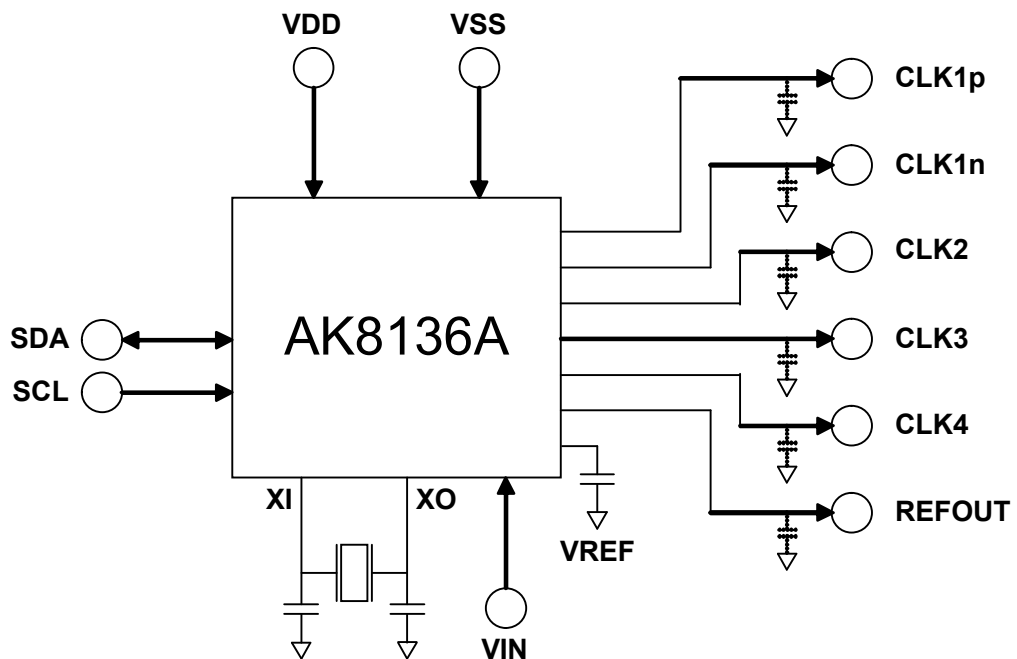


Figure 1. AK8136A Evaluation Board

Functions

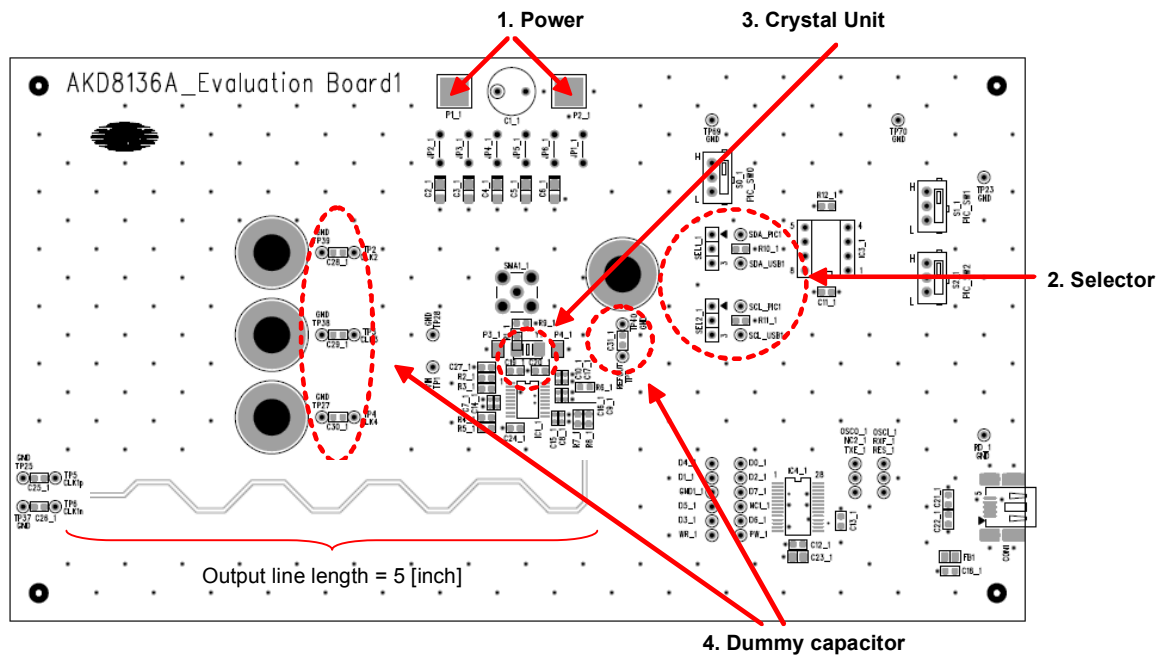


Figure 2. AKD8136A_A top view

1. Power Supply

Please connect the lead line to P1 (3.3V : TYP) and P2 (GND).

2. Selector Setting

Selector 1-2 are connected to the serial interface pins of AK8136A.

If these pins are controlled with USB interface, please keep these selectors “SDA_USB” and “SCL_USB” respectively.

Table 1. Selector Connection

Selector	Connect to:
SEL1	AK8136A Pin15 (SDA)
SEL2	AK8136A Pin16 (SCL)

3. Quartz oscillator foot pattern

C19 and C20 are the load capacitance for crystal unit. In case of external clock input, please remove these capacitors.

4. Dummy capacitor loads

There are several dummy capacitor loads, C28 through C31. It is useful to measure clock performance or current consumption by loading capacitor which is virtually assumed in the system. It is important to take line capacitance into account and it is approximately 5pF. Consequently if there is 15pF capacitance assumed in the system, another 10pF capacitor needs to be mounted. Each clock outputs from AK8136A lead to TP2, TP3, TP4 and TP7. Chassis mount test jacks for miniature probe (Tektronix 131-0258-00) are available by mounting there.

Table 2. Dummy capacitor Connection

TPn/Cn	Connect to:
TP2/C28	AK8136A Pin5 (CLK2)
TP3/C29	AK8136A Pin8 (CLK3)
TP4/C30	AK8136A Pin9 (CLK4)
TP7/C31	AK8136A Pin18 (REFOUT)

Jitter measurement

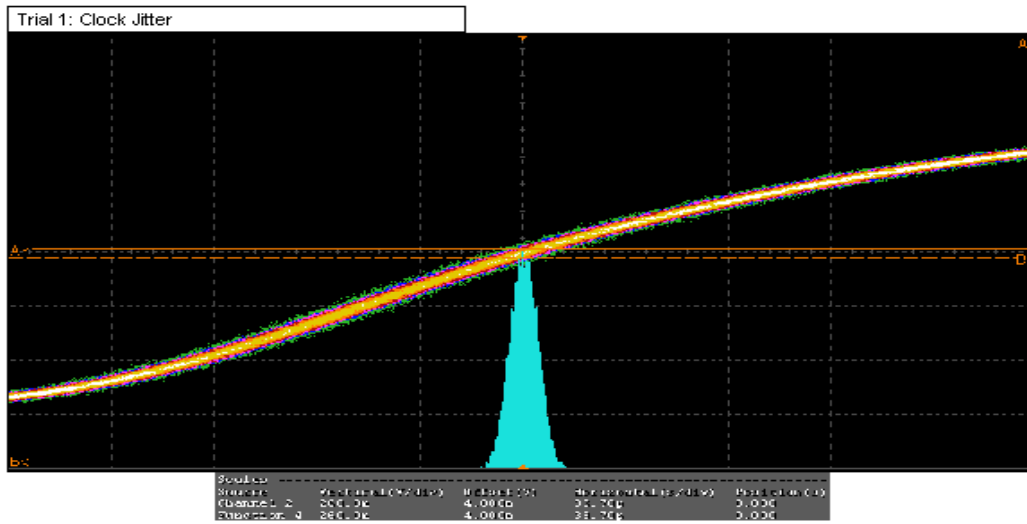
Device:AK8136A

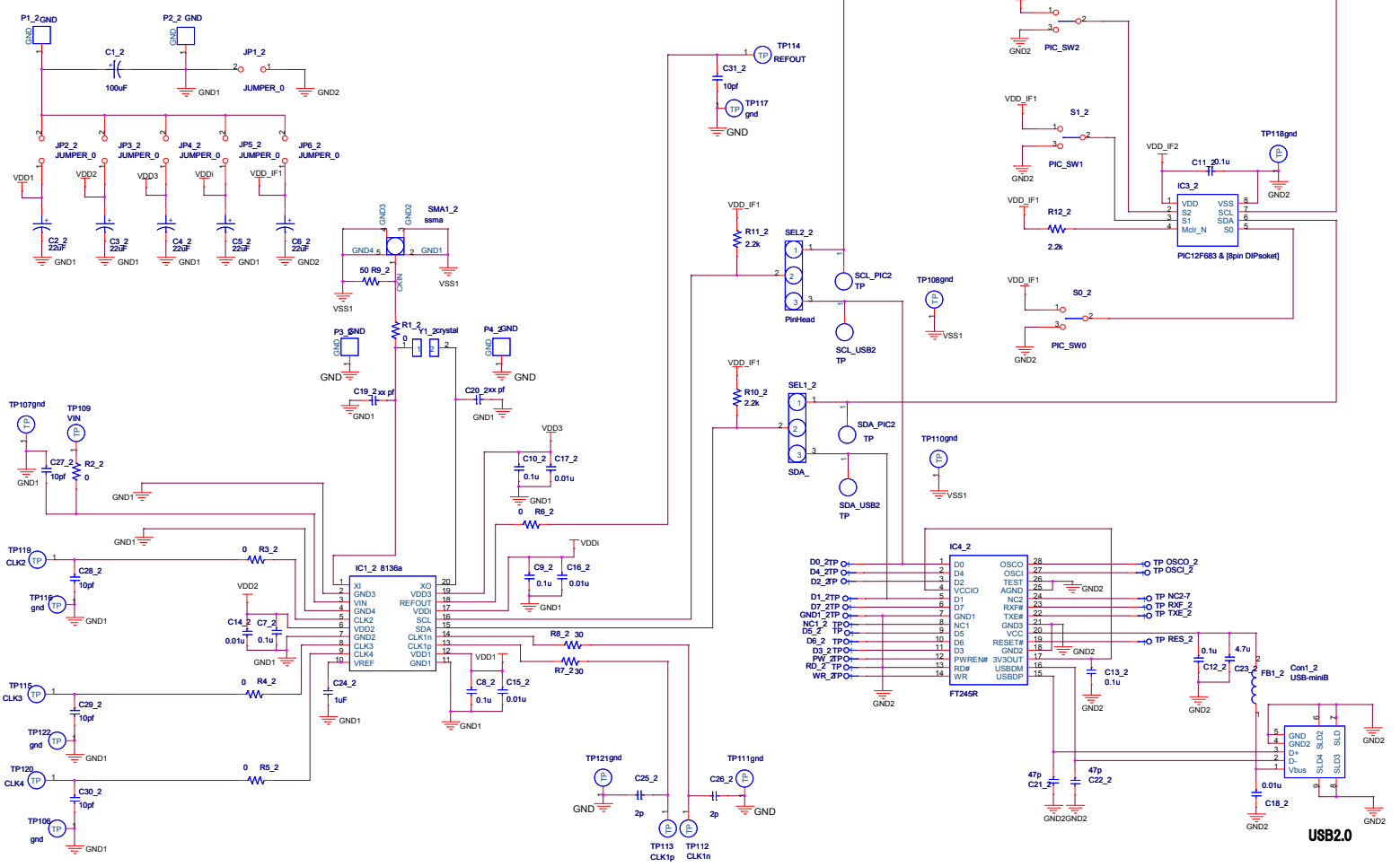
✓ 7-9: Clock Jitter
 Test Summary: Pass | Test Description: | 2 Channels Connection Model: TMD5 differential clock jitter must not exceed 0.25*Tbit, re
 Test Limits: <= 250mTbit | Clock Jitter (Worst of 10 Trials) 56mTbit | # Trials Run: 10 | Worst Trial: T

Overall Summary + details of worst 10 trials

	Actual Value	Margin	Test Frequency(MHz)	# Edges	Tbit(ps)	Clock Jitter(ps)
<i>Avg</i>	52.87mTbit	78.88%				
<i>StdDev</i>	2.365mTbit	957.8m%				
<i>Range</i>	7.224mTbit	2.800%				
<i>Min</i>	48.93mTbit	77.60%				
<i>Max</i>	56.16mTbit	80.40%				
<i>Sum</i>	528.7mTbit	788.8%				
✓ Trial 1	52mTbit	79.2%	148.477	16.00000M	673.506	35.200
✓ Trial 2	54mTbit	78.4%	148.490	16.00000M	673.448	36.320
✓ Trial 3	52mTbit	79.2%	148.464	16.00000M	673.566	34.820
✓ Trial 4	55mTbit	78.0%	148.475	16.00000M	673.515	37.070
✓ Trial 5	49mTbit	80.4%	148.474	16.00000M	673.518	33.330
✓ Trial 6	53mTbit	78.8%	148.482	16.00000M	673.484	35.570
✓ Trial 7	49mTbit	80.4%	148.502	16.00000M	673.394	32.950
✓ Trial 8 (Worst)	56mTbit	77.6%	148.480	16.00000M	673.492	37.820
✓ Trial 9	55mTbit	78.0%	148.492	16.00000M	673.437	37.070
✓ Trial 10	53mTbit	78.8%	148.477	16.00000M	673.506	35.950

Clock Jitter





File	AKD8136A_Evaluation Board2.		
Size	Document Number		Rev
A3	<Doc>		<Rev>
Date:	Tuesday, January 13, 2009	Sheet	1 of 1