# Evaluation Board for AK8137A
# AKD8137A

## Description

The AKD8137A is an evaluation board for AK8137A clock generator. Therefore, it is easy to evaluate the jitters and VCXO performance.
2 types of boards are prepared depending on foot pattern of output load for SATA_Cp/Cn, USB_Cp/Cn and CPU_Cp/Cn pins.

## Ordering guide

- AKD8137A_X

  X: Output Load Condition for SATA_Cp/Cn, USB_Cp/Cn and CPU_Cp/Cn pins
  A: Output line length = 5 [inch]
  B: Output line length = 1 [inch]

## Block Diagram

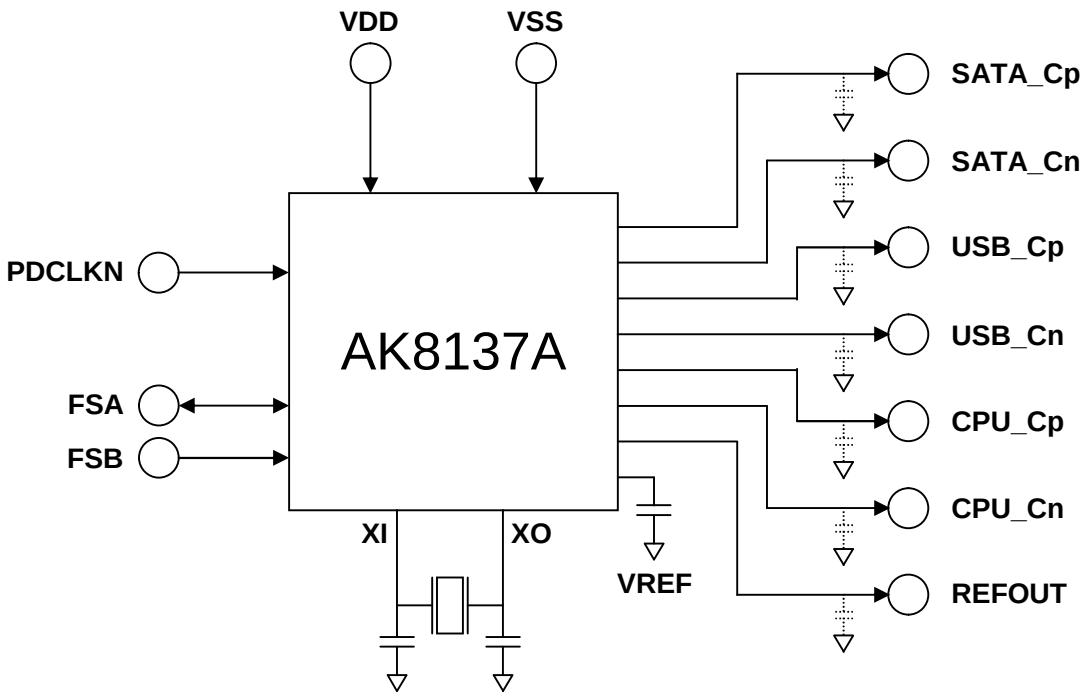



**Figure 1. AK8137A Evaluation Board**

## Functions

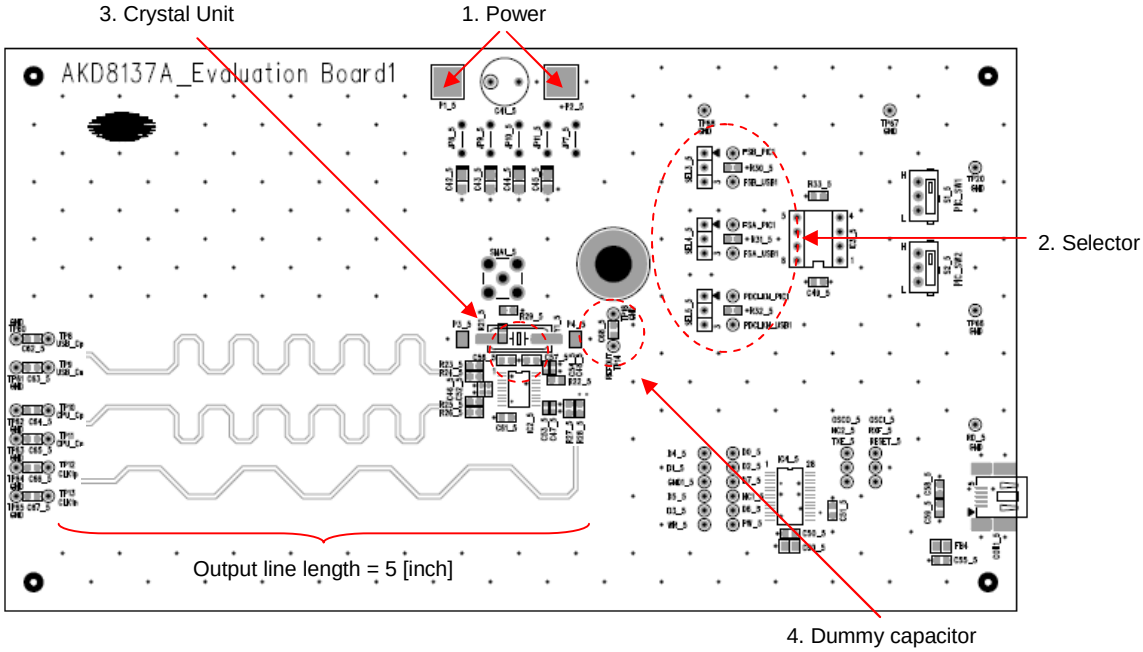



**Figure 2. AKD8137A_A top view**

### 1. Power Supply

Please connect the lead line to P1 (3.3V : TYP) and P2 (GND).

### 2. Selector Setting

Selector 3-5 are connected to FSA, FSB and PDCLKN pins of AK8137A.
If these pins are controlled with USB interface, please keep these selectors “SDA_USB” and “SCL_USB” respectively.

**Table 1. Selector Connection**

| Selector | Connect to: |
|---|---|
| SEL3 | AK8137A Pin9 (FSB) |
| SEL4 | AK8137A Pin15 (FSA) |
| SEL5 | AK8137A Pin16 (PDCLKN) |

### 3. Quartz oscillator foot pattern

C56 and C57 are the load capacitance for crystal unit. In case of external clock input, please remove these capacitors.

## 4. Dummy capacitor loads

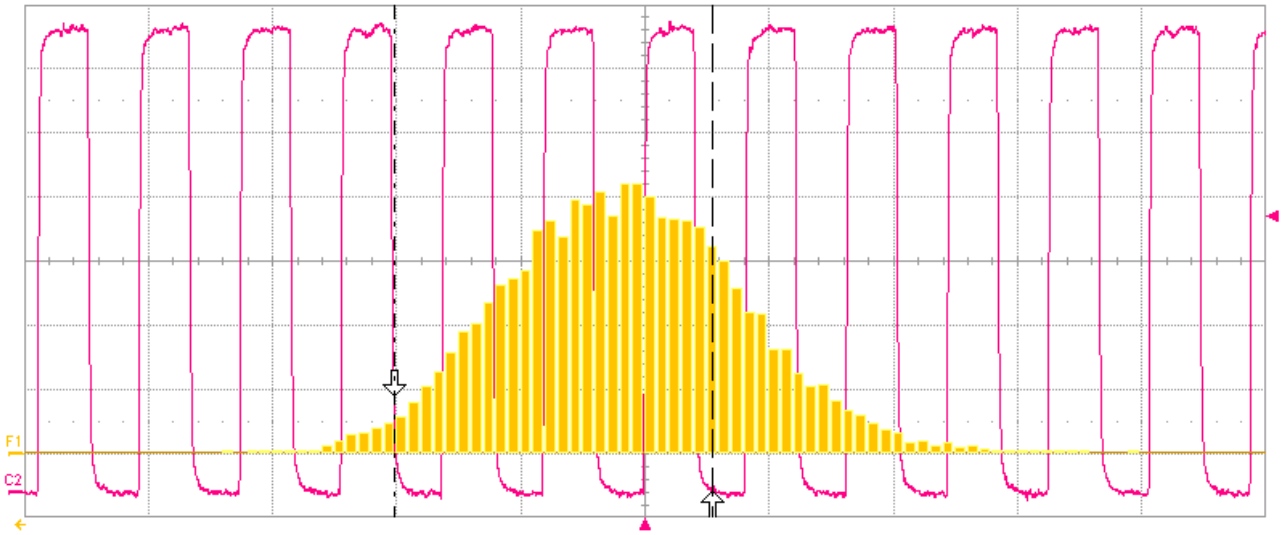
There is a dummy capacitor load, C68. It is useful to measure clock performance or current consumption by loading capacitor which is virtually assumed in the system. It is important to take line capacitance into account and it is approximately 5pF. Consequently if there is 25pF capacitance assumed in the system, another 20pF capacitor needs to be mounted. Each clock outputs from AK8137A lead to TP14. A Chassis mount test jack for miniature probe (Tektronix 131-0258-00) is available by mounting there.

**Table 2. Dummy capacitor Connection**

| TPn/Cn | Connect to: |
|---|---|
| TP14/C68 | AK8137A Pin18 (REFOUT) |

## Jitter measurement

Device:AK8137A
Condition: S2/S1/S0=HHH, Dummy capacitor=0pF




| Measure | P1:freq(C2) | P2:per@lv(C2) | P3:duty@lv(C2) | P4:dper@lv(C2) | P5:TIE@lv(C2) | P6:max(C2) | P7:min(C2) | P8:mean(C2) |
|---|---|---|---|---|---|---|---|---|
| value | 24.5654 MHz | 40.708 ns | 49.99 % | 11 ps | 28 ps | 3.28 V | -50 mV | 1.614 V |
| mean | 24.576202 MHz | 40.68977 ns | 49.9814 % | -1 fs | 6.46 ps | 3.2660 V | -37.0 mV | 1.61353 V |
| min | 24.5517 MHz | 40.658 ns | 49.90 % | -60 ps | -79 ps | 3.25 V | -57 mV | 1.605 V |
| max | 24.5956 MHz | 40.730 ns | 50.07 % | 52 ps | 99 ps | 3.30 V | -22 mV | 1.621 V |
| sdev | 5.769 kHz | 9.55 ps | 20.8 m% | 14.87 ps | 18.54 ps | 7.9 mV | 5.1 mV | 2.51 mV |
| num | 13.812e+3 | 13.812e+3 | 13.812e+3 | 12.661e+3 | 14.963e+3 | 1.151e+3 | 1.151e+3 | 1.151e+3 |
| status | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |