AK8464

3ch input 10bit 35MSPS/ch AFE for MFP or CIS module with CCDI/F, TG, LVDS, LDO, Synth_PLL, and SSCG_PLL

1.General Description

The AK8464 is a 3-channel 10bit 35MSPS/Ch A/D convertor integrating TG, LVDS, LDO, Synth_PLL, SSCG_PLL and OSC circuits. The Timing Generator(TG) can generate CCD sensor driving pulse for linear CCD, CIS sensor driving pulse for CIS modules and LED control pulse. It is suitable for MFPs and CIS modules.

2.Features

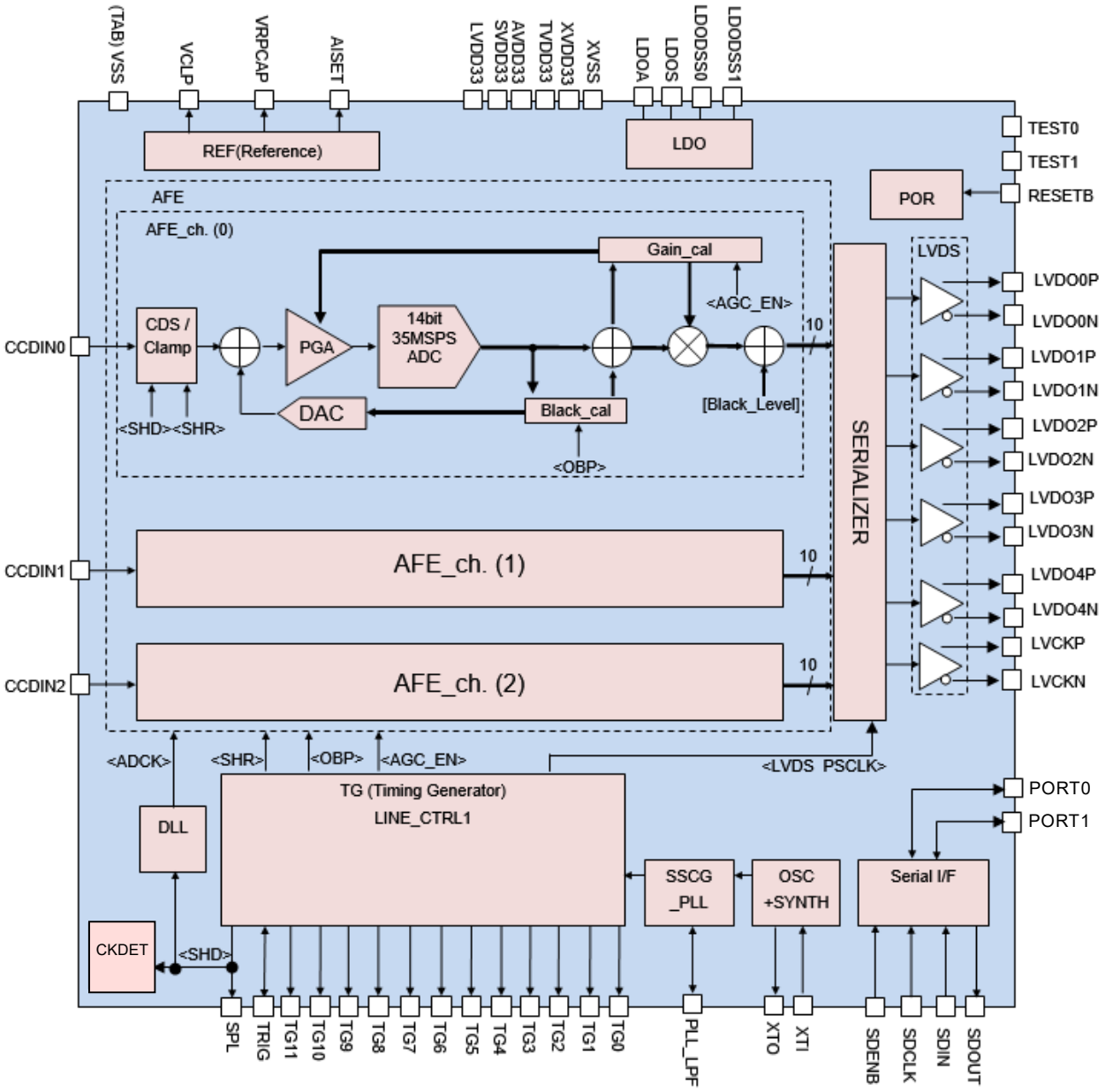
☐ Input Block	3Ch
☐ Sensor Type	CCD (Negative)/CMOS-CIS (Positive)
☐ CCDIN Input Range	1.05Vpp (min.) (CDS: bit clamp mode for CCD sensor)
	1.00Vpp (min.) (Line Clamp mode for CCD sensor)
	1.00Vpp (min.) (DC-direct mode for CMOS sensor)
☐ Reference Voltage Range of the Sensor	2.33V(typ.)@Output (CDS or Clamp for CCD)
	0.55 ~ 1.15V@input (DC-direct for CMOS)
	0.7 ~ 1.1V(typ.)@Output: 2bit setting (for CMOS sensor)
☐ ADC Maximum Conversion Speed	35MSPS/Ch
☐ ADC Resolution:	10bit Output/14bit Internal (Straight Binary Code)
☐ ADC Linearity	No Missing Code @12bit accuracy
☐ Gain Adjustment Range	Analog: 0, 6 dB @1bit
	Digital: 1 ~ 3.98V/V @ 8bit
☐ Offset Compensation Range:	Analog: ±381mV min. @ 5bit
	Digital: ±127.75LSB @ 10bit
☐ Sensor Offset Compensation Range:	±200mV (except 50mV AFE internal offset)
☐ Automatic Black Level and White Level Correction Function for CCD	
☐ Pixel clock (<PCLK> signal)	8.75M ~ 35MHz
☐ Input clock (*XTI*)	10M ~ 25MHz (with Crystal Oscillator)
	8.75M ~ 35MHz (External clock input)
☐ Synth_PLL Multiplier	1 ~ 1.57 times
	@ 2.632% or 1.429% step (Input Frequency Ratio)
☐ Spread Spectrum clock input	Modulation Width: ±2% (max.)
	Modulation Frequency: 80kHz (max.)
	Center Frequency: 8.75M ~ 35MHz
☐ Spread Spectrum Clock Generator	Modulation Width: ±2.08% (max.)
	Modulation Frequency: 30k ~ 50kHz
	Center Frequency: 8.75M ~ 35MHz

☐ TG	Phase Resolution: 56 phases Maximum Pixel Rate: 35 MHz TG Output pin: 12 pins (*TG0-11* pin*s*) For CCD Pixel clock resolution pulse: Shift pulse: <SH0> ~ <SH6> Phase Adjustable clock: <P0>, <P1>, <P2>, <PRS>, <PCL> For CIS Pixel clock resolution pulse: <SP1>, <SP2>, <LED0> ~ <LED5>, <LED_EN> Phase Adjustable clock: <CISCK>
☐ LVDS Output Format:	5 Data Pairs, 1 clock pair (channel Link)
☐ CPU I/F:	4-wire Serial Interface
☐ Power Supply	3.0V-3.6V Single
☐ Power Consumption:	696mW (typ.)
☐ Operation Temperature:	0 ~ 85 ºC
☐ Package:	56-pin QFN (With TAB exposure, 0.4mm pitch, 7mm☐)

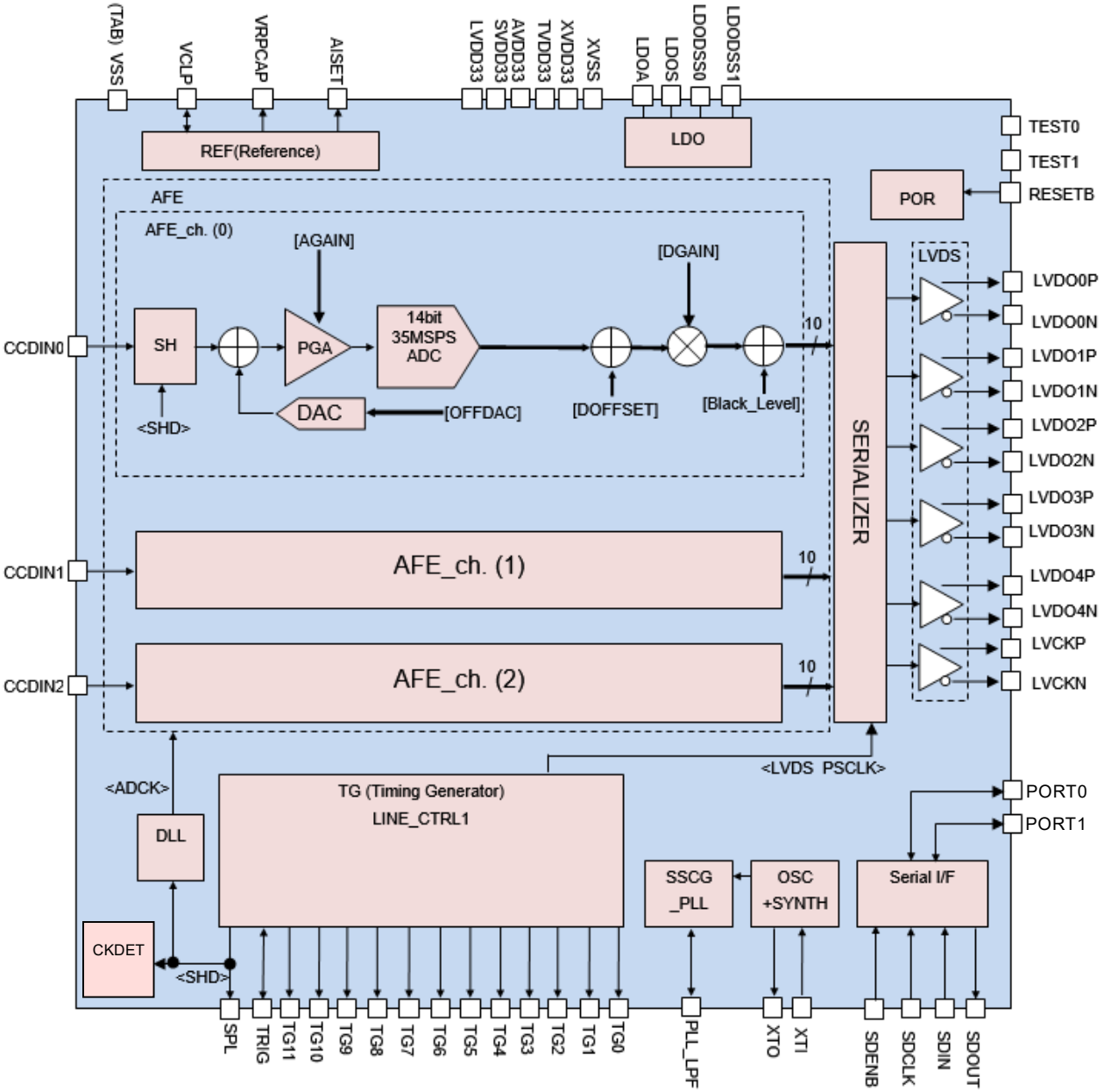
3.Table of Contents

4.Block Diagram

4.1. Block Diagram (Sensor mode: CCD)



4.2. Block Diagram (Sensor mode: CIS)



4.3. Block Functions

☐ REF(Reference): Reference Voltage Generation Circuit
This block generates sensoer referenve voltage, (*VCLP*), ADC reference voltage and internal reference current.

☐ CDS/Clamp/SH: Sensor Interface Circuit
This circuit samples pixel signal level of sensor ouput. Three modes are available for sampling: CDS mode, clamp mode and DC direct mode.

☐ DAC: D/A Converter for Adding Offset
Offset voltage that is added to the sampling signal at sensor interface is generated in this block. DAC setting range is more than ±381mV (min.) and the resolution is 25.4mV/step. Offset voltage can be set independently for each channel by register settings. Automatic offset compensation sequence is also available.

☐ PGA: Gain Adjustment Circuit
It is a programmable analog gain amplifier that can adjust signal amplitude for each channel. The gain setting range is 0dB or 6dB (typ.). Gain setting can be applied independently for each channel by register setting. Automatic gain adjustment sequence is also available.

☐ ADC: A/D Converter
It is a 14bit 35MSPS A/D converter that converts pixel signal to digital data after gain adjustment and offset compensation.

☐ Black_cal: Black Level Correction Circuit
Sampled black level during <OBP> period is automatically calibrated to the setting black level ([BLKLVL] register). This function is for CCD sonsors. Offset level should be set manually with CIS sensors.

☐ Gain_cal: Gain Correction Circuit
Sampled white level (peak value) during pixel detection period (<AGC_EN>) is automatically calibrated to the setting code ([WLVL]) by PGA and D-gain. This function is for CCD sensors. Gain level should be set manually for CIS sensors.

☐ Serializer
This block converts parallel data of ADC each channel output into serial data.

☐ LVDS: LVDS Interface Circuit
This block is output buffer that outputs ADC output in LVDS level. The output data consists of 5 data pairs and 1 clock pair.

☐ TG(Timing Generator), LINE_CTRL1: Timing Generation Circuit
This block generates sensor drive pulse and line control pulse from pixel cycle clock <PCLK>.

with CCD Sensor
Sensor drive pulses, <P0~2>, <PRS> and <PCL>, are generated based on <PCLK> clock.
Internal drive pulses, <SHD> and <SHR>, are generated based on <PCLK> clock.
Stop period of sensor drive pulse, vertical transmission period, <SH0> ~ <SH6> and general-purpose signal <PWM> are generated based on <PCLK> clock and the *TRIG* pin.
<AGC_EN>, <OBP>, <SHR_EN>, <SH> and <EN> are generated based on <PCLK> clock and the *TRIG* pin.

with CIS Sensor
Sensor drive pulse <CISCK> is generated based on <PCLK> clock.
Internal drive pulse <SHD> is generated based on <PCLK> clock.
Sensor reference signal <SP1> and <SP2>, stop period of sensor drive pulse, and LED control pulse <LED0 ~ 5> and <LED_EN> are generated based on <PCLK> clock and the *TRIG pin.*
Three LED lighting modes, MAN, RGB1 and RGB2, are supported.
<BOS>, <STA>, <CL0>, <CL1> and <EN> are generated based on PLCK clock and the *TRIG* pin.

Rising and falling edges of <P0~2>, <PRS>, <PCL>, <SHD>, <SHR>, <CISCK> and the *TRIG* pin can be set in 1/56 phase of one pixel cycle by referring a rising edge of <PCLK> clock as 0 phase.
<SH0> ~ <SH6>, <PWM>, <SP1>, <SP2>, <LED0 ~ 5> and <LED_EN> change on a rising edge (0 phase) of <PCLK> clock in pixel cycle.

☐ OSC+SYNTH: Pixel Cycle clock generator
Pixel cycle clock is generated by multiplying an external input clock or crystal oscillator signal by 1~1.57 times.
When an external SS clock is input, this block is bypassed and clock frequency of the input clock will be the pixel cycle.

☐ SSCG_PLL: SS clock generator
Generate spread spectrum clock. The SS clock has 30kHz ~ 50kHz modulation cycle and 0.43 ~ 2.08% modulation width.

SS clock generation can also be set ON/OFF setting of is also available. When inputting external SS clock, this SS clock generator should be OFF.

☐ DLL: ADC Operation clock generation Circuit

ADC operational clock is generated from <SHD> by this DLL circuit.

☐ Serial I/F: Control Register, Interface Circuit
This block is a 4-wire serial interface to access control registers.
Control register settings can also be readout.
When *PORT0/1* is input mode, input signal polarity of *PORT0/1* can be read by register value.
When *PORT0/1* is output mode, the output signal polarity can be set by register setting.

☐ LDO: Low Voltage Power Supply block
LDOA generates 1.8V internal power from 3.3V input to the *AVDD33, LDOS, LDODSS0*, *LDODSS1* and *SDVDD33* pins. The AK8464 has three LDOs for the ADC, GIG, TG, LVDS, SYNTH_PLL and SSCG_PLL blocks.

☐ POR: Reset Control block

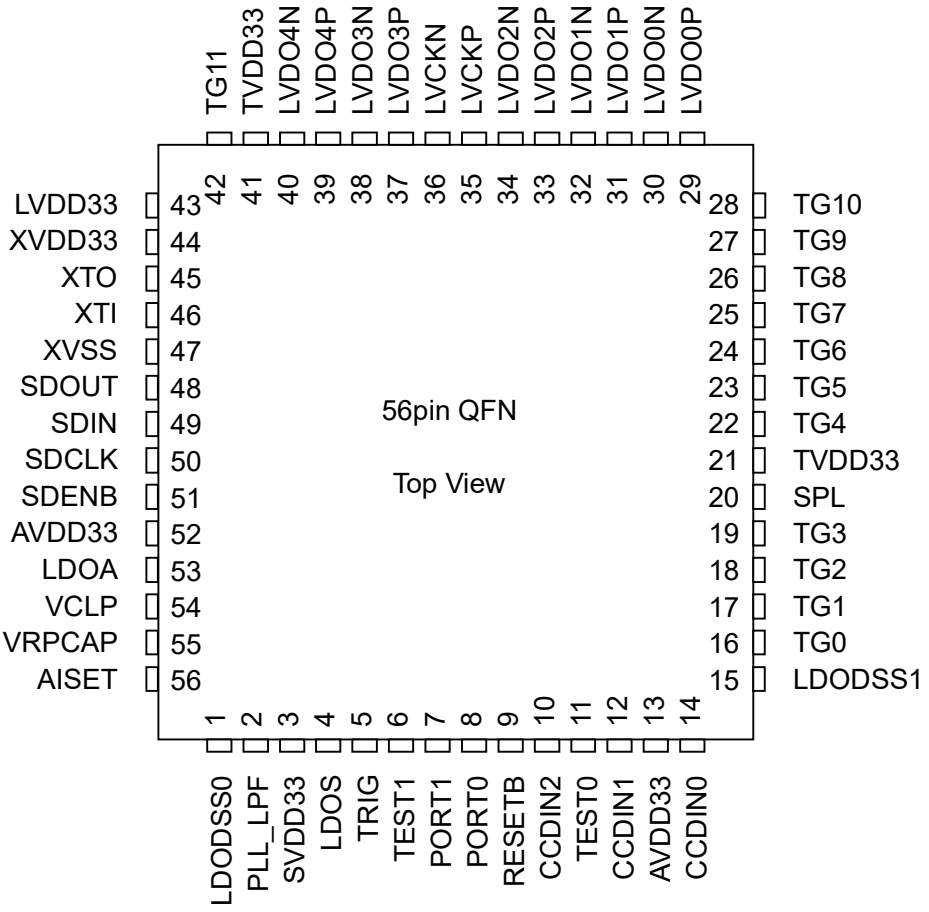
Internal reset release can be controlled by the power-on circuit when power up the AK8464 while the *RESETB* pin is connected to VDD or opened.

☐ CKDET: clock detection Circuit

This block detects if the input clock:<SHD> to DLL is stopped.

5.Pin Configurations and Functions

5.1. Pin Configurations



The exposed pad on the bottom surface of the package must be connected to VSS.

5.2. Pin Functions

No	Pin Name	IO	Reset State (*1)	[SRSTN] (*2)	Description
1	CCDIN0	I	---	---	Sensor signal input CH0
2	AVDD33	P	---	---	Analog Power Supply 3.3V
3	CCDIN1	I	---	---	Sensor signal input CH1
4	TEST0	I	---	---	Test pin (must be fixed to Low) This pin is internally pulled-down by 100kΩ.
5	CCDIN2	I	---	---	Sensor signal input CH2
6	RESETB	I	---	---	Reset signal input This pin is internally pulled-down by 100kΩ.
7	PORT0	IO	---	---	General Purpose Input/Output This pin becomes input during reset. It is internally pulled-down by 100kΩ.
8	PORT1	IO	---	---	General Purpose Input/Output This pin becomes input during reset. It is internally pulled-down by 100kΩ.
9	TEST1	I	---	---	Test pin (must be fixed to Low) This pin is internally pulled-down by 100kΩ.
10	TRIG	IO	---	---	Synchronize signal Input/Output for Main Scanning This pin becomes input during reset. It is internally pulled-down by 100kΩ.
11	LDOS	O	Low	Low	LDO Output 1.8V is generated from SVDD33 and output. Connect a 1.0uF capacitor between this pin and VSS. This pin is internally pulled-down when [NPD] = 0.
12	SVDD33	P	---	---	Power Supply for LDO 3.3V
13	PLL_LPF	IO	Low	Low	CP Output of SSCG_PLL Connect R, C1 and C2 between this pin and VSS. This pin is internally pulled-down when [NPD] = 0. Parasitic capacity of the board connected to *PLL_LPF* must be less than 10pF when [SSCG_ON] = 0.
14	LDODSS0	O	Low	1.8V	LDO Output 1.8V is generated from SVDD33 and output. Connect a 1.0uF capacitor between this pin and VSS. This pin is internally pulled-down during reset.
15	LDODSS1	O	Low	1.8V	LDO Output 1.8V is generated from SVDD33 and output. Connect a 1.0uF capacitor between this pin and VSS. This pin is internally pulled-down during reset.
16	TG0	O	Low	Low	TG Output
17	TG1	O	Low	Low	TG Output
18	TG2	O	Low	Low	TG Output
19	TG3	O	Low	Low	TG Output
20	SPL	O	Low	Low	AFE Sampling signal Output, Internal signal Monitor pin
21	TVDD33	P	---	---	TG Input/Output Buffer Power 3.3V
22	TG4	O	Low	Low	TG Output
23	TG5	O	Low	Low	TG Output
24	TG6	O	Low	Low	TG Output
25	TG7	O	Low	Low	TG Output
26	TG8	O	Low	Low	TG Output
27	TG9	O	Low	Low	TG Output
28	TG10	O	Low	Low	TG Output
29	TG11	O	Low	Low	TG Output
30	TVDD33	P	---	---	TG Input/Output Buffer Power 3.3V
31	LVDO4N	O	High-Z	High-Z	LVDS Data Output

32	LVDO4P	O	High-Z	High-Z	LVDS Data Output
33	LVDO3N	O	High-Z	High-Z	LVDS Data Output
34	LVDO3P	O	High-Z	High-Z	LVDS Data Output
35	LVCKN	O	High-Z	High-Z	LVDS clock Output
36	LVCKP	O	High-Z	High-Z	LVDS clock Output
37	LVDO2N	O	High-Z	High-Z	LVDS Data Output
38	LVDO2P	O	High-Z	High-Z	LVDS Data Output
39	LVDO1N	O	High-Z	High-Z	LVDS Data Output
40	LVDO1P	O	High-Z	High-Z	LVDS Data Output
41	LVDO0N	O	High-Z	High-Z	LVDS Data Output
42	LVDO0P	O	High-Z	High-Z	LVDS Data Output
43	LVDD33	P	---	---	LVDS Output Buffer Power 3.3V
44	XVDD33	P	---	---	Power Supply for Crystal Oscillator 3.3V
45	XTO	O	---	---	Oscillation Circuit Output [EXT_CLK_IN] = 0. Crystal Oscillation mode: [EXT_CLK_IN] = 1. External clock input mode: Do not connect anything.
46	XTI	I	---	---	Crystal/External clock input [EXT_CLK_IN] = 0. Crystal Oscillation mode: [EXT_CLK_IN] = 1. External clock input mode: Input clock
47	XVSS	P	---	---	Ground for Crystal Oscillator
48	SDOUT	O	High-Z	High-Z	Serial I/F Data Output Connect an external pull-up or pull-down resistor since this pin is tri state buffer.
49	SDIN	I	---	---	Serial I/F Data input
50	SDCLK	I	---	---	Serial I/F clock input
51	SDENB	I	---	---	Serial I/F Data Enable input
52	AVDD33	P	---	---	Analog Power Supply 3.3V
53	LDOA	O	Low	Low	LDO Output 1.8V is generated from SVDD33 and output. Connect a 1.0uF capacitor between this pin and VSS. This pin is internally pulled-down when [NPD] = 0.
54	VCLP	IO	High-Z	High-Z	Sensor signal Reference Voltage Input/Output
55	VRPCAP	O	Low	Low	AFE Reference Voltage Output Connect a 1.0uF capacitor between this pin and VSS.
56	AISET	O	---	---	Resistor Connection for Bias Current setting Connect an 8.2kΩ resistor between this pin and VSS.
Tab	VSS	P	---	---	Ground

Note
(* 1) When “*RESETB* is Low” or “Reset state by POR circuit”.
(* 2) In case of "[SRSTN] = 0" in a wait state for ”Register access" after LDODSS started up.

6. Ordering Guide

AK8464	0~85ºC	56-pin QFN

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.