



AK9223MK

Application notes

This document shows circuit and layout diagrams of the AK9223 as the reference design.

■ Circuit Diagram

It shows compositions of power supply decoupling capacitors and analog input filters. Switching land patterns are also shown here since the internal/external VREF or CLK can be selected with the AK9223.

Peripheral Parts/Pattern Details

- R1, R2, C1, C2, C3: Low-pass Filter of the AIN1
- R3, R4, C4, C5, C6: Low-pass Filter of the AIN0
- C7, C8, C12, C13: Decoupling Capacitor for AVDD
- C9: Decoupling Capacitor for DVDD
- C10: Decoupling Capacitor for REFI1
- C11: Decoupling Capacitor for REFI0
- SH0, SH1: Internal/External Switching of the VREF
- EXT, INT: Internal/External Switching of the CLK

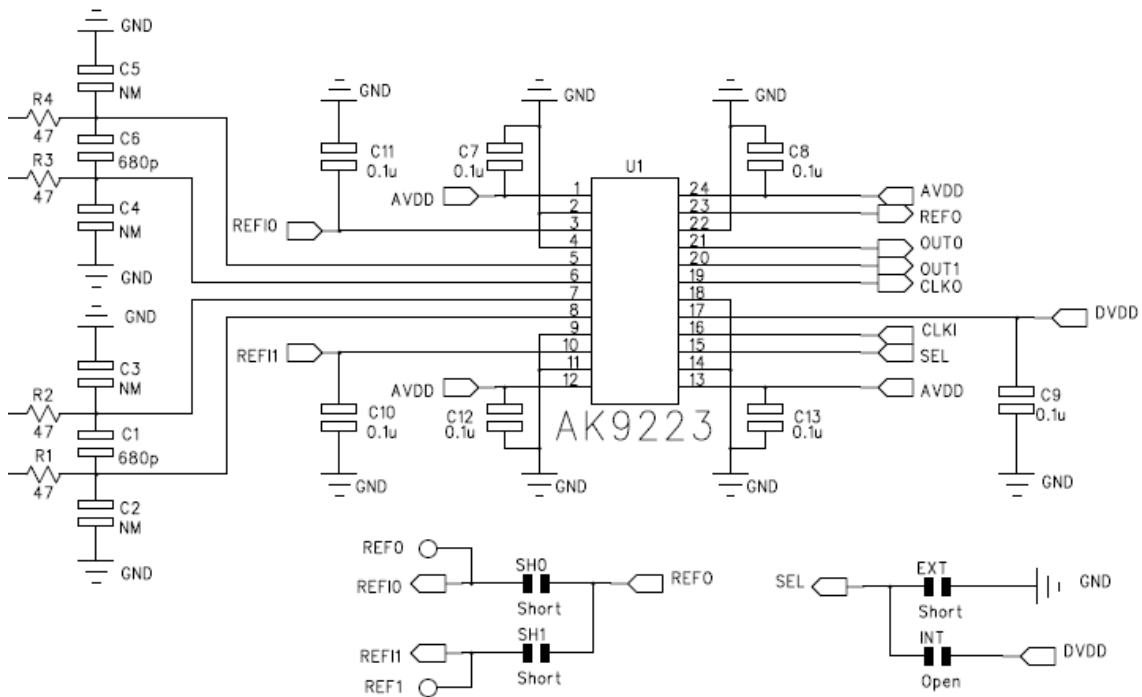


Figure 1. AK9223 Circuit Diagram

■ Layout

Four layered printing board is used. The second layer is for the ground and the third layer is for power supply. AVDD and DVDD are separated on the power supply layer.

All areas except parts and wirings are GND in the first and the fourth layers.

All used chip parts here are located as 1005 (1.0mm x 0.5mm) size layout.

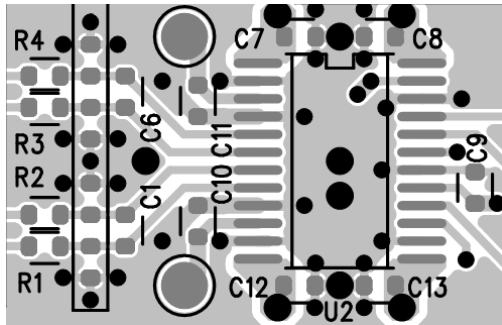


Figure 2. First Layer Layout

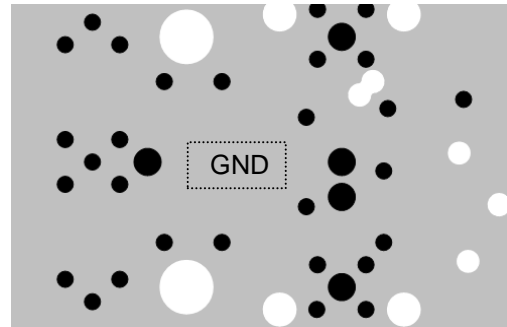


Figure 3. Second Layer Layout

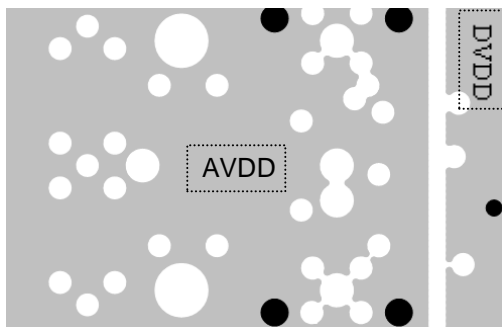


Figure 4. Third Layer Layout

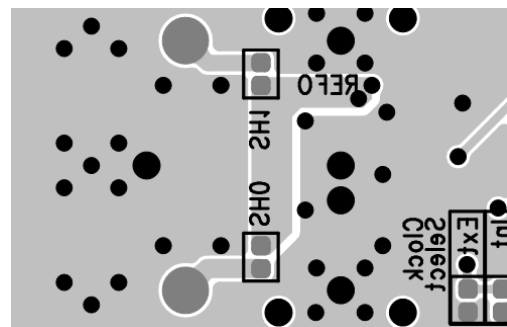


Figure 5. Fourth Layer Layout (Reverse Side)

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Inquiry

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