AK9235

Dual 12-Bit 1.03MSPS SAR A/D Converter

1. General Description

The AK9235 is a 12-bit 1.03MSPS SAR A/D converter. It supports a wide range of power supply voltage, realizing to compose a general purpose system while reducing the cost. It is easy to achieve the system characteristics since it is configured with small input capacity. In addition, low current consumption is achieved therefore a low power consumption system can be designed.
The AK9235 is available in a small package, saving space on the printing board.

Application

- Motor Control: Position Measurement Using SinCos Encoders
- Three-Phase Power Controls
- Programmable Logic Controllers
- Power Quality Measurement
- Industrial Automation

2. Features

☐	2ch Simultaneous Sampling 12-bit SRA A/D Converter	
☐	Sampling Rate:	1.03MSPS
☐	Differential/Pseudo Differential Inputs	
☐	12-bit No Missing Code,	INL: ±1.0LSB (Max.)
☐	S/N	73 dB (Typ.) at 20kHz Input
☐	Power Consumption	VDD: 6 mA (Typ.) DRVDD: 0.25 mA (Typ.) (fs=1.03MSPS, VDD= 5.0V, DRVDD=3.3V)
☐	Input Capacitance:	13 pF (Typ.)
☐	Power Supply	VDD: 3.0 ~ 5.5 V DRVDD: 2.7 ~ 5.5 V
☐	Operation Temperature:	-40 ~ 125ºC
☐	Package:	Small 16-pin QFN (3mm x 3mm, 0.5mm pitch)
☐	Pin Compatible with ADS7250	

3. Table of Contents

4. Block Diagram

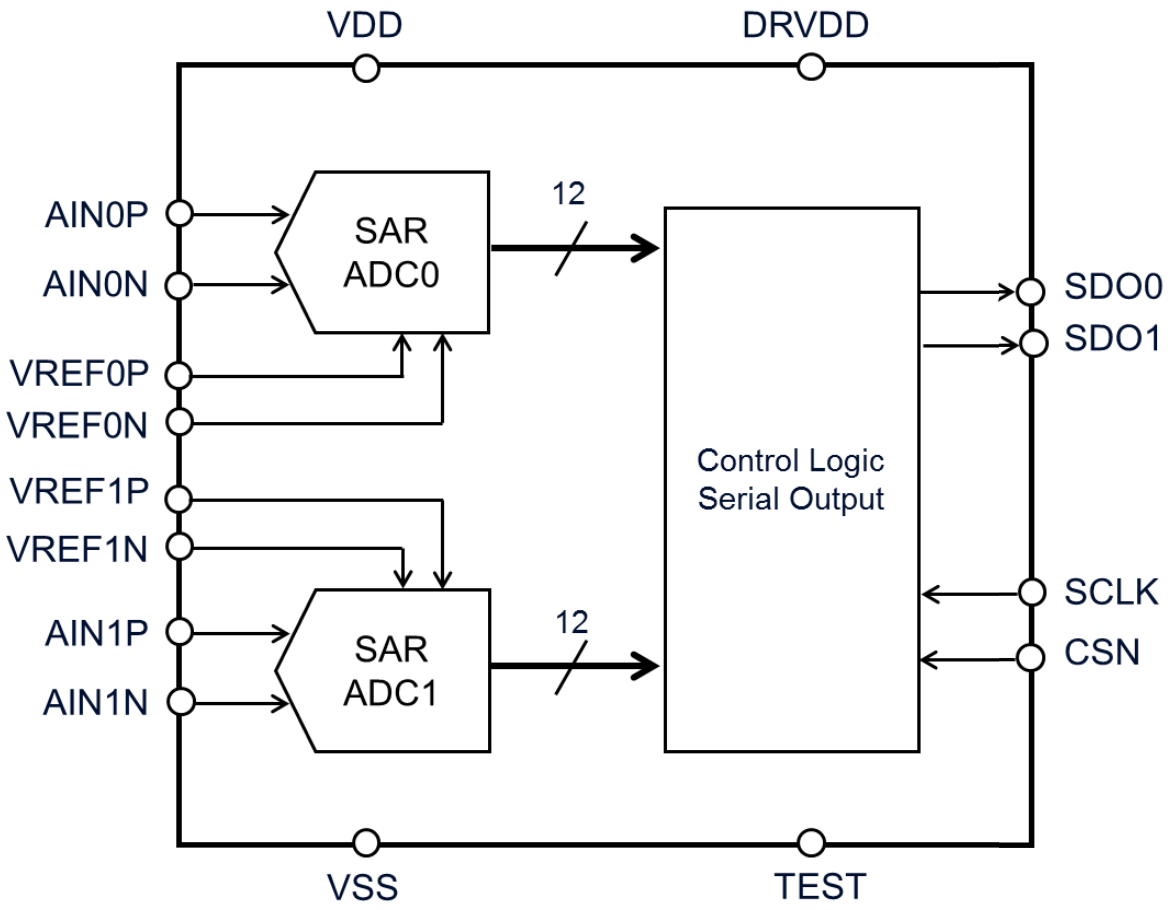
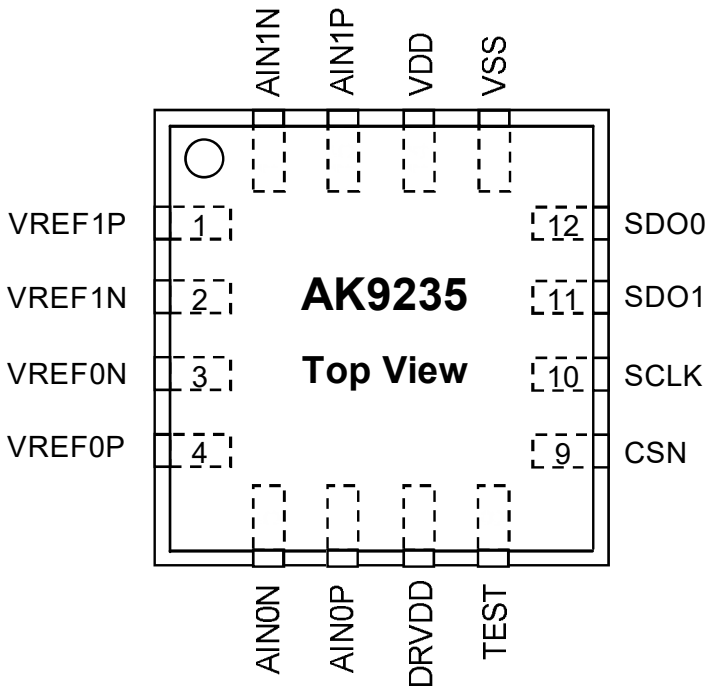


Figure 1. Block Diagram

5. Pin Configurations and Function

■ Pin Layout



■ Pin Functions

Pin No.	Pin Name	I/O	Function
1	VREF1P	AI	ADC1 High level Voltage Reference Input Decouple this pin to VREF1N with a 1μF capacitor.
2	VREF1N	AI	ADC1 Low level Voltage Reference Input This pin must be connected to VSS.
3	VREF0N	AI	ADC0 Low level Voltage Reference Input This pin must be connected to VSS.
4	VREF0P	AI	ADC0 High level Voltage Reference Input Decouple this pin to VREF0N with a 1μF capacitor.
5	AIN0N	AI	ADC0 Negative Analog Input
6	AIN0P	AI	ADC0 Positive Analog Input
7	DRVDD	P	Digital Power Supply
8	TEST	DI	Test Pin. This pin must be connected to VSS. This pin is connected to VSS by internal resistor. (typ. 100kΩ)
9	CSN	DI	Chip Select Pin (* 2)
10	SCLK	DI	Clock Input (* 2)
11	SDO1	DO	ADC1 Serial Data Output
12	SDO0	DO	ADC0 Serial Data Output
13	VSS	G	Ground
14	VDD	P	Analog Power Supply
15	AIN1P	AI	ADC1 Positive Analog Input
16	AIN1N	AI	ADC1 Negative Analog Input
Thermal pad		-	Exposed thermal pad. Open or connect to VSS. AKM recommends connecting the thermal pad to VSS.

Notes:

* 1. AI: Analog Input, DI: Digital Input, DO: Digital Output, P: Power Supply, G: Ground
* 2. Digital input pins (CSN, SCLK) must not be allowed to float.
* 3. In this document, there is a case that describes VREF0P and VREF1P as VREFxP, VREF0N and VREF1N as VREFxN, AIN0P and AIN1P as AINxP, AIN0N and AIN1N as AINxN, and SDO0 and SDO1 as SDOx.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Pin Name	Setting
AIN0P, AIN0N, VREF0P, VREF0N	Connect to VSS
AIN1P, AIN1N, VREF1P, VREF1N	Connect to VSS

6. Absolute Maximum Ratings

(VSS = VREF0N = VREF1N = 0V; * 4)

Parameter	Symbol	Min.	Max.	Unit
Power Supply1	VDD	-0.3	+6.2	V
Power Supply2	DRVDD	-0.3	+6.2	V
Analog Input Current * 5	AIN	-	±10	mA
Digital Input Current * 6	DIN	-	±10	mA
Analog Input Voltage * 5	AVIN	-0.3	VDD+0.3	V
Digital Input Voltage * 6	DVIN	-0.3	+6.2	V
Storage Temperature	Tstg	-65	150	ºC

Note:
* 4. All voltages are with respect to ground (VSS).
* 5. VREF0P, VREF1P, AIN0P, AIN0N, AIN1P, and AIN1N pins
* 6. CSN and SCLK pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS = VREF0N = VREF1N = 0V; * 4)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply1 * 7	VDD	3.0	5.0	5.5	V
Power Supply2 * 7	DRVDD	2.7	3.3	5.5	V
Ambient Operating Temperature	Ta	-40	-	125	ºC

Note:
* 4. All voltages are with respect to ground (VSS).
* 7. The power supply condition must always satisfy “DRVDD ≤ VDD + 0.3V”.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

(Ta = -40 ~ 125ºC; VDD= 5.0V; DRVDD= 3.3V; fs= 1.03MSPS, VREFxP= VREF= 2.5V, AINxP= -0.5dBFS, AINxN= 2.5V; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
Analog Input						
Full Scale Range			-VREF	-	VREF	V
Absolute Input Voltage Range * 8	Pseudo Differential (AINxP)		0	-	2 × VREF	V
	Pseudo Differential (AINxN)		VREF-0.1	VREF	VREF+0.1	V
	Differential (AINxP, AINxN)		VCM - VREF/2	-	VCM +VREF/2	V
	Differential (VCM) * 9		0.45 × VDD	0.5 × VDD	0.55 × VDD	V
Input Capacitance		In Sample Mode	-	13	-	pF
		In Hold Mode	-	4	-	pF
Input Leakage Current		In Sample Mode	-	1.5	-	nA
Sampling Dynamics						
Throughput Rate			-	-	1.03	MSPS
Aperture Delay			-	8	-	ns
Aperture Delay match			-	40	-	ps
Aperture Jitter			-	10	-	ps
Clock Frequency			0.5	-	33	MHz
External Reference Voltage						
Reference Input Voltage Range * 8			0.45 x VDD	2.5	0.5 x VDD	V
Reference Input Current			-	120	-	µA
Reference Leakage Current	In Sample Mode		-	-	1	µA
External ceramic reference capacitance			-	1	-	µF
Power Supply Current						
Analog Supply Current	During Conversion		-	6	9	mA
	No Conversion		-	4	7	mA
Digital Supply Current	For code 800h		-	0.25	-	mA

Notes:

* 8. VDD ≥ 2 x VREF

* 9. Common-Mode Voltage Range: VCM = (AINxP+AINxN)/2

Parameter		Min.	Typ.	Max.	Unit
Resolution		12	-	-	bit
Static Characteristics					
No Missing Codes		12	-	-	bit
Integral Nonlinearity (INL) Error		-1	±0.5	1	LSB
Differential Nonlinearity (DNL) Error		-0.99	±0.4	1	LSB
Offset Error		-2	±0.75	2	mV
Offset Error Channel Mismatch		-2	±0.75	2	mV
Offset Error Thermal Drift		-	1	-	µV/°C
Gain Error		-0.1	±0.05	0.1	%
Gain Error Channel Mismatch		-0.1	±0.05	0.1	%
Gain Error Thermal Drift		-	1	-	ppm/°C
Common-Mode Rejection Ratio * 10		-	74	-	dB
Dynamics Characteristics					
S/(N+D)	fin = 20kHz	71.5	73	-	dB
	fin = 100kHz	-	73	-	dB
	fin = 250kHz	-	72	-	dB
S/N	fin = 20kHz	72	73	-	dB
	fin = 100kHz	-	73	-	dB
	fin = 250kHz	-	72	-	dB
THD	fin = 20kHz	-	-90	-	dB
	fin = 100kHz	-	-86	-	dB
	fin = 250kHz	-	-80	-	dB
SFDR	fin = 20kHz	-	90	-	dB
	fin = 100kHz	-	90	-	dB
	fin = 250kHz	-	84	-	dB
Channel to Channel Isolation	fin = 20kHz fNOISE = 25kHz	-	-90	-	dB
Full power Bandwidth	@ -3dB	-	25	-	MHz
	@ -0.1dB	-	5	-	MHz

Notes:
* 10. DC to 20kHz

9. DC Characteristics

(Ta= -40 ~ 125ºC, DRVDD=2.7V ~ 5.5V)

Parameter	Symbol	Min.	Max.	Unit
High-Level Input Voltage * 11	VIH	0.7 x DRVDD	-	V
Low-Level Input Voltage * 11	VIL	-	0.3 x DRVDD	V
High-Level Output Voltage (Iout = -1mA) * 12	VOH	0.8 x DRVDD	-	V
Low-Level Output Voltage (Iout = 1mA) * 12	VOL	-	0.2 x DRVDD	V
Input Leakage Current * 11	Iin	-1	+1	μA

Notes:

* 11. CSN and SCLK pins
* 12. SDO0 and SDO1 pins
* 13. Outgoing current from the AK9235 is defined as “-” polarity, and incoming current to the AK9235 is defined as “+” polarity.

10. Switching Characteristics

(Ta= -40 ~ 125ºC, VDD=3.0V ~ 5.5V, DRVDD=2.7V ~ 5.5V, C_L=10pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CSN Clock Frequency		fCSN	-	-	1.03	MSPS
CSN Clock Period		tCSN	0.97	-	-	µs
SCLK Clock Frequency		fSCK	0.5	-	33	MHz
SCLK Clock Period		tSCK	30.3	-	2000	ns
SCLK High Pulse Width	tSCK= 1/fSCK	tSCKH	0.4 × tSCK	-	-	ns
SCLK Low Pulse Width	tSCK= 1/fSCK	tSCKL	0.4 × tSCK	-	-	ns
Conversion time		tCONV	-	tCSS+ 14 x tSCK	-	ns
Acquisition time		tACQ	70	-	-	ns
CSN High time		tCS	20	-	-	ns
CSN High time after frame abort		tCSSH	70	-	-	ns
CSN "↓" to SDOx "0" Delay		tCSD	-	-	12	ns
31st SCLK "↓" to CSN "↑"		tCHH	15	-	-	ns
CSN "↑" to SDOx Hi-Z State	* 14	tCCZ	-	-	10	ns
CSN "↓" to First SCLK "↓"		tCSS	15	-	-	ns
Setup time : SDOx Valid to SCLK "↓"		tDS	5	-	-	ns
Hold time : SCLK "↓" to SDOx Valid data		tDH	3	-	-	ns

Notes:

* 14. Guaranteed by design. This value is not tested in mass production.

■ Timing Diagram

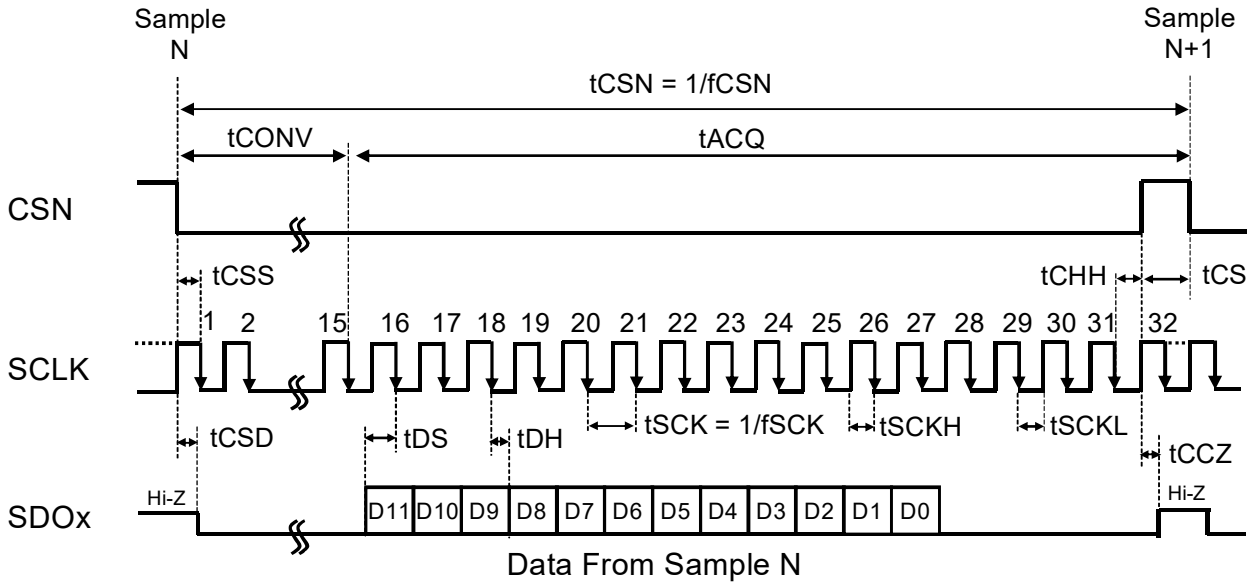


Figure 2. Data Output Timing

11. Functional Descriptions

■ Analog Input

The AK9235 supports differential input and pseudo differential input data.

(1) Pseudo Differential Input
Input VREF voltage to the AINxN pin.
In pseudo differential input mode, the AK9235 executes AD conversion if the AINxP pin input is in a range from 0V to “2 x VREF”.
However, the input voltage must not exceed VDD.

(2) Differential Input
In differential input mode, the AK9235 executes AD conversion if the differential voltage (AINxP - AINxN) is in a range from –VREF to +VREF.
In this case, the center voltage (VCM) at the AINxP and the AINxN pins must be in a range from “0.45 x VDD” to “0.55 x VDD”.

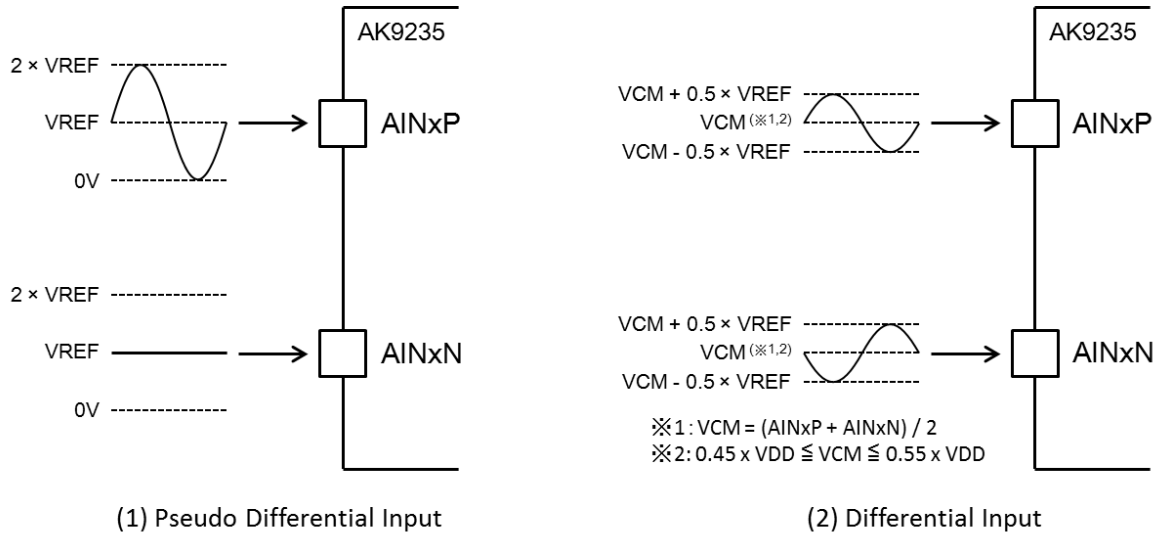


Figure 3. Analog Input Amplitude with Pseudo Differential and Differential Inputs

■ ADC Output Code

The AK9235 output data is 2's complement format. The full scale and LSB size is shown below.

Full Scale = 2 * VREF

1LSB = Full Scale / 4096 [V]

Input/Output transfer function of the AK9235 is shown below.

Table 1. ADC Transfer Function

Analog Input	Input Voltage			Output Code (HEX)
	AINxP	AINxN	AINxP – AINxN	Digital Data
Pseudo – Differential	0	VREF	– VREF	800
	1 LSB		– VREF + 1 LSB	801
	VREF – 1 LSB		– 1 LSB	FFF
	VREF		0	000
	2 × VREF – 1 LSB		VREF – 1 LSB	7FF
Differential	VCM – VREF / 2	VCM + VREF / 2	– VREF	800
	VCM – VREF / 2 + 0.5 LSB	VCM + VREF / 2 – 0.5 LSB	– VREF + 1 LSB	801
	VCM – 0.5 LSB	VCM + 0.5 LSB	– 1 LSB	FFF
	VCM	VCM	0	000
	VCM + VREF / 2 – 0.5 LSB	VCM – VREF / 2 + 0.5 LSB	VREF – 1 LSB	7FF

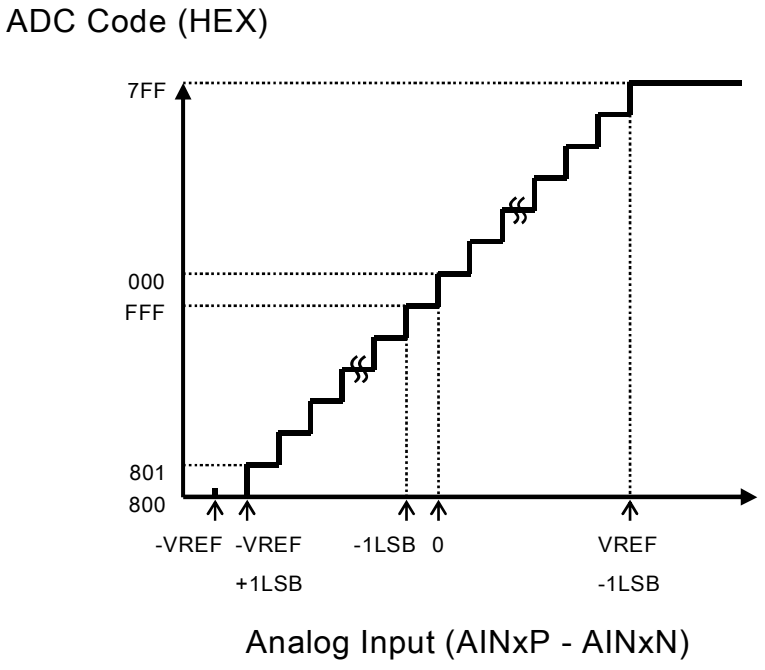


Figure 4. ADC Transfer Function

12. Digital Interface

■ Normal Opertaion Timing

Input signal is sampled on a falling edge of CSN and AD conversion starts. The conversion phase ends 15th falling edge of SCLK after the falling edge of CSN. “L” data is output from the SDOx pin during the conversion and a 12-bit AD converted data starts being output in MSB first on the 15th falling edge of SCLK. It outputs “L” data after the 27th falling edge of SCLK.
The AK9235 also enters acquisition phase and start sampling the input signal for the next AD conversion on the 15th falling edge of SCLK.
In normal operation, set the CSN pin to “H” after the 27th falling edge of SCLK. The SDOx output will become “Hi-Z” after a rising edge of CSN.

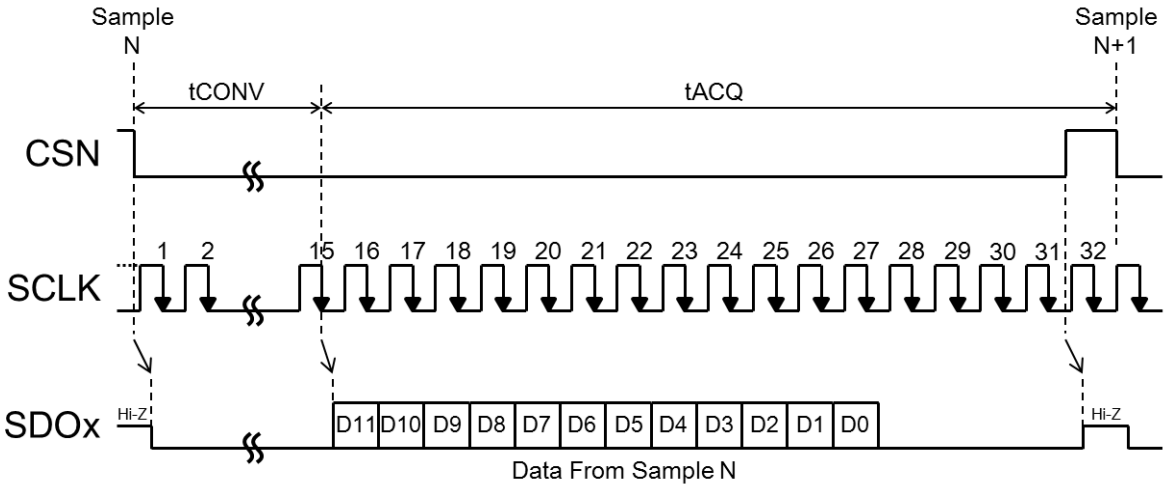


Figure 5. Data Output Timing in Normal Operation

■ Interrupt Timing

The AK9235 finishes transmission of 12-bit data on the 27th falling edge of SCLK.
The followings show cases that CSN is set to “H” before the 27th falling edge of SCLK.

(1) When CSN is set to “H” before the 15th falling edge of SCLK
The AD conversion is cancelled and the SDO output becomes “Hi-Z” state. The AK9235 also enters acquisition phase.

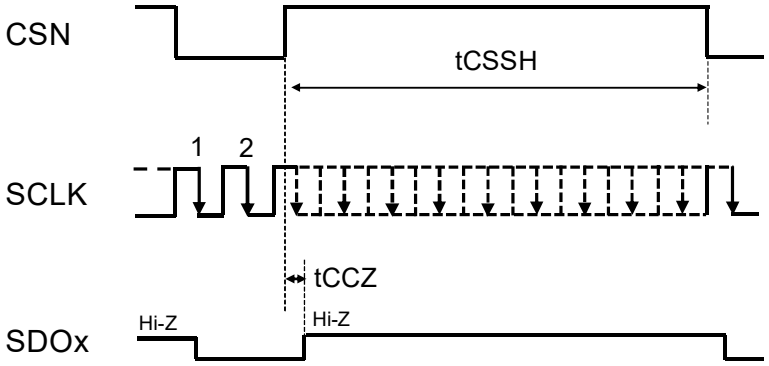


Figure 6. Interrupt Operation (before 15th SCLK “↓”)

(2) When CSN is set to “H” after the 15th falling edge of SCLK
The SDO output becomes “Hi-Z” state after transmitting the data that is output until the rising edge of CSN as valid data.

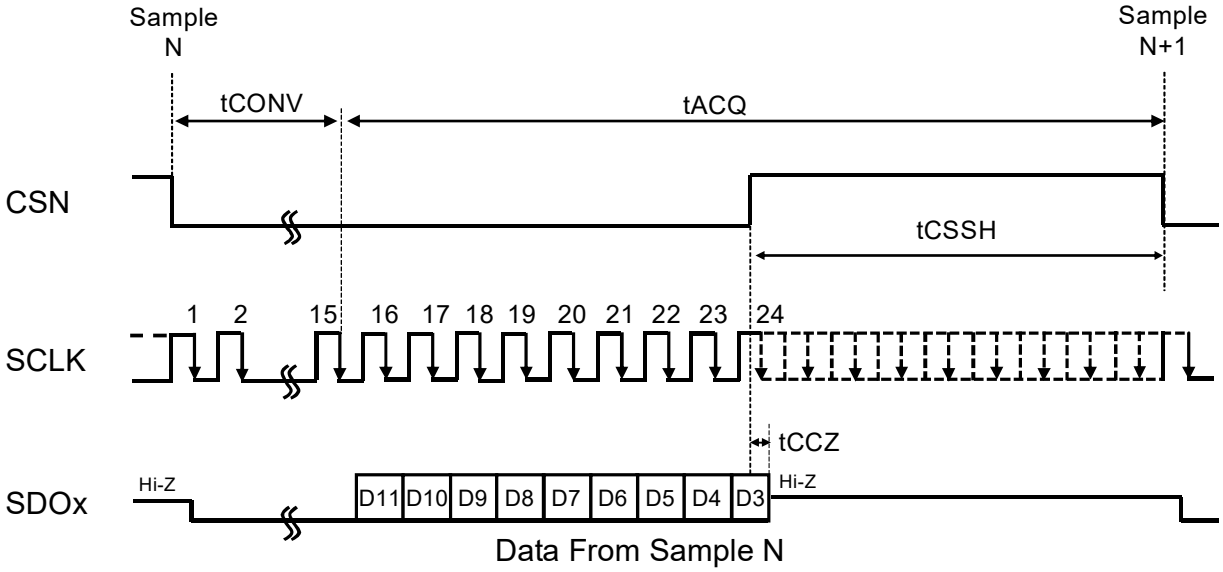


Figure 7. Interrupt Operation (after 15th SCLK “↓”)

Set the CSN pin to “L” with an interval of tCSSH (min. 70ns) for the next conversion if an interrupt shown in Figure 6 or Figure 7 is occurred.

■ System Reset

Set the CSN pin to “L” and input SCLK to start AD conversion after the VDD / DRVDD are powered up.

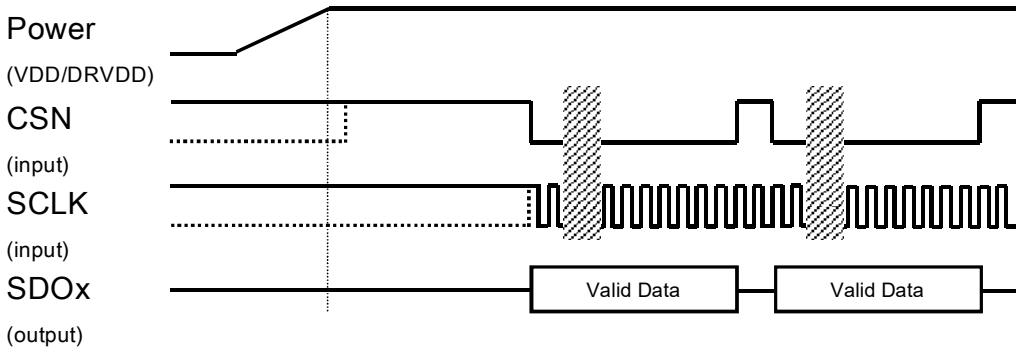


Figure 8. Power-up Sequence

13. Recommended External Circuits

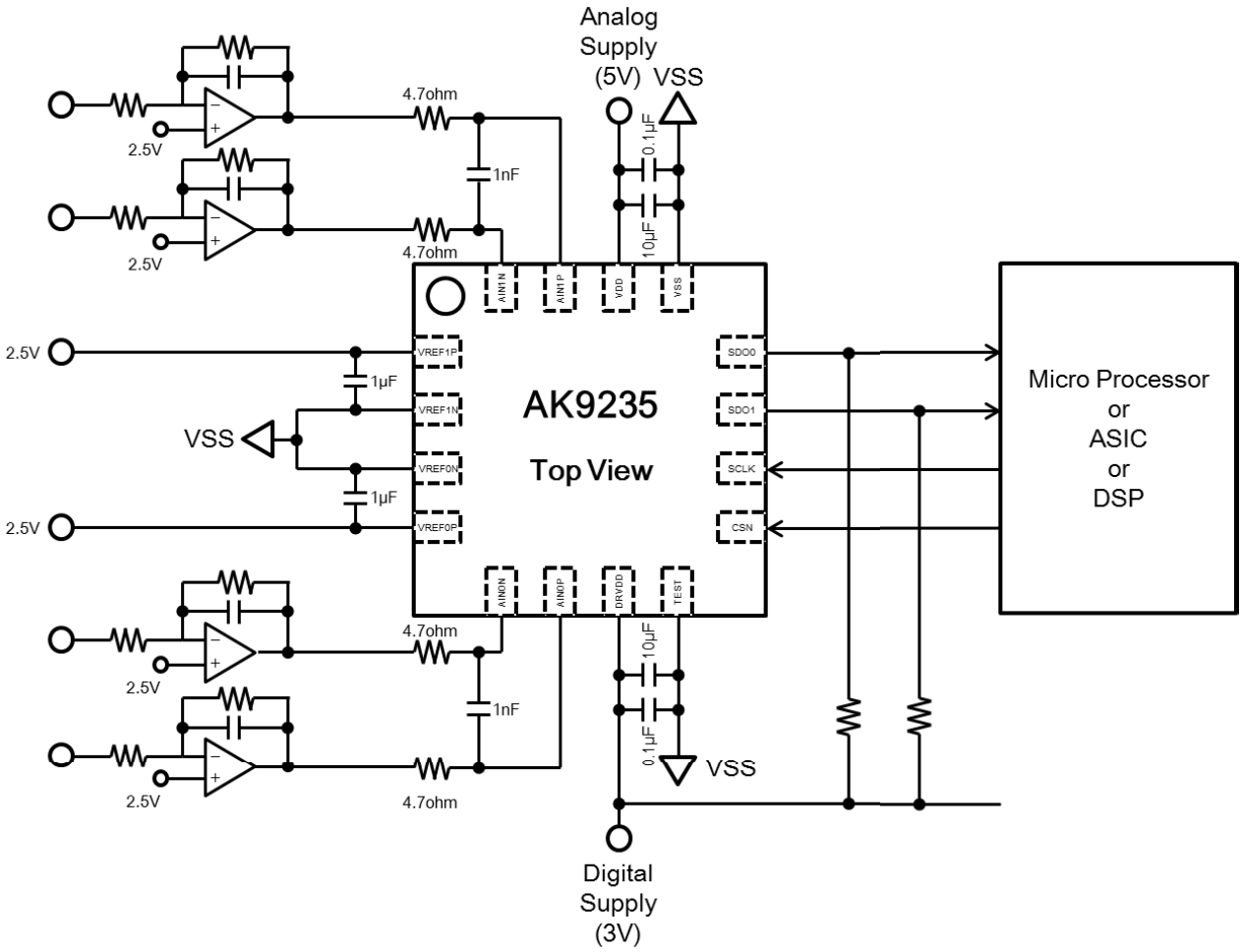
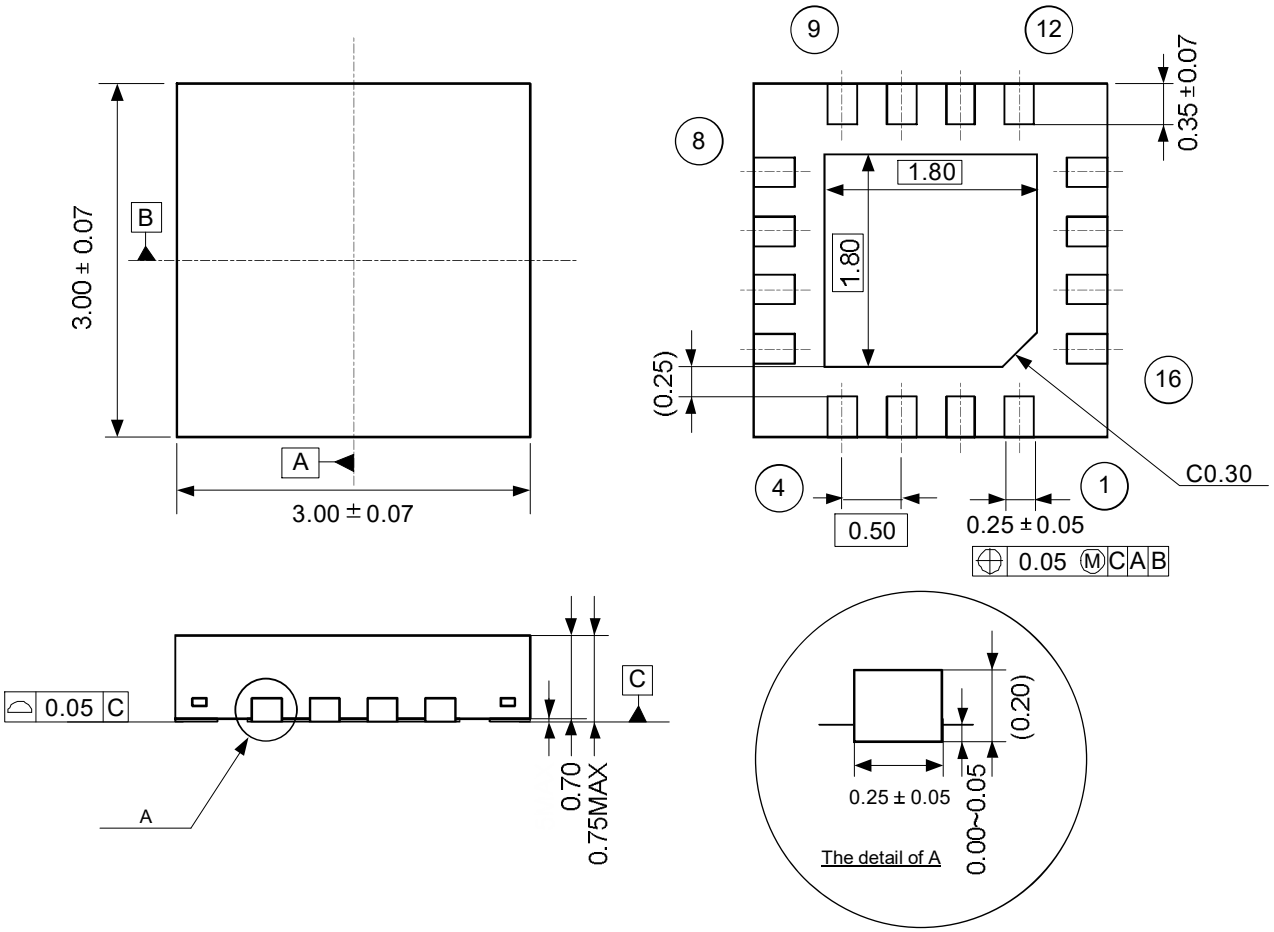


Figure 9. Typical Connection Example

14. Package

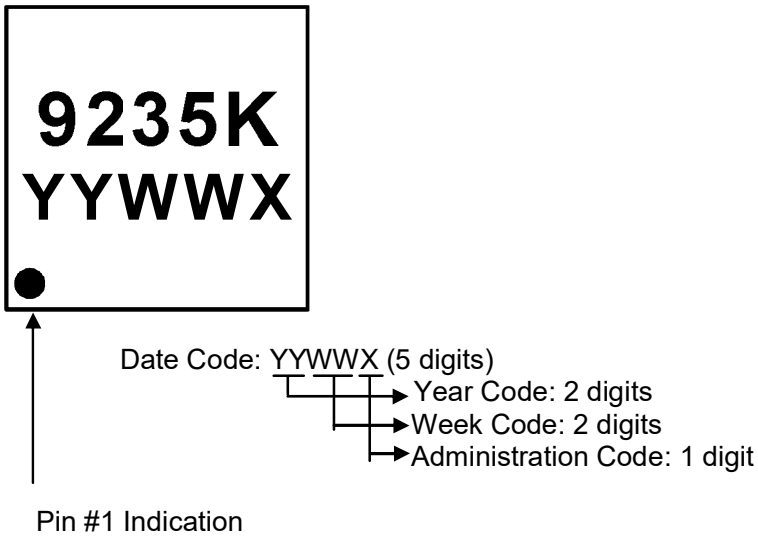
■ **Outline Dimensions**



Note:

* 15. The exposed pad on the bottom surface of the package must be open or connected to the ground.
The PCB wiring density must be more than 200%.
AKM recommends connecting the exposed pad to the ground.

■ Marking


9235K
YYWWX
Date Code: YYWWX (5 digits)
Year Code: 2 digits
Week Code: 2 digits
Administration Code: 1 digit
Pin #1 Indication

15. Ordering Guide

AK9235NK	-40 ~ 125ºC	16-pin QFN (3.0mm x 3.0mm, 0.5mm pitch)
AKD9235	Evaluation Board for AK9235	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/2/9	00	First Edition		

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