



# AK9240NK

## Application notes

This document shows circuit and layout diagrams of the AK9240 as the reference design.

**■ Circuit Diagram**

It shows compositions of power supply decoupling capacitors.

**Peripheral Parts/Pattern Details**

- C7 : Capacitor for LED Driver Band Adjustment
- C8 : Decoupling Capacitor for VDD1
- C9 : Decoupling Capacitor for DRVDD
- C10 : Decoupling Capacitor for VDD0
- C11 : Decoupling Capacitor for VREFP

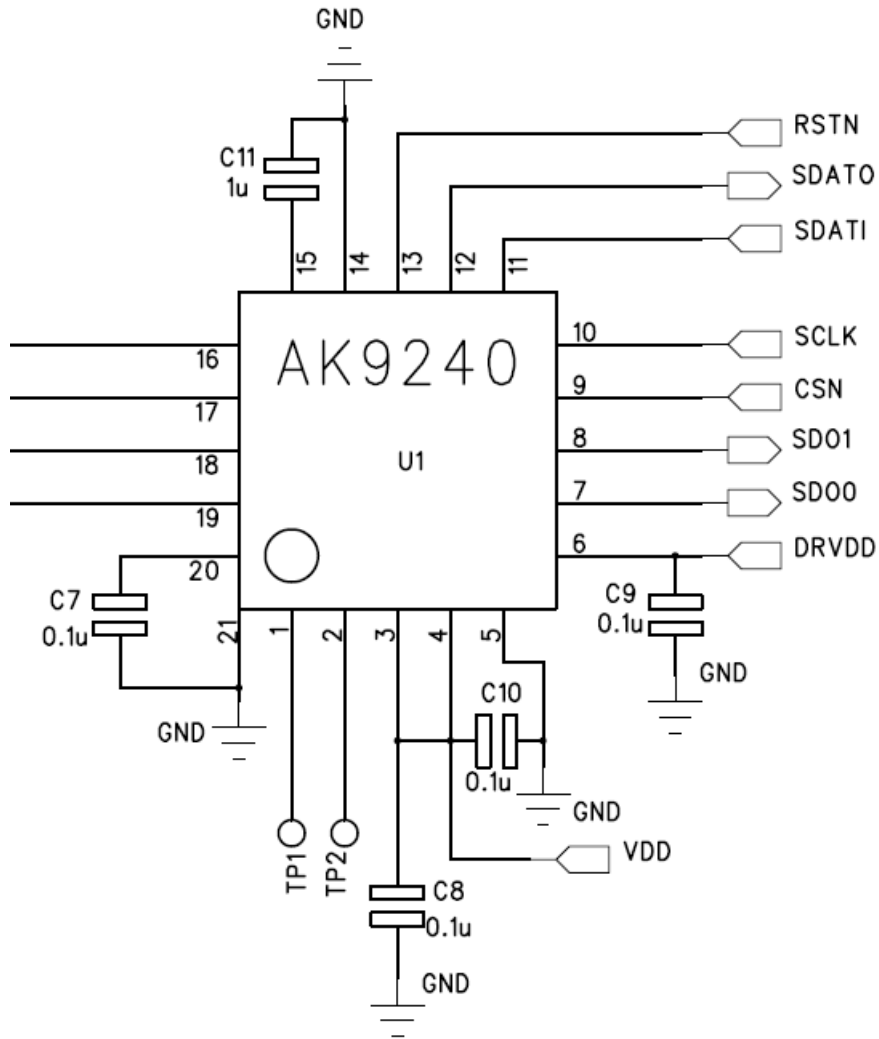


Figure 1 Circuit Diagram

**Layout**

Four layered printing board is used. The second layer is for the ground and the third layer is for power supply. VDD and DRVDD are separated on the power supply layer.

All areas except parts and wirings are GND in the first and the fourth layers.

All used chip parts here are located as 1005 (1.0mm x 0.5mm) size layout.

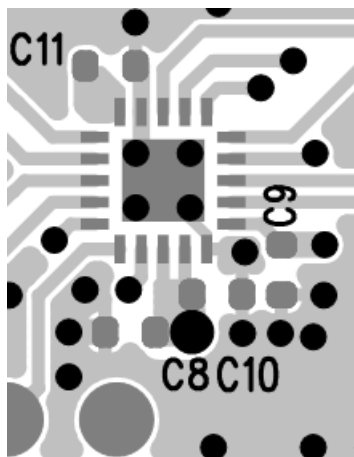


Figure 2 First Layer Layout

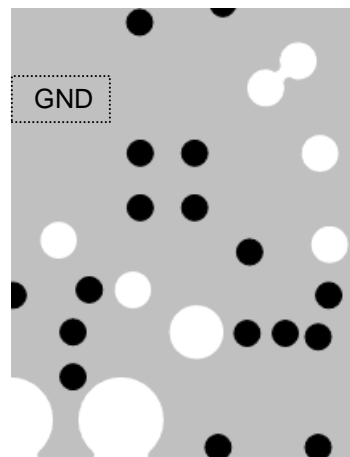


Figure 3 Second Layer Layout

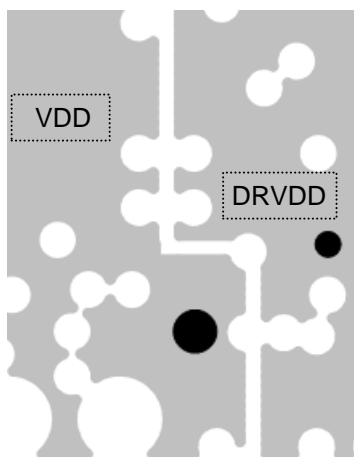


Figure 4 Third Layer Layout



Figure 5 Fourth Layer Layout (Reverse Side)

Digital wiring reduction method for the AK9240 is shown in this document.

The AK9240 has the SDATI and the SDATO pins. Wiring can be reduced according to the application and the environment.

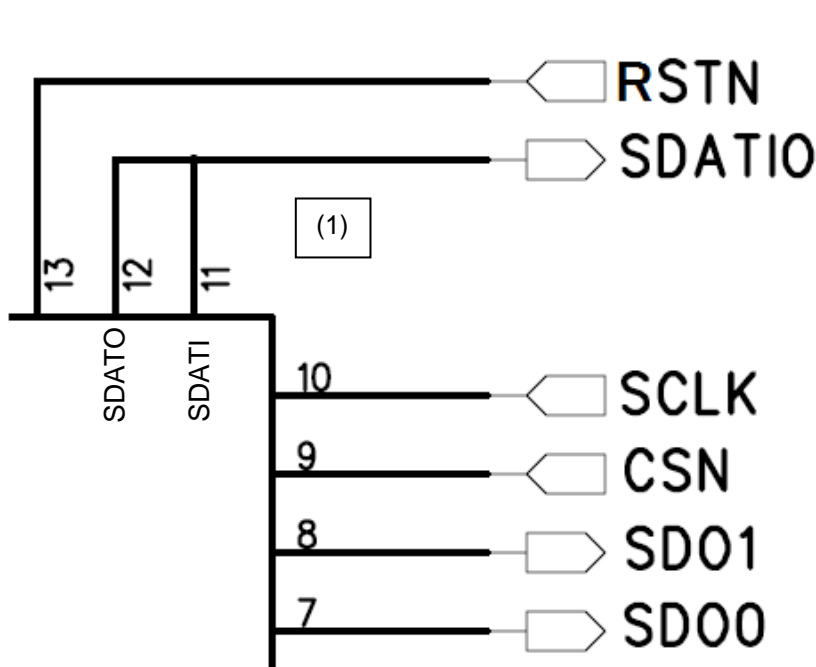


Figure 6. Circuit Diagram

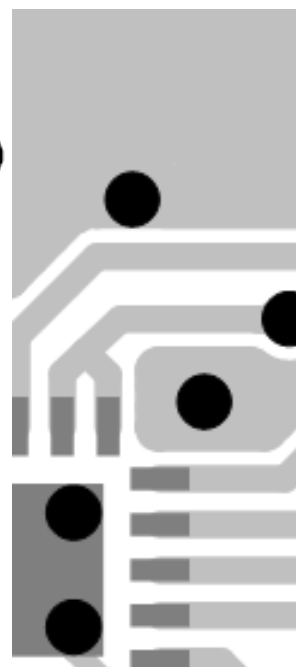


Figure 7. Layout

**(1) Short of SDATO/SDATI Pins**

Register writing and reading via 3-wire serial interface (CSN, SCLK and SDATI/SDATO pins) are enabled by shorting the SDATO pin and the SDATI pin.

In this case, the pin of a connected device to the AK9240 should be I/O pin.

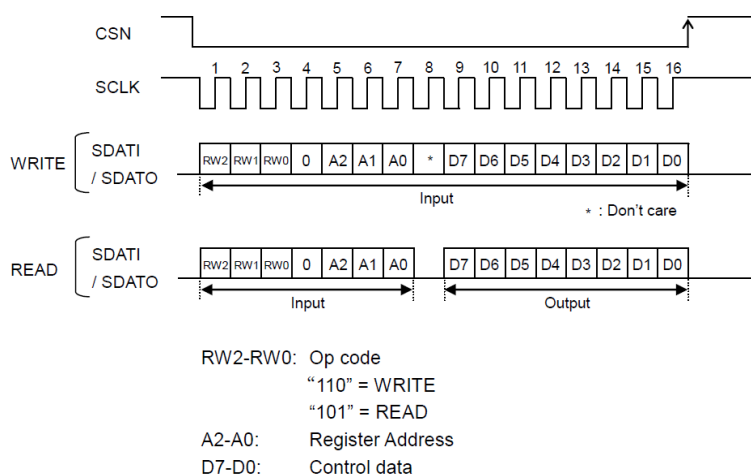


Figure 8. Serial I/F Timing (SDATI, SDATO Common)

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**Inquiry**

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