GENERAL DESCRIPTION

The AKD5522-A is an evaluation board for AK5522, which is 32bit, 8k - 192kHz, 2ch ADC. The AKD5522-A is includes the analog input circuit and also has a digital interface transmitter. Further, the AKD5522-A can achieve the interface with digital audio systems via output-connector.

Ordering guide
AKD5522-A -- Evaluation board for AK5522

FUNCTION

• DIT with COAX or Optical digital output.
• ADC 2ch input is possible.
• SMA connector for an external clock input.
• DAC 2ch Analog outputs.

Figure 1. AKD5522-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.
**Description**

(1) U101 (AK5522)  
32bit, 8k - 192kHz, 2ch A/D Converter.

(2) J201, J202 (Analog data)  
Mini-pin jack connector: Differential Analog Input

(3) U301 (AK4118A)  
AK4118A has DIT. Transports output data from AK5522.

(4) J301 / PORT301 (Digital data)  
COAX Connector / Optical Connector: Digital Output.

(5) PORT401 (Pin header)  
Pin header for evaluation (MCLK, BICK, LRCK, SDTO).

(6) U302 (AK4432)  
AK4432 has DAC. Outputs analog data from AK5522.

(7) SW501 (Toggle switch)  
Toggle type-switch PDN for AK5522.  
"H": PDN = High  
"L": PDN = Low

(8) SW504 (Toggle switch)  
Toggle type-switch PDN for AK4118A.  
"H": PDN = High  
"L": PDN = Low

(9) SW505 (Toggle switch)  
Toggle type-switch PDN for AK4432.  
"H": PDN = High  
"L": PDN = Low
(10) SW506 (Toggle switch)
Toggle type-switch SMUTE for AK4432.
“H”: PDN = High
“L”: PDN = Low

(11) SW501 (Dip switch)
DIP type-switch for AK5522.
“H”: Digital signal = High
“L”: Digital Signal = Low

(12) SW301 (Dip switch)
DIP type-switch for AK4118A.
“H”: Digital signal = High
“L”: Digital Signal = Low

(13) SW502 (Dip switch)
DIP type-switch for AK4432.
“H”: Digital signal = High
“L”: Digital Signal = Low

(14) J401 (MCLK external input)
SMA Connector: External Clock Input (MCLK).

(15) J701, J702, J703, J704, J705, J706, J708 (Power supply)
Power Supply Connector.
## Evaluation Board Manual

### Operation sequence

1. Power supply line settings
2. Jumped pins settings
3. DIP switches settings
4. Toggle switches settings
5. Register control (Serial control)
[1] Power supply line settings

(1-1) Power supply settings : Used the regulator <Default>

Set up the power supplied lines :

* Each supply line should be distributed from the power supply unit.

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Setting (Typ)</th>
<th>Function</th>
<th>Comments</th>
<th>Default Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>J701</td>
<td>+12V</td>
<td>Red</td>
<td>+12V</td>
<td>Regulator power supply</td>
<td>Should always be connected</td>
</tr>
<tr>
<td>J702</td>
<td>AVDD</td>
<td>Yellow</td>
<td>+5.0V / 3.3V</td>
<td>AK5522 AVDD</td>
<td>5.0V regulator is used, JP701=5.0V and JP702=REG by default.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When 3.3V regulator is used, JP701=3.3V and JP702=REG.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When jack is used, JP702=CON.</td>
</tr>
<tr>
<td>J703</td>
<td>DAC</td>
<td>Yellow</td>
<td>+3.3V</td>
<td>AK44322 AVDD</td>
<td>3.3V regulator is used, JP703=REG and JP704=REGAO by default.</td>
</tr>
<tr>
<td></td>
<td>AVDD</td>
<td></td>
<td></td>
<td></td>
<td>When REGAO from AK5522 is used, JP703=REG and JP704=REGAO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When jack is used, JP703=CON and JP704=REG-CON.</td>
</tr>
<tr>
<td>J704</td>
<td>DVDD</td>
<td>Yellow</td>
<td>+3.3V / +1.8V</td>
<td>AK5522 DVDD</td>
<td>3.3V regulator is used, JP705=3.3V and JP706=REG by default.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When 1.8V regulator is used, JP705=1.8V and JP706=REG.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When jack is used, JP706=CON.</td>
</tr>
<tr>
<td>J705</td>
<td>LVDD</td>
<td>Yellow</td>
<td>+3.3V</td>
<td>AK4432 LVDD</td>
<td>Regulator is used, JP707=REG.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When jack is used, JP707=short.</td>
</tr>
<tr>
<td>J706</td>
<td>D3.3V</td>
<td>Yellow</td>
<td>+3.3V</td>
<td>AK4118A, Logic IC power supply</td>
<td>Regulator is used, JP708=REG by default.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When jack is used, JP708=JACK short.</td>
</tr>
<tr>
<td>J708</td>
<td>GND</td>
<td>Black</td>
<td>0V</td>
<td>Ground</td>
<td>Should always be connected.</td>
</tr>
</tbody>
</table>

Table 1. Power supply line setting ( default : used the regulator )
(1-2) About jumper for power supply :
The roles of the jumper or the short resistance for each power supply supplied from the regulator are as follows.

Connection of the jumper for power supply :

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Comments</th>
<th>Default Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP701</td>
<td>AVDD-SEL1 Select 5.0V regulator or 3.3V regulator for AK5522 AVDD.</td>
<td>AVDD selector for AK5522: JP701=AV50V: 5.0V regulator is used. (default) JP701=A3,3V: 3.3V regulator is used.</td>
<td>A5.0V</td>
</tr>
<tr>
<td>JP702</td>
<td>AVDD-SEL2 Select regulator power supply or jack for AVDD.</td>
<td>AVDD for AK5522: JP702=REG: Regulator is used. (default) JP702=CON: Jack is used.</td>
<td>REG</td>
</tr>
<tr>
<td>JP703</td>
<td>DAC AVDD-SEL1 Select regulator power supply or jack for AK4432 AVDD.</td>
<td>AVDD selector for AK4432: JP703=REG: Regulator is used. (default) JP703=CON: Jack is used.</td>
<td>REG</td>
</tr>
<tr>
<td>JP704</td>
<td>DAC AVDD-SEL2 Select power supply DAC AVDD-SEL1 or REGAO from AK5522 for TVDD</td>
<td>AVDD for AK4432: JP704=REGAO: REGAO from AK5522 is used. (default) JP704=REG-CON: Regulator or Jack is used.</td>
<td>REGAO</td>
</tr>
<tr>
<td>JP705</td>
<td>DVDD-SEL1 Select regulator power supply or jack for DVDD.</td>
<td>DVDD selector for AK5522: JP705=3.3V: 3.3V regulator is used. (default) JP705=1.8V: 1.8V regulator is used.</td>
<td>3.3V</td>
</tr>
<tr>
<td>JP706</td>
<td>DVDD-SEL2 Select regulator power supply or jack for DVDD.</td>
<td>DVDD for AK5522: JP706=REG: Regulator is used. (default) JP706=CON: Jack is used.</td>
<td>REG</td>
</tr>
<tr>
<td>JP707</td>
<td>LVDD-SEL Select regulator power supply or jack for LVDD.</td>
<td>LVDDV for AK4432: JP707=REG: 3.3V regulator is used. (default) JP707=CON: Jack is used.</td>
<td>REG</td>
</tr>
<tr>
<td>JP708</td>
<td>D3.3V-SEL Select regulator power supply or jack for D3.3V.</td>
<td>D3.3V for AK4118A and Logic IC: JP708=REG: 3.3V regulator is used. (default) JP708=JACK: Jack is used.</td>
<td>REG</td>
</tr>
<tr>
<td>JP602</td>
<td>USB-BUS Select +12V(J701) or usb-bus.</td>
<td>No use.</td>
<td>Open</td>
</tr>
</tbody>
</table>

Table 2. Jumper for power supply
### Jumped pins settings

<table>
<thead>
<tr>
<th>No</th>
<th>Names</th>
<th>Default</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>JP103 DVDD-SEL</td>
<td>open</td>
<td>Select REGDO of AK5522. Open: DVDD of AK5522=3.0V-3.6V. (default) Short: DVDD of AK5522=1.7V-1.98V.</td>
</tr>
<tr>
<td>2</td>
<td>JP104 LOOP</td>
<td>1-pin short</td>
<td>No use.</td>
</tr>
<tr>
<td>10</td>
<td>JP301 DACMCLK-SEL</td>
<td>AD</td>
<td>Select input to AK4432 (U302) MCLK: JP301=AD; DAC-MCLK1 from PORT402. (default) JP301=EXT; EXT-MCLK from J401.</td>
</tr>
<tr>
<td>11</td>
<td>JP303 TX-SEL</td>
<td>COAX</td>
<td>Select output from AK4118A(U301): JP303=COAX: Output port is TX-COAX. (default) JP303=OPT: Output port is TX-OPT.</td>
</tr>
<tr>
<td>13</td>
<td>SW401 PORT401-SEL</td>
<td>1-pin short</td>
<td>Select PORT401: 1-2pin: PORT401 is OUTPUT to AK5522. (default) 2-3pin: PORT401 is INPUT to AK5522.</td>
</tr>
<tr>
<td>14</td>
<td>PORT402 MCLK-SEL</td>
<td>1-pin short</td>
<td>Select input / output to AK5522 (U101) MCLK 1-2pin: Select AK4118A (U301) (default) 3-4pin: Select PORT401 1-2pin. 5-6pin: Select with AK4432 (U302) and other port. 7-8pin: Select EXT-MCLK (J401)</td>
</tr>
<tr>
<td>15</td>
<td>PORT403 BICK-SEL</td>
<td>1-pin short</td>
<td>Select input / output to AK5522 (U101) BICK 1-2pin: Select AK4118A (U301) (default) 3-4pin: Select PORT401 1-2pin. 5-6pin: Select AK4432 (U302)</td>
</tr>
<tr>
<td>Number</td>
<td>PORT405</td>
<td>Jumper Pin Setting</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>---------</td>
<td>--------------------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 16     | LRCK-SEL| 1-2pin short       | Select input / output to AK5522 (U101) LRCK  
1-2pin: Select AK4118A.(U301) (default)  
3-4pin: Select PORT401 1-2pin.  
5-6pin: Select AK4432.(U302) |
| 17     | SDTO-SEL| 1-2pin short       | Select output to AK5522 (U101) SDTO  
1-2pin: Select AK4118A.(U301) (default)  
3-4pin: Select PORT401 1-2pin.  
5-6pin: Select AK4432.(U302) |

Table 3. Main board Jumper pin setting
[3] DIP switches settings

(3-1). Setting for SW301 (Sets AK4118A (U301) audio format and master clock setting)

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIF2</td>
<td>Set-up of DIF2 pin.</td>
<td>H</td>
</tr>
<tr>
<td>2</td>
<td>DIF1</td>
<td>Set-up of DIF1 pin.</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>DIF0</td>
<td>Set-up of DIF0 pin.</td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>OCKS1</td>
<td>Set-up of OCKS1 pin.</td>
<td>H</td>
</tr>
<tr>
<td>5</td>
<td>OCKS0</td>
<td>Set-up of OCKS0 pin.</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 4. SW301 Setting (AK4118A)

<table>
<thead>
<tr>
<th>Mode</th>
<th>DIF2 bit</th>
<th>DIF1 bit</th>
<th>DIF0 bit</th>
<th>DAUX</th>
<th>SDTO</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>24bit, Left justified</td>
<td>16bit, Right justified</td>
<td>I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>H/L</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>H/L</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>H/L</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>H/L</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>H/L</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>L/H</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>H/L</td>
<td>I</td>
<td>64-128fs</td>
<td>I</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>L/H</td>
<td>I</td>
<td>64-128fs</td>
<td>I</td>
</tr>
</tbody>
</table>

Table 5. Audio format (AK4118A)

<table>
<thead>
<tr>
<th>OCKS1 pin SW301_4</th>
<th>OCKS1 pin SW301_5</th>
<th>(X’tal)</th>
<th>MCKO1</th>
<th>MCKO2</th>
<th>fs (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OCKS0 pin SW301_5</td>
<td>OCKS0 pin SW301_5</td>
<td></td>
<td></td>
<td></td>
<td>default</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>256fs</td>
<td>256fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>256fs</td>
<td>256fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>512fs</td>
<td>512fs</td>
<td>256fs</td>
<td>48 kHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>128fs</td>
<td>128fs</td>
<td>64fs</td>
<td>192 kHz</td>
</tr>
</tbody>
</table>

Table 6. Master Clock Frequency Select (AK4118A)
(3-2). Setting for SW501 (Sets AK5522 (U101) )

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
</table>
| 1   | PSN         | Control mode select.  
L: Serial control mode.  
H: Parallel control mode. | H |
| 2   | CKS3        | Clock Mode Setting #3 | L |
| 3   | CKS2        | Clock Mode Setting #2 | H |
| 4   | CKS1        | Clock Mode Setting #1 | L |
| 5   | CKS0        | Clock Mode Setting #0 | L |
| 6   | SD          | Digital Filter Select. (PSN ="H")  
L: Sharp roll-off.  
H: Short delay sharp roll-off. | L |
| 7   | DIF         | Audio Data Format select.  
L: MSB justified.  
H: I2S compatible. | L |

Table 7. SW501 Setting

(3-3). Setting for SW502 (Sets AK4432 (U302) )

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
</table>
| 1   | PS          | Control mode select.  
L: Serial control mode.  
H: Parallel control mode. | H |
| 2   | I2CFIL      | I2C Interface mode select.  
L: Fast mode(400kHz).  
H: Fast mode plus(1MHz). | L |
| 3   | ACKS        | Auto setting mode select. (PS ="H")  
L: Manual setting mode.  
H: Auto setting mode. | H |
| 4   | DIF         | Audio Data Format select.  
L: MSB justified.  
H: I2S compatible. | L |

Table 8. SW502 Setting
Operation Mode (Parallel Control mode)

<table>
<thead>
<tr>
<th>Mode</th>
<th>CKS3 /SDA pin</th>
<th>CKS2 /SCL pin</th>
<th>CKS1 /TDM pin</th>
<th>Master /Slave</th>
<th>Stereo /TDM</th>
<th>MCLK</th>
<th>I/O</th>
<th>LRCK (fs) [kHz]</th>
<th>I/O</th>
<th>BICK</th>
<th>I/O</th>
<th>PLL Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Master</td>
<td>Stereo</td>
<td>512fs</td>
<td>I</td>
<td>8 - 54</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Master</td>
<td>Stereo</td>
<td>256fs</td>
<td>I</td>
<td>54 - 108</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Master</td>
<td>Stereo</td>
<td>256fs</td>
<td>I</td>
<td>8 - 54</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>Master</td>
<td>Stereo</td>
<td>128fs</td>
<td>I</td>
<td>108 - 216</td>
<td>O</td>
<td>64fs</td>
<td>O</td>
</tr>
<tr>
<td>4</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
<td>1024fs</td>
<td>I</td>
<td>8 - 32</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>768fs</td>
<td>I</td>
<td>8 - 48</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>512fs</td>
<td>I</td>
<td>8 - 54</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>384fs</td>
<td>I</td>
<td>48 - 96</td>
<td>I</td>
<td>≤ 128fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>256fs</td>
<td>I</td>
<td>54 - 108</td>
<td>I</td>
<td>≤ 128fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>192fs</td>
<td>I</td>
<td>96 - 192</td>
<td>I</td>
<td>≤ 64fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>128fs</td>
<td>I</td>
<td>108 - 216</td>
<td>I</td>
<td>≤ 64fs</td>
<td>I</td>
</tr>
<tr>
<td>5</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Slave</td>
<td>Stereo</td>
<td>384fs,</td>
<td>I</td>
<td>8 - 48</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>256fs</td>
<td>I</td>
<td>8 - 54</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td>6</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
<td>512fs</td>
<td>O</td>
<td>44,1,48</td>
<td>I</td>
<td>64fs</td>
<td>I</td>
</tr>
<tr>
<td>7</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
<td>256fs</td>
<td>O</td>
<td>44,1,48</td>
<td>I</td>
<td>64fs</td>
<td>I</td>
</tr>
<tr>
<td>8</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
<td>256fs</td>
<td>O</td>
<td>88,2,96</td>
<td>I</td>
<td>64fs</td>
<td>I</td>
</tr>
<tr>
<td>9</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Slave</td>
<td>Stereo</td>
<td>128fs</td>
<td>O</td>
<td>176,4,192</td>
<td>I</td>
<td>64fs</td>
<td>I</td>
</tr>
<tr>
<td>10</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
<td>512fs</td>
<td>O</td>
<td>44,1,48</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td>11</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>Slave</td>
<td>Stereo</td>
<td>256fs</td>
<td>O</td>
<td>44,1,48</td>
<td>I</td>
<td>≤ 256fs</td>
<td>I</td>
</tr>
<tr>
<td>12</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>Slave</td>
<td>Stereo</td>
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<td>O</td>
<td>88,2,96</td>
<td>I</td>
<td>≤ 128fs</td>
<td>I</td>
</tr>
<tr>
<td>13</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Slave</td>
<td>Stereo</td>
<td>128fs</td>
<td>O</td>
<td>176,4,192</td>
<td>I</td>
<td>≤ 64fs</td>
<td>I</td>
</tr>
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<td>14</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>TDMI</td>
<td>Slave</td>
<td>TDM</td>
<td>256fs</td>
<td>I</td>
<td>8 - 54</td>
<td>I</td>
<td>256fs</td>
<td>I</td>
</tr>
</tbody>
</table>

Table 9. Operation Mode Setting (Parallel Control mode)

Up="H", Down="L"

[SW503] (Power Down (PDN) for AK5522):
Power Down (PDN) Switch for AK5522
Reset AK5522 (U101) once by bring SW503 to “L” once upon power-up.
Keep “H” when AK5522 is in use; keep “L” when AK5522 is not in use.

[SW504] (Power Down (PDN) for AK4118A):
Power Down (PDN) Switch for AK4118A
Reset AK4118A (U201) once by bring SW504 to “L” once upon power-up.
Keep “H” when AK4118A is in use; keep “L” when AK4118A is not in use.

[SW505] (Power Down (PDN) for AK4432):
Power Down (PDN) Switch for AK4432
Reset AK4432 (U202) once by bring SW505 to “L” once upon power-up.
Keep “H” when AK4432 is in use; keep “L” when AK4432 is not in use.

[SW506] (Soft mute (SMUTE) for AK4432):
Soft mute (SMUTE) Switch for AK4432 in parallel control mode.
SW506 to “H” soft mute cycle is initiated.
Keep “L” when AK4432 is output mute releases.
[5] Register control (Serial control)
Evaluation Board and Control Software Settings

(1) Set-up the AKD5522-A by referring preceding chapters.
(2) Connect the evaluation board and PC with a USB cable.

The USB connection is recognized as HID (Human Interface Device) on the PC.

This connection can be checked in the device manager.

(3) Access the CD-ROM (labeled “AKD5522-A Evaluation Kit”) and execute “AK5522.exe” to open the control program. Click the “Port Reset” button to initialize the USB interface if the USB I/F box does not show “AKDUSBIF-B”.

(4) Begin evaluation by following the procedure below.

Figure 3. Startup Screen
Operation Overviews

Functions and Register map are controlled by this control software. These controls may be selected by the upper tabs.

Frequently used Buttons, such as the register initializing button “READ” and etc., are located outside of the switching tab window as shown below.

![Control Buttons in Main Window](image)

(1) [Port Reset]: Reset the USB port of the main board. This button must be pressed to initialize the USB port when unplugging/plugging the USB cable or when the USB port is not recognized correctly.

(2) [Write Default]: Initialize all registers of the AK5522.

(3) [All Write]: Executes write commands for all registers displayed.

(4) [All Read]: Executes read commands for all registers displayed.

(5) [Save]: Saves current register settings to a file.

(6) [Load]: Executes data write from a saved file.

(7) [All Req Write]: Opens “All Req Write” dialog box.

(8) [Sequence]: Opens “Sequence” dialog box.

(9) [Sequence (File)]: Opens “Sequence(File)” dialog box.

(10) [Close]: Quit the control software.
### Tab Functions

1. **[Function] Tab: Functions**

   Sequence operation and a setup of a register are executed with the function button arranged at the right side, and each button in a block diagram.

![Figure 5 “Function” Tab Window](image)

Path, dialog and various setting block: Executes a setup of the path and various functions. (Refer (1-1))

~ **Explanation of the color of a pass line** ~

Thick lines (blue, red) show that the paths are connected.

- thick line (blue): The path is connected and the power of block on this path is "OFF".
- thick line (red): The path is connected and the power of block on this path is "ON".
1-1. Path and Various Setting block
1-1-1. Path Setting

Register settings for clock sync domain and data source for input and output data ports of the AK5522 can be controlled by this window. The register map will be updated by setting in this window. (Refer to the AK5522 datasheet for register definitions)

Figure 6 [Path and Various Setting] Block

[LDO_ON] button : The power of ADC1 is controlled.
[PLL_OFF] button : The power of ADC2 is controlled.
[RST_N] button : The power of ADCM is controlled.
[LCH_OFF] button : The power of DAC1 is controlled.
[RCH_OFF] button : The power of DAC2 is controlled.
[HPF_Enable] button : The availability of HPF is controlled.
1-1-2. Gain Setting

The volume can be changed by writing a value in a dialog box. When writing a value in a dialog box, a configurable value is automatically selected and the written value is changed to the selected value. The slide bar moves to the value that is written in the dialog box. Use the mouse or arrow keys on the keyboard for fine adjustments.

Figure 7. Gain Slider
2. Register Map Tabs

Register write and read are available in this window. Each tab name shows register address range included in the tab window.

Each bit on the register map is a push-button switch. Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red). Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray).

Grayed out registers are Read-Only registers. They cannot be controlled. The registers which are not defined on the datasheet, “0” assigned bits and Reserved bits are indicated as “---”.

[Write] and [Read] buttons are shown on the right of the each address if the register is writable and readable. Read-Only registers has a [Read] button only and Reserved registers do not have these buttons.

Figure 8. Register Map Tab
2-1. [Write]: Data Write Dialog

![Register Write Window]

Figure 9. Register Write Window

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown above.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. By clicking the [All Check] button, all writable registers will be checked. Click [Write] to write the set values to the registers, or click [Close] to cancel this setting.

2-2. [Read]: Data Read

Click the [Read] button located on the right of the each corresponding address to execute a register read. The register map will be updated after executing the [Read] command.
Dialog Boxes

1. [Save Address of Register] Dialog

Click the [Save] button in the main window for save address setting dialog box.

![Save Address of Register Dialog]

Figure 10. [Save] Window

- [All Address] check box: When the [All Address] checkbox is checked, all register settings will be saved.
- [Start Address] edit box: When the [All Address] check box is not checked, the starts register address to save will be set.
- [End Address] edit box: When the [All Address] check box is not checked, the end register address to save will be set.
- [AK4432] check box: When the [AK4432] checkbox is checked, AK4432 settings will be saved.
- [OK] button: Selects a file to save and saves register settings.
- [Cancel] button: Cancel and finish this process.
2. **[All Register Write] Dialog**

Click the [All Reg Write] button in the main window to open register setting file window show below. Register setting files saved by the [Save] button may be applied.

![All Register Write Window](image)

**Figure 11. [All Reg Write] Window**

- **[Open (left)] button**: Selects a register setting file (*.akr) that was saved by [Save] in the main window.
- **[Write] button**: Executes register write with selected file setting.
- **[Help] button**: Opens a help window.
- **[Save] button**: Saves a register setting file assignment. File name is “*.mar”.
- **[Open (right)] button**: Opens a saved register setting file assignment “*.mar”.
- **[Close] button**: Closes the dialog box and finish the process.
- **[All Write] button**: Executes all register write. Selected files are executed in descending order.
- **[Start] button**: Start the register writing.
- **[Stop] button**: Stop the register writing.
- **[Interval time] edit box**: Set interval time to start next register setting file. (5msec ~ 10,000msec)
- **[Current No] edit box**: The file number which is being processed is displayed. (File number is assigned 1-10 from top to bottom.)
~ Operating Suggestions ~

1. Files saved by the [Save] button and opened by the [Open] button on the right of the dialog “*.mar” should be stored in the same folder.

2. Then register settings are changed by the [Save] button in the main window, re-read the file to reflect new register settings.
3. **[Sequence] Dialog**

Click the [Sequence] button in the main window to open register sequence setting dialog box. Register sequence can be set in this dialog box.

![Figure 12. [Sequence] Window](image)

**~Sequence Setting~**

Set register sequence according to the following process.

1. Select a command
   
   Use [Select] pull-down box to choose commands. Corresponding boxes will be valid.

   < Select items>
   
   - No use : Not using this address
   - Register : Register write
   - Reg_Mask : Register write (Masked)
   - Interval : Takes an interval
   - Stop : Pauses the sequence
   - End : Ends the sequence
2. Input sequence

[Address] : Data address
[Data] : Write data
[Mask] : Mask

This value “ANDed” with the write data becomes the input data. The bits which corresponding Mask bit = “0” are not changed. At this time, data read is not executed, and the storage data of this software is used. “Write Default” must be executed after power up the AK5522 or when the AK5522 is reset by the PDN pin since the storage data and register values are different.

This is the actual write data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[Interval] : Interval time

Valid boxes for each process command are shown below.
・No use : None
・Register : [ Address ], [ Data ], [ Interval ]
・Reg_Mask : [ Address ], [ Data ], [ Mask ], [ Interval ]
・Interval : [ Interval ]
・Stop : None
・End : None

~ Control Buttons ~

Functions of Control Button are shown below.

[DEL] button : Checked step is deleted.
[INS] button : The last deleted step is inserted to checked step.
[Start Step] select : Select start step.
   No.1 Step : Start from No.1 step.
   Checked Step : Start from checked step.
[Start] button : Executes the sequence.
[Stop] button : Stops the sequence.
[Help] button : Opens a help window.
[Save] button : Saves sequence settings as a file. The file name is “*.aks”.
[Open] button : Opens a sequence setting file “*.aks”.
[Close] button : Closes the dialog box and finishes the process.

~ Stop of the Sequence ~

When “Stop” is selected in the sequence, the process is paused at this step and restart step number is checked. It starts again from the checked step by clicking the [Start] button. When the process at the end of sequence is finished, “Step No.1” of [start step] is selected automatically.
4. **[Sequence by *.aks file] Dialog**

Click the [Sequence (File)] button to open sequence setting file dialog box shown below. Files saved in the “Sequence setting dialog” can be applied in this dialog.

![Sequence by *.aks file](image)

**Figure 13. [Sequence (File)] Window**

- **[Open (left)] button**: Opens a sequence setting file (*.aks) that was saved by [Sequence] in the main window.
- **[Start] button**: Executes the sequence by the setting of selected file.
- **[Start All] button**: Executes all sequence settings. Selected files are executed in descending order.
- **[Stop] button**: Stops the sequence process.
- **[Help] button**: Opens a help window.
- **[Save] button**: Saves a sequence setting file assignment. The file name is “*.mas”.
- **[Open (right)] button**: Opens a saved sequence setting file assignment “*.mas”.
- **[Close] button**: Closes the dialog box and finishes the process.
# Measurement Results

## Measurement condition
- **Measurement unit**: Audio Precision, SYS-2722(00095)
- **MCKI**: 512fs/256fs/128fs (24.576MHz)
- **fs**: 48kHz / 96kHz / 192kHz
- **Bit**: 24bit
- **Measurement Mode**: Ext Slave Mode
- **Power Supply**: AVDD=5.0V (Regulator), DVDD=3.3V (Regulator)
- **Input Frequency**: 1kHz
- **Measurement Frequency**: 20 ~ 20kHz @48kHz / 20 ~ 40kHz @96kHz / 20 ~ 40kHz @192kHz
- **Temperature**: Room

## Measurement Results

1. Full Differential Inputs

<table>
<thead>
<tr>
<th></th>
<th>Result (dB)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S/(N+D)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fs = 48kHz (-1dBFS)</td>
<td>97.9</td>
<td>97.6</td>
</tr>
<tr>
<td>fs = 96kHz (-1dBFS)</td>
<td>98.0</td>
<td>97.9</td>
</tr>
<tr>
<td>fs = 192kHz (-1dBFS)</td>
<td>97.9</td>
<td>97.8</td>
</tr>
<tr>
<td><strong>DR</strong></td>
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<td></td>
</tr>
<tr>
<td>fs = 48kHz (-60dBFS, A-Weighted)</td>
<td>108.1</td>
<td>107.9</td>
</tr>
<tr>
<td>fs = 96kHz (-60dBFS, A-Weighted)</td>
<td>107.6</td>
<td>107.5</td>
</tr>
<tr>
<td><strong>S/N</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fs = 48kHz (A-weighted)</td>
<td>108.0</td>
<td>108.0</td>
</tr>
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</table>
fs = 48 kHz
AK5522 FFT (-1dBFS Input)
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, fin=1kHz

Figure 14. FFT (-1dBFS Input)

AK5522 FFT (-60dBFS Input)
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, fin=1kHz

Figure 15. FFT (-60dBFS Input)
fs = 48 kHz
AK5522 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, fin=1kHz

Figure 16. FFT (No Signal Input)

AK5522 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, fin=1kHz

Figure 17. THD+N vs. Input Level
fs = 48 kHz
AK5522 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, -1dBFS Input

Figure 18. THD+N vs. Input Frequency

AK5522 Linearity
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, fin=1kHz

Figure 19. Linearity
fs = 48 kHz
AK5522 Frequency Response
AVDD=5.0V, DVDD=3.3V, MCLK=512fs, -1dBFS input

Figure 20. Frequency Response
$f_s = 96$ kHz

AK5522 FFT (-1dBFS Input)

AVDD=5.0V, DVDD=3.3V, MCLK=256fs, $f_{in}$=1kHz

Figure 21. FFT (-1dBFS Input)

AK5522 FFT (-60dBFS Input)

AVDD=5.0V, DVDD=3.3V, MCLK=256fs, $f_{in}$=1kHz

Figure 22. FFT (-60dBFS Input)
fs = 96 kHz
AK5522 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, MCLK=256fs, fin=1kHz

Figure 23. FFT (No Signal Input)
AK5522 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, MCLK=256fs, fin=1kHz

Figure 24. THD+N vs. Input Level
fs = 96 kHz
AK5522 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, MCLK=256fs, -1dBFS Input

Figure 25. THD+N vs. Input Frequency

AK5522 Linearity
AVDD=5.0V, DVDD=3.3V, MCLK=256fs, fin=1kHz

Figure 26. Linearity
fs = 96 kHz
AK5522 Frequency Response
AVDD=5.0V, DVDD=3.3V, MCLK=256fs, -1dBFS Input

Figure 27. Frequency Response
fs = 192 kHz
AK5522 FFT (-1dBFS Input)
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, fin=1kHz

Figure 28. FFT (-1dBFS Input)

AK5522 FFT (-60dBFS Input)
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, fin=1kHz

Figure 29. FFT (-60dBFS Input)
fs = 192 kHz
AK5522 FFT (No Signal Input)
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, fin=1kHz

Figure 30. FFT (No Signal Input)

AK5522 THD+N vs. Input Level
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, fin=1kHz

Figure 31. THD+N vs. Input Level
fs = 192 kHz
AK5522 THD+N vs. Input Frequency
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, -1dBFS Input

Figure 32. THD+N vs. Input Frequency

AK5522 Linearity
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, fin=1kHz

Figure 33. Linearity
$fs = 192$ kHz
AK5522 Frequency Response
AVDD=5.0V, DVDD=3.3V, MCLK=128fs, -1dBFS Input

Figure 34. Frequency Response
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