GENERAL DESCRIPTION
The AKD5556-B is an evaluation board for AK5556, which is 32bit, 8k – 768kHz, 6ch ADC. The AKD5556-B has the analog input circuit and a digital audio interface transmitter (DIT). In addition, the regulators and crystal oscillator on the board generate the necessary power and clock for the ICs. The AKD5556-B can be easily connected to your audio system.

Ordering guide
AKD5556-B -- Evaluation board for AK5556
(A USB I/F BOX and control software for Windows 10 computer are included in this package.)

FUNCTION
• Onboard Voltage Regulators: Operate only with ±15V power supplies.
• Onboard System Clocks: No clock source is required.
  \[fs=48kHz, 96kHz, 192kHz\] are available.
• Analog Input: Differential input (CANNON)
• Digital Output: PCM, DSD (Header pins) and digital audio interface (BNC and Optical)
• Operation Mode Setting: Register control and pin control are available.
  (note: Default setting of the board is register control with I2C)

Figure 1. AKD5556-B Block Diagram
* Circuit diagram and PCB layout are attached at the end of this manual.
Figure 2. Layout of Connectors and Switches

*AKD5556-B Evaluation Board
Overview of Connectors and Switches

(1) U100 (AK5556)
    32bit,8k - 768kHz,6ch A/D Converter.

(2) J200, J201, J300, J301, J400, J401 (Cannon Connector)
    Differential Analog Signal Input.

(3) J600 (BNC Connector)
    Digital Audio Interface Coaxial Output.

(4) PORT600 (Optical Connector)
    Digital Audio Interface Optical Output.

(5) J1000, J1001, J1002, J1003, J1004, J1005, J1006, J1007, J1008, J1009 (Banana Jack)
    Power Supply Input.

(6) PORT800, PORT801 (pin header)
    Clocks Input/Output and PCM data Output and TDM data Input.
    (MCLK, BICK, LRCK, SDTO1, SDTO2, SDTO3, SDTO4, TDMIN).

(7) PORT802, PORT803 (pin header)
    DSD data and Clock Output.

(8) PORT700 (Pin Header)
    I2C or 3-wire serial signals input/output.

(9) U600 (AK4118A)
    Generate system clocks. Convert A/D data as digital audio interface format.

(10) SW800 (Toggle switch)
    Set PDN of AK5556.

(11) SW801 (Toggle switch)
    Set PDN of AK4118A.

(12) SW802, SW803, SW804 (Dip switch)
    Set pin logical Level of AK5556 input pins.

(13) SW600 (Dip switch)
    Set input data format and output clock frequency of AK4118A.

(14) J800 (BNC Connector)
    External Master Clock Input (MCLK).

(15) T1001, T1002, T1003, T1004, T1005
    Regulator for Power supply of AK5556, AK4118A, Logic Circuit.
    T1001 : Regulated AVDD, VBIAS (5.0V) from +15V.
    T1002 : Regulated VCC1, VCC2 (5.0V) from +15V.
    T1003 : Regulated TVDD (3.3V) from +5V.
    T1004 : Regulated TVDD, VDD18 (1.8V) from +5V
    T1005 : Regulated D33V (3.3V) from +5V.
Evaluation Board Setting

- Operation sequence

  [1] Power Supply Path Settings

  [2] Clocks and Data Path Settings

  [3] Control Mode Settings

  [4] Analog Input Settings

  [5] Slave Mode/Master Mode Setting

  [6] AK4118A Settings

  [7] AK5556 Setting Tables

  [8] Start-up Sequence
[1] Power supply Path settings

(1-1) Power supply Jacks setting :

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Voltage (Typ)</th>
<th>Supply Destination</th>
<th>Comments</th>
<th>Default Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1000</td>
<td>+15V</td>
<td>Green</td>
<td>+15V</td>
<td>Regulator and Op-amps</td>
<td>Should always be connected.</td>
</tr>
<tr>
<td>J1001</td>
<td>-15V</td>
<td>Blue</td>
<td>-15V</td>
<td>Regulator and Op-amps</td>
<td>Should always be connected.</td>
</tr>
<tr>
<td>J1004</td>
<td>AVDD</td>
<td>Red</td>
<td>+5.0V</td>
<td>AK5556 AVDD and VREFH</td>
<td>Optional Input.</td>
</tr>
<tr>
<td>J1005</td>
<td>VBIAS</td>
<td>Red</td>
<td>+5.0V</td>
<td>Source of Analog Input Signal Common Level</td>
<td>Optional Input. The signal common level becomes VBIAS.</td>
</tr>
<tr>
<td>J1009</td>
<td>VCC</td>
<td>Red</td>
<td>+5.0V</td>
<td>Regulator for AK5556 TVDD and VDD18 and Peripheral Logic IC.</td>
<td>Optional Input.</td>
</tr>
<tr>
<td>J1006</td>
<td>TVDD</td>
<td>Orange</td>
<td>+1.8 or +3.3V</td>
<td>AK5556 TVDD and Peripheral Logic IC.</td>
<td>Optional Input.</td>
</tr>
<tr>
<td>J1007</td>
<td>VDD18</td>
<td>Orange</td>
<td>+1.8V</td>
<td>AK5556 VDD18</td>
<td>Optional Input.</td>
</tr>
<tr>
<td>J1008</td>
<td>D3.3V</td>
<td>Orange</td>
<td>+3.3V</td>
<td>AK4118A VDD and Peripheral Logic IC.</td>
<td>Optional Input.</td>
</tr>
<tr>
<td>J1002</td>
<td>AVSS</td>
<td>Black</td>
<td>0V</td>
<td>Analog ground</td>
<td>Should always be connected</td>
</tr>
<tr>
<td>J1003</td>
<td>DVSS</td>
<td>Black</td>
<td>0V</td>
<td>Digital ground</td>
<td>Should always be connected</td>
</tr>
</tbody>
</table>

Table 1-1. Power supply Jacks

In the default settings of the board, the onboard regulators supply the power the AK5556 and peripheral ICs. If you want to use external power supplies, set the jumpers as described on the next table.

(1-2) The Power Supply Source Selection :

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1007</td>
<td>AVDD1 Select AVDD1 source.</td>
<td>R1007=short, R1008=open : Regulator output. (default)</td>
</tr>
<tr>
<td>R1008</td>
<td></td>
<td>R1007=short, R1008=short : Jack is used.</td>
</tr>
<tr>
<td>R1009</td>
<td>VBIAS Select VBIAS source.</td>
<td>R1009=short, R1010=open : Regulator output. (default)</td>
</tr>
<tr>
<td>R1010</td>
<td></td>
<td>R1009=short, R1010=short : Jack is used.</td>
</tr>
<tr>
<td>R1011</td>
<td>VCC1, VCC2 Select VCC source.</td>
<td>R1011=short, R1012=short : Regulator output. (default)</td>
</tr>
<tr>
<td>R1012</td>
<td></td>
<td>R1011=short, R1012=short : Jack is used.</td>
</tr>
<tr>
<td>JP1000</td>
<td>TVDD-VSEL Select regulator voltage for TVDD.</td>
<td>JP1000=3.3V : 3.3V regulator. (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP1000=1.8V : 1.8V regulator.</td>
</tr>
<tr>
<td>JP1001</td>
<td>TVDD-SEL Select TVDD source.</td>
<td>JP1001=REG : Regulator. (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP1001=JACK : Jack input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP1002=JACK : Jack input.</td>
</tr>
<tr>
<td>JP1003</td>
<td>D33V-SEL Select power supply source for peripheral ICs.</td>
<td>JP1003=REG : Regulator output. (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP1003=JACK : Jack input.</td>
</tr>
<tr>
<td>JP1004</td>
<td>VSS-SEL Select connection / separation between analog ground and digital ground.</td>
<td>JP1004=short: Connect analog ground AVSS and DVSS. (default)</td>
</tr>
</tbody>
</table>

Table 1-2. Jumper for power supply Setting
When you want to operate the IO pins of AK5556 at 1.8V, turn off the internal LDO and supply 1.8V to TVDD pin and VDD18 pin.

<table>
<thead>
<tr>
<th>LDOE SW803-1</th>
<th>LDO</th>
<th>VDD18 pin Status</th>
<th>TVDD pin Power Supply Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>OFF</td>
<td>External Power Supply Input 1.7 - 1.98V</td>
<td>1.7 - 1.98V</td>
</tr>
<tr>
<td>H</td>
<td>ON</td>
<td>LDO Power Output</td>
<td>3.0 - 3.6V default</td>
</tr>
</tbody>
</table>

Table 1-3. Internal LDO Setting (AK5556)
[2] Clock and Data path settings

(2-1) Connecters for Clocks and Data

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Default Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORT800</td>
<td>LRCK</td>
<td>LRCK Input or Output</td>
</tr>
<tr>
<td></td>
<td>BICK</td>
<td>BICK Input or Output</td>
</tr>
<tr>
<td></td>
<td>MCLK</td>
<td>MCLK Input</td>
</tr>
<tr>
<td>PORT801</td>
<td>SDTO1</td>
<td>CH1 and CH2 A/D Data Output</td>
</tr>
<tr>
<td></td>
<td>SDTO2</td>
<td>CH3 and CH4 A/D Data Output</td>
</tr>
<tr>
<td></td>
<td>SDTO3</td>
<td>CH5 and CH6 A/D Data Output</td>
</tr>
<tr>
<td></td>
<td>SDTO4</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>TDMIN</td>
<td>TDM Data Input</td>
</tr>
<tr>
<td>PORT802</td>
<td>DSDOL1</td>
<td>CH1 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>DSDOR1</td>
<td>CH2 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>DSDOL2</td>
<td>CH3 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>DSDOR2</td>
<td>CH4 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PORT803</td>
<td>DSDOL3</td>
<td>CH5 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>DSDOR3</td>
<td>CH6 DSD Data Output</td>
</tr>
<tr>
<td></td>
<td>DSDOL4</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>DSDOR4</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>DCLK</td>
<td>DSD Clock Output</td>
</tr>
<tr>
<td>PORT600</td>
<td>TX-OPT</td>
<td>Digital Audio Interface Output (Optical Connector)</td>
</tr>
<tr>
<td>J600</td>
<td>TX-COAX</td>
<td>Digital Audio Interface Output (BNC Connector)</td>
</tr>
</tbody>
</table>

Table 2-1. Connecters for Clocks and Data
(2-2) **Jumper Setting for Clocks and Data**

<table>
<thead>
<tr>
<th>Names</th>
<th>Functions</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP600</td>
<td>TXDATA-SEL</td>
<td>Select output connector for the digital audio interface TX data from AK4118A.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COAX: BNC (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OPT: Optical Connector</td>
</tr>
<tr>
<td>JP801</td>
<td>BICK-SEL</td>
<td>Select clock source for BICK.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIT: AK4118A output (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PORT: Pin Header PORT800-BICK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND: Connected to DVSS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open: No signal</td>
</tr>
<tr>
<td>JP802</td>
<td>LRCK-SEL</td>
<td>Select clock source for LRCK.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIT: AK4118A output (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PORT: Pin Header PORT800-LRCK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND: Connected to DVSS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open: No signal</td>
</tr>
<tr>
<td>PORT807</td>
<td>BICK-PHASE</td>
<td>Select BICK polarity.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>THR: Non-inverted (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>INV: Inverted</td>
</tr>
<tr>
<td>JP803</td>
<td>SDTO_SEL</td>
<td>Select A/D data channel inputting to digital interface transmitter (AK4118A).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDTO1: SDTO1 pin, Channel 1&amp;2 (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDTO2: SDTO2 pin, Channel 3&amp;4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDTO3: SDTO3 pin, Channel 5&amp;6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDTO4: -</td>
</tr>
<tr>
<td>JP804</td>
<td>TDMI-SEL</td>
<td>Select TDMIN input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open: No signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Short: Pin Header PORT801-TDMIN (default)</td>
</tr>
<tr>
<td>JP800</td>
<td>MCLK-SEL</td>
<td>Select clock source for MCLK of AK5556.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DIT: AK4118A output (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PORT: Pin Header PORT800-MCLK input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXT: External MCLK (J800 EXT) input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND: Connected to DVSS</td>
</tr>
<tr>
<td>JP810</td>
<td>EXT-T</td>
<td>Terminating External MCLK.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open: Not terminate (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Short: Terminating with 51Ω</td>
</tr>
</tbody>
</table>

**Table 2-2. Jumper Settings for Clocks and Data**
[3] Control Mode Settings

AK5556 can be controlled by pins or registers. The pin control mode is called parallel control mode in the AK5556 datasheet. The register control mode is called serial control mode. The register access is made by I2C bus or 3-wire serial bus. The setting method for each control mode is described below. The board default setting is I2C bus mode. If you use parallel control mode or 3-wire serial control mode, change the DIP switch and jumper settings.

<table>
<thead>
<tr>
<th>I2C pin SW803-4</th>
<th>PS pin SW803-10</th>
<th>Control Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>3-wire Serial</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>3-wire Serial</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>I2C Bus</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Parallel</td>
</tr>
</tbody>
</table>

Table 3-1. Control Mode Select (AK5556)

(3-1) I2C Bus Control Mode < default >

Switch Settings

Set sub-address by CAD0-I2C bit and CAD1 bit.

Figure 3-1-1. Switch Settings for I2C Bus control mode

The default control mode for the board is I2C bus mode.
Registers can be set using the included USB I/F BOX and control software.
Connect the flat cable from USB I/F BOX to PORT700. And connect USB I/F BOX to PC by USB cable in I2C bus mode.
(3-2) 3-wire Serial Bus Control Mode

Switch Setting

Set chip address by CAD0-SPI bit and CAD1 bit.

Figure 3-2-1. Switch Settings for 3-wire serial bus control mode

The USB I/F BOX and control software don’t support 3-wire serial bus control mode. When controlling the board by 3-wire serial bus, connect the CSN, CCLK and CDTI signals to header pins of PORT700.

![Port Assignments](image)

Figure 3-2-2. The pin assignments of PORT700

Registers can be set using the included USB I/F BOX and control software. Connect the flat cable from USB I/F BOX to PORT700. And connect USB I/F BOX to PC by USB cable. In 3-wire serial bus mode.
(3-3) Parallel Control Mode

Switch Settings

In parallel control mode, set the operation mode with the DIP switches.
USB I/F BOX and control software are not used.

Figure 3-3-1. Switch Settings for Parallel Control mode

Differential signals can be connected to the cannon connectors. The table below shows the relationship between channel number and connector number.

<table>
<thead>
<tr>
<th>ADC Channel</th>
<th>AIN1</th>
<th>AIN2</th>
<th>AIN3</th>
<th>AIN4</th>
<th>AIN5</th>
<th>AIN6</th>
</tr>
</thead>
<tbody>
<tr>
<td>6ch</td>
<td>J200</td>
<td>J201</td>
<td>J300</td>
<td>J301</td>
<td>J400</td>
<td>J401</td>
</tr>
</tbody>
</table>

**Table 4-1. Differential Analog Signal Input Cannon Connector**

Cannon Connectors (J200, J201, J300, J301, J400, J401) : Differential analog input signals for AK5556 Analog input Circuit :

![Analog Input Circuit Diagram]

**Figure 4-1. Analog Input Circuit**
[5] Slave Mode/Master Mode Setting

(5-1) Slave Mode (Default)

The default setting for the board is slave mode. The MCLK, LRCK and BICK are supplied from AK4118A (DIT) on the board to AK5556.

![Switch and Jumper Settings for Slave Mode](image)

Figure 5-1. Switch and Jumper Settings for Slave Mode

(5-2) Master Mode

Set the DIP switch SW602-5 to “H” and select “PORT” in PORT801, PORT802 when using in master mode. LRCK and BICK are output to PORT800 and PORT801 together with SDTO. Jumper PORT800 selects the MCLK input connector. The “PORT” is the header pin PORT800 and the “EXT” is the BNC J800.

![Switch and Jumper Settings for Master Mode](image)

Figure 5-2. Switch and Jumper Settings for Master Mode
[6] AK4118A settings

The onboard AK4118A converts A/D data to digital audio interface format. Select the data format with the DIP switch SW600.

![Diagram of SW600 switch](image)

Figure 6. SW400 Assignment (AK4118A)

### (3-1). Setting for SW600 (Sets AK4118A (U4) audio format and master clock setting)

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIF2</td>
<td>DIT input and output data format select</td>
<td>H</td>
</tr>
<tr>
<td>2</td>
<td>DIF1</td>
<td>DIT input and output data format select</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>DIF0</td>
<td>DIT input and output data format select</td>
<td>H</td>
</tr>
<tr>
<td>4</td>
<td>OCKS1</td>
<td>System clocks frequency select</td>
<td>H</td>
</tr>
<tr>
<td>5</td>
<td>OCKS0</td>
<td>System clocks frequency select</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 6-1. SW600 Setting (AK4118A)

### Table 6-2. Audio format (AK4118A)

In the default settings of the board, the AK4118A generate the system clocks (MCLK, LRCK and BICK) and supply them to AK5556. The AK4118A supports up to fs=192kHz.

<table>
<thead>
<tr>
<th>Mode</th>
<th>DIF2 SW600_1</th>
<th>DIF1 SW600_2</th>
<th>DIF0 SW600_3</th>
<th>DAUX input from AK5556</th>
<th>SDTO output to COAX, OPT</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>16bit, Right justified</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>24bit, Left justified</td>
<td>18bit, Right justified</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>20bit, Right justified</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>24bit, Left justified</td>
<td>24bit, Right justified</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>64fs</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>24bit, I2S</td>
<td>24bit, I2S</td>
<td>L/H</td>
<td>64fs</td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>1</td>
<td>64-128fs</td>
</tr>
<tr>
<td>7</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>24bit, I2S</td>
<td>24bit, I2S</td>
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Table 6-2. Audio format (AK4118A)

If you want higher fs than 192kHz, connect external clocks to pin headers or connectors and set the jumpers. See the Table 2-2.
7] AK5556 setting tables

(7-1) Serial Control mode (I2C bus)

The AK5556 operation modes are set by the control software in I2C control mode.

![Figure 7-1. Control Software Main Window (AK5556)](image)

Register data is indicated on the register map. Each bit on the register map is a push-button switch. Button DOWN with red lettering indicates “1” and button UP with blue lettering indicates “0”. Buttons with “---” are undefined in the datasheet.

- **PW6-1**: Power Down control for channel 6-1
  - 0: Power OFF
  - 1: Power ON (default)

- **RSTN**: Internal Timing Reset
  - 0: Reset. All registers are not initialized.
  - 1: Normal Operation (default)
- MONO2-1: Channel Summation Select

<table>
<thead>
<tr>
<th>MONO2 bit</th>
<th>MONO1 bit</th>
<th>Data on Slot</th>
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Figure 7-1. Slot Data Assign (AK5556)

- HPFE: High Pass Filter Enable
  0: High Pass Filter OFF
  1: High Pass Filter ON (default)
### Table 7-1-2. Data Interface mode setting

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<tr>
<th>No</th>
<th>Multiplex Mode</th>
<th>Speed Mode</th>
<th>TDM1</th>
<th>TDM0</th>
<th>MSN SW802-5</th>
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<th>DFTO</th>
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- DIF1-0: Audio Data Format Modes Select (default = 00b)
- TDM1-0: TDM Modes Select (default = 00b)
• CKS3-0: Sampling Speed Mode and MCLK Frequency Select

In default setting for the board, AK4118A supplies LRCK and MCLK to AK5556. The LRCK (fs) is 48kHz and the MCLK is 512fs. When using the board in default settings, set CKS3-0 bits to "0000b".

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<td>1</td>
<td>0</td>
<td>0</td>
<td>L</td>
<td>64fs</td>
<td>Hex Speed Mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>H</td>
<td>1024fs</td>
<td>Normal Speed Mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>L</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>H</td>
<td>Auto</td>
<td>8kHz ≤ fs ≤ 216kHz</td>
</tr>
</tbody>
</table>

Table 7-1-3. Speed mode and MCLK Frequency setting

• SLOW: Slow Roll-off Filter Select
• SD: Short Delay Filter Select

<table>
<thead>
<tr>
<th>SD bit</th>
<th>SLOW bit</th>
<th>Filter Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Sharp Roll-off Filter</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Slow Roll-off Filter</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Short Delay Sharp Roll-off Filter</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Short Delay Slow Roll-off Filter</td>
</tr>
</tbody>
</table>

Table 7-1-4. Digital Filter Select: PCM Mode

• DP: DSD Mode Select
0: PCM mode (default)
1: DSD mode
• DSDSEL1-0: Select the Frequency of DCLK (DSD Clock)

<table>
<thead>
<tr>
<th>DSDSEL1</th>
<th>DSDSEL0</th>
<th>Frequency Mode</th>
<th>DSD Sampling Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>64fs</td>
<td>fs=32kHz, fs=44.1kHz, fs=48kHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>128fs</td>
<td>2.048MHz, 2.8224MHz, 3.072MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>256fs</td>
<td>4.096MHz, 5.6448MHz, 6.144MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-</td>
<td>Reserved, Reserved, Reserved</td>
</tr>
</tbody>
</table>

Table 7-1-5. DSD Sampling Frequency Select

• DCKB: Polarity of DCLK
  0: DSD data is output from DCLK Falling Edge (default)
  1: DSD data is output from DCLK Rising Edge

• PMOD: DSD Phase Modulation Mode
  0: Not Phase Modulation mode (default)
  1: Phase Modulation mode

• DCKS: Master Clock Frequency Select at DSD mode
  0: 512fs (default)
  1: 768fs

• TST7-0: Test register.
  Must be “0”

• TRST: Test register
  Must be “0”
(7-2) Parallel Control mode (DIP Switches)

The AK5556 operation modes are set by the DIP switches in parallel control mode.

![DIP Switch Diagram]

Figure 7-2. DIP Switches for AK5556 Operation Settings

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TEST</td>
<td>TEST Enable. Must be “L”.</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>PW0</td>
<td>Power and Summation mode setting. See Table 7-2-4. ~ Table 7-2-5.</td>
<td>H</td>
</tr>
<tr>
<td>3</td>
<td>PW1</td>
<td>Power and Summation mode setting. See Table 7-2-4. ~ Table 7-2-5.</td>
<td>H</td>
</tr>
<tr>
<td>4</td>
<td>PW2</td>
<td>Power and Summation mode setting. See Table 7-2-4. ~ Table 7-2-5.</td>
<td>H</td>
</tr>
</tbody>
</table>
| 5   | MSN         | Master/Slave select.  
L: Slave Mode  
H: Master Mode | L |

Table 7-2-1. SW802 assignment

<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
</table>
| 1   | LDOE        | LDO Enable  
L: LDO Disable  
H: LDO Enable | H |
| 2   | ODP         | Output Data Placement Select. See Table 7-2-4. ~ Table 7-2-5. | L |
| 3   | HPFE/DCKS   | High Pass Filter Enable in PCM mode  
L: HPF Disable  
H: HPF Enable  
Master Clock Frequency select in DSD Mode  
L: 512fs  
H: 768fs | H |
| 4   | I2C         | Control mode select | H |
| 5   | TDM0        | TDM Interface Format select #0 See Table 7-2-7. | L |
| 6   | TDM1        | TDM Interface Format select #1 See Table 7-2-7. | L |
| 7   | DIF1/DSDSEL1 | Audio Data Format select in PCM Mode  
DSD Sampling Rate Control in DSD Mode See Table 7-2-7. | L |
| 8   | DIF0/DSDSEL0 | Audio Data Format select in PCM Mode  
DSD Sampling Rate Control in DSD Mode See Table 7-2-7. | H |
| 9   | DP          | DSD Mode Enable  
L: PCM Mode  
H: DSD Mode | L |
<p>| 10  | PSN         | Control mode select | L |</p>
<table>
<thead>
<tr>
<th>No.</th>
<th>Switch Name</th>
<th>Function</th>
<th>default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAD0-SPI</td>
<td>Chip Address0 Pin in 3-wire serial control mode.</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>CAD0-I2C</td>
<td>Chip Address0 Pin in I2C bus serial control mode.</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>CAD1</td>
<td>Chip Address1 Pin in I2C bus or 3-wire serial control mode.</td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>CKS0</td>
<td>Clock Mode Setting #0 See Table 7-2-6.</td>
<td>L</td>
</tr>
<tr>
<td>5</td>
<td>CKS1</td>
<td>Clock Mode Setting #1 See Table 7-2-6.</td>
<td>H</td>
</tr>
<tr>
<td>6</td>
<td>CKS2</td>
<td>Clock Mode Setting #2 See Table 7-2-6.</td>
<td>H</td>
</tr>
<tr>
<td>7</td>
<td>CKS3</td>
<td>Clock Mode Setting #3 See Table 7-2-6.</td>
<td>L</td>
</tr>
</tbody>
</table>
| 8   | SLOW/DCKB   | Slow Roll-OFF Digital Filter select in PCM Mode Polarity of DCLK in DSD Mode  
L: Not-Invert  
H: Invert | See Table 7-2-9. L |
| 9   | SD/PMOD     | Short Delay Digital Filter select in PCM Mode  
DSD Phase Modulation Mode select in DSD Mode  
L: Normal  
H: Phase Modulation | See Table 7-2-9. L |
| 10  | NC          | -        |         |

Table 7-2-3. SW804 assignment
- PW2-0: Power Down control for channel 6-1 (default=“HHH”)

ODP pin = “L”

**Table 7-2-4. Channel Power & Mono Mode Select (ODP pin = “L”) (AK5556)**

<table>
<thead>
<tr>
<th>PW2 pin SW802_4</th>
<th>PW1 pin SW802_3</th>
<th>PW0 pin SW802_2</th>
<th>Ch6</th>
<th>Ch5</th>
<th>Ch4</th>
<th>Ch3</th>
<th>Ch2</th>
<th>Ch1</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

**Default**

**Table 7-2-4-1. Channel Power ON/OFF Select (ODP pin = “L”) (AK5556)**

<table>
<thead>
<tr>
<th>PW2 pin SW802_4</th>
<th>PW1 pin SW802_3</th>
<th>PW0 pin SW802_2</th>
<th>Slot 6</th>
<th>Slot 5</th>
<th>Slot 4</th>
<th>Slot 3</th>
<th>Slot 2</th>
<th>Slot 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Not Available</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Not Available</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>(CH5+6) /2</td>
<td>(CH5+6) /2</td>
<td>(CH3+4) /2</td>
<td>(CH3+4) /2</td>
<td>(CH1+2) /2</td>
<td>(CH1+2) /2</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>All “0”</td>
<td>All “0”</td>
<td>CH4</td>
<td>CH3</td>
<td>CH2</td>
<td>CH1</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>CH6</td>
<td>All “0”</td>
<td>CH4</td>
<td>CH3</td>
<td>CH2</td>
<td>CH1</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>All “0”</td>
<td>CH5</td>
<td>CH4</td>
<td>CH3</td>
<td>CH2</td>
<td>CH1</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>CH6</td>
<td>CH5</td>
<td>CH4</td>
<td>CH3</td>
<td>CH2</td>
<td>CH1</td>
</tr>
</tbody>
</table>

**Default**

**Table 7-2-4-2. Mono Mode Select (ODP pin = “L”) (AK5556)**
ODP pin = “H”

Table 7-2-5. Channel Power & Mono Mode Select (ODP pin = “H”) (AK5556)

<table>
<thead>
<tr>
<th>PW2 pin SW802_4</th>
<th>PW1 pin SW802_3</th>
<th>PW0 pin SW802_2</th>
<th>Ch6</th>
<th>Ch5</th>
<th>Ch4</th>
<th>Ch3</th>
<th>Ch2</th>
<th>Ch1</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

Table 7-2-5-1. Channel Power ON/OFF Select (ODP pin = “H”) (AK5556)

<table>
<thead>
<tr>
<th>PW2 pin SW802_4</th>
<th>PW1 pin SW802_3</th>
<th>PW0 pin SW802_2</th>
<th>Slot 6</th>
<th>Slot 5</th>
<th>Slot 4</th>
<th>Slot 3</th>
<th>Slot 2</th>
<th>Slot 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
<td>All “0”</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH3+4) /2</td>
<td>(CH1+2) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>CH6</td>
<td>CH5</td>
<td>CH4</td>
<td>CH3</td>
<td>CH2</td>
<td>CH1</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH3+4) /2</td>
<td>(CH1+2) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>All “0” or TDMIN</td>
<td>(CH5+6) /2</td>
<td>(CH1+2+3+4+5+6) /6</td>
</tr>
</tbody>
</table>

Table 7-2-5-2. Mono Mode Select (ODP pin = “H”) (AK5556)
- CKS3-0: Sampling Speed Mode and MCLK Frequency Select

<table>
<thead>
<tr>
<th>CKS3 SW804-7</th>
<th>CKS2 SW804-6</th>
<th>CKS1 SW804-5</th>
<th>CKS0 SW804-4</th>
<th>MSN pin SW802-5</th>
<th>MCLK Frequency</th>
<th>fs Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>128fs</td>
<td>Quad Speed Mode 108kHz &lt; fs ≤ 216kHz</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>192fs</td>
<td>Quad Speed Mode 108kHz &lt; fs ≤ 216kHz</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>256fs</td>
<td>Normal Speed Mode 8kHz ≤ fs ≤ 54kHz</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>256fs</td>
<td>Double Speed Mode 54kHz &lt; fs ≤ 108kHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>384fs</td>
<td>Double Speed Mode 54kHz &lt; fs ≤ 108kHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>384fs</td>
<td>Normal Speed Mode 8kHz ≤ fs ≤ 54kHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>512fs</td>
<td>Normal Speed Mode 8kHz &lt; fs ≤ 54kHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>768fs</td>
<td>Normal Speed Mode 8kHz ≤ fs ≤ 54kHz</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>64fs</td>
<td>Oct Speed Mode fs = 384kHz</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>32fs</td>
<td>Hex Speed Mode fs = 768kHz</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>96fs</td>
<td>Oct Speed Mode fs = 384kHz</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>48fs</td>
<td>Hex Speed Mode fs = 768kHz</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>64fs</td>
<td>Hex Speed Mode fs = 768kHz</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>1024fs</td>
<td>Normal Speed Mode 8kHz ≤ fs ≤ 32kHz</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>Auto</td>
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Table 7-2-7. Data Interface mode setting

* Don’t Care
- DSDSEL1-0: Select the Frequency of DCLK (DSD Clock)

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<th>DSDSEL1 SW803-7</th>
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<th>DSD Sampling Frequency</th>
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<td>H (1)</td>
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<td>fs=44.1kHz</td>
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<td>H (1)</td>
<td>L (0)</td>
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<td>H (1)</td>
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Table 7-2-8. DSD Sampling Frequency Select (AK5556)

- SLOW: Slow Roll-off Filter Select
- SD: Short Delay Filter Select

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<th>SD SW804-9</th>
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<td>L (0)</td>
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<td>Slow Roll-off Filter</td>
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<td>H (1)</td>
<td>Short Delay Slow Roll-off Filter</td>
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Table 7-2-9. Digital Filter Select: PCM Mode (AK5556)
[8] Start-up and stop sequence

[SW800] Power Down (PDN) for AK5556
Reset AK5556 (U100) once by bringing SW800 to “L” once upon power-up.
Keep “H” when AK5556 is in use; keep “L” when AK5556 is not in use.

[SW801] Power Down (PDN) for AK4118A
Reset AK4118A (U600) once by bringing SW801 to “L” once upon power-up.
Keep “H” when AK4118A is in use; keep “L” when AK4118A is not in use.

(8-1) Serial Control mode

Start-up
(1) Set the Jumpers and DIP switches on board.
(2) Connect USB I/F BOX to PC.
(3) Open control software.
(4) Set SW800 and SW801 to “L” (Power down)
(5) Power up the external power supplies.
(6) Set SW800 and SW801 to “H” (Start normal operation)
(7) Reset USB I/F BOX.
(8) Set control registers.
(9) Enable analog input signals.

Stop
(1) Set SW800 and SW801 to “L” (Power down)
(2) Disconnect USB I/F BOX from PC.
(3) Power down the external power supplies.

(8-2) Parallel Control mode

Start-up
(1) Set the Jumpers and DIP switches on board.
(2) Set SW800 and SW801 to “L” (Power down)
(3) Power up the external power supplies.
(4) Set SW800 and SW801 to “H” (Start normal operation)

Stop
(1) Set SW800 and SW801 to “L” (Power down)
(2) Power down the external power supplies.
Control Software Manual

Set-up evaluation board and control software

1. Set up AKD5556-B evaluation board according to above instructions.
2. Connect PC with AKD5556-B evaluation board by USB cable (included in package).
3. Insert the CD-ROM labeled “AKD5556-B Evaluation Kit” into the CD-ROM drive.
4. Access the CD-ROM drive, double-click on “akd5556-a.exe” and set up the control program.
5. Evaluate according to the following.

Operation flow

1. Set up control program as above and open control program.
   The following operation screen will be shown. (Default setting)

Figure 9-1. Control software window
2. Click the “Write” button on right side of Addr 01H register.

![Register Set Window]

**Figure 9-2. Register set window**

3. Input dummy command settings and click “OK” to write dummy command to AK5556. The following No Ack error message will pop up. Click “OK”.

![No Ack Message Window]

**Figure 9-3. No ack message window**

4. Input registers accordingly into dialog box to evaluate AK5556.

### Button Functions

1. [Port Reset] : Set up USB interface board (AKDUSBIF-B).
2. [Write Default] : Initialize all register setting.
3. [All Write] : Write all registers currently displayed.
4. [All Read] : Read all register setting.
5. [Save] : Save the current register setting to .akr file.
7. [All Reg Write] : Opens “All Register Write” dialog box. (see Dialog boxes below)
8. [Data R/W] : Opens “Data Read/Write” dialog box. (see Dialog boxes below)
9. [Read] : Read and display current register setting in register window (on right side of main window).
   Different from [All Read] as it does not reflect to the register map.
10. [Close] : Close Control Software window.
Dialog boxes

1. [All Register Write]: Dialog box to write register setting files

Clicking the [All Reg Write] button in the main window opens the dialog box below. Multiple register setting files created by the [SAVE] button can be set and applied.

Figure 9-4. Window of [All Reg Write]

<Operation flow>
(1) Click [Open(left)] Button.
(2) Select file (*.akr) and Click [Open] Button. Up to 10 files can be selected.
(3) Click [Write] to write each file. [Write ALL] writes all files selected.

Button Functions:
1. [Open (left)] : Select register setting file (*.akr).
3. [Write ALL] : Write all register setting files selected. Write is executed in descending order.
5. [Save] : Save the current register map setting (*.mar).
6. [Open (right)] : Load register map setting file (*.mar).
7. [Close] : Close dialog box.
2. [Data Read/Write]: Dialog box to manually enter register setting

Click the [Data R/W] button in the main window to open the data read/write dialog box. Data manually entered into Data box is written to the specified address.

![Data Read/Write dialog box]

**Figure 9-5. Window of [Data R/W]**

**Textbox Functions:**
- **Address**: Input register address in 2 hexadecimal digits.
- **Data**: Input register data in 2 hexadecimal digits.
- **Mask**: Input mask data in 2 hexadecimal digits. This value is AND-ed with input data.

**Button Functions:**
- **Write**: Writes data generated from [Data] and [Mask] to register specified in [Address]
- **Read**: Displays register data specified in [Address] in [Read Data] box in hexadecimal.
- **Close**: Closes dialog box. To cancel a process close the dialog box without writing

※ Register map updated after [Write] and [Read] operation.
Tab Functions
1. [REG]: Register Map
   Register data is indicated on the register map. Each bit on the register map is a push-button switch.
   Button DOWN and red lettering indicates “1” and button UP with blue lettering indicates “0”.
   Buttons with “---“are undefined in the datasheet.

![Register Map Diagram]

Figure 9-6. [REG] window (REG 00H-07H)
2. [Tool]: Testing Tools

This tab screen is for the evaluation testing tool. Click button for each testing tool.

Figure 9-7. [Tool] window
### Measurement Results

#### Measurement condition
- Measurement unit: Audio Precision SYS2722 (No. 00454)
- MCKI: 512fs/256fs/128fs (24.376MHz)
- BICK: 64fs
- fs: 48kHz / 96kHz / 192kHz
- Bit: 24bit
- Measurement Mode: ADC @ Slave Mode
- Power Supply: VOP+(15V)=15V, GND
  - AVDD=+5.0V (Regulator), TVDD=+3.3V (Regulator)
- Input Frequency: 1kHz
- Measurement Frequency: BW=20kHz @48kHz / BW=40kHz @96kHz / BW=40kHz @192kHz
- Temperature: Room

#### Measurement Results

1. Stereo ADC (Differential Inputs)

<table>
<thead>
<tr>
<th>Result</th>
<th>SDTO1</th>
<th>SDTO2</th>
<th>SDTO3</th>
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<tbody>
<tr>
<td>Lch</td>
<td>Rch</td>
<td>Lch</td>
<td>Rch</td>
</tr>
<tr>
<td>Stereo ADC : AINL/R =&gt; ADC =&gt; SDTO1/2/3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D)</td>
<td>fs = 48kHz (-1dBFS)</td>
<td>111.7</td>
<td>111.6</td>
</tr>
<tr>
<td></td>
<td>fs = 96kHz (-1dBFS)</td>
<td>108.5</td>
<td>108.6</td>
</tr>
<tr>
<td></td>
<td>fs = 192kHz (-1dBFS)</td>
<td>108.3</td>
<td>108.2</td>
</tr>
<tr>
<td>DR</td>
<td>fs = 48kHz (-60dBFS, A-Weighted)</td>
<td>117.0</td>
<td>117.0</td>
</tr>
<tr>
<td>S/N</td>
<td>fs = 48kHz (A-weighted)</td>
<td>116.8</td>
<td>116.8</td>
</tr>
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</table>
AKD5556: Stereo Mode

fs = 48 kHz

AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, fin=1kHz

Figure 9-1. FFT (-1dBFS Input)

AK5556 FFT (-60dBFS Input)

AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, fin=1kHz

Figure 9-1.2. FFT (-60dBFS Input)
$f_s = 48 \text{ kHz}$

AK5556 FFT (No Signal Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, fin=1kHz

Figure 9-1-3. FFT (No Signal Input)

AK5556 THD+N vs. Input Level
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, fin=1kHz

Figure 9-1-4. THD+N vs. Input Level
fs = 48 kHz
AK5556 THD+N vs. Input Frequency
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, -1dBFS Input

Figure 9-1.5. THD+N vs. Input Frequency

AK5556 Linearity
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, fin=1kHz

Figure 9-1.6. Linearity
fs = 48 kHz
AK5556 Frequency Response
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, -1dBFS input

![Frequency Response Graph](image)

Figure 9-1-7. Frequency Response

AK5556 Crosstalk
AVDD=+5.0V, TVDD=+3.3V, MCLK=512fs, -1dBFS Input

![Crosstalk Graph](image)

Figure 9-1-8. Crosstalk
fs = 96 kHz
AK5556 FFT (-1dBFS Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, fin=1kHz

Figure 9-2-1. FFT (-1dBFS Input)

AK5556 FFT (-60dBFS Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, fin=1kHz

Figure 9-2-2. FFT (-60dBFS Input)
fs = 96 kHz
AK5556 FFT (No Signal Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, fin=1kHz

Figure 9-2-3. FFT (No Signal Input)

AK5556 THD+N vs. Input Level
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, fin=1kHz

Figure 9-2-4. THD+N vs. Input Level
fs = 96 kHz
AK5556 THD+N vs. Input Frequency
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, -1dBFS Input

Figure 9-2-5. THD+N vs. Input Frequency

AK5556 Linearity
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, fin=1kHz

Figure 9-2-6. Linearity
fs = 96 kHz
AK5556 Frequency Response
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, -1dBFS Input

Figure 9-2-7. Frequency Response

AK5556 Crosstalk
AVDD=+5.0V, TVDD=+3.3V, MCLK=256fs, -1dBFS Input

Figure 9-2-8. Crosstalk
Red : Lch, Blue : Rch

fs = 192 kHz

AK5556 FFT (-1dBFS Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, fin=1kHz

Figure 9-3-1. FFT (-1dBFS Input)

AK5556 FFT (-60dBFS Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, fin=1kHz

Figure 9-3-2. FFT (-60dBFS Input)
fs = 192 kHz
AK5556 FFT (No Signal Input)
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, fin=1kHz

Figure 9-3-3. FFT (No Signal Input)

AK5556 THD+N vs. Input Level
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, fin=1kHz

Figure 9-3-4. THD+N vs. Input Level
fs = 192 kHz
AK5556 THD+N vs. Input Frequency
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, -1dBFS Input

Figure 9-3-5. THD+N vs. Input Frequency

AK5556 Linearity
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, fin=1kHz

Figure 9-3-6. Linearity
fs = 192 kHz
AK5556 Frequency Response
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, -1dBFS Input

Figure 9-3-7. Frequency Response

AK5556 Crosstalk
AVDD=+5.0V, TVDD=+3.3V, MCLK=128fs, -1dBFS Input

Figure 9-3-8. Crosstalk
# Revision History

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<thead>
<tr>
<th>Date</th>
<th>Manual Revision</th>
<th>Board Revision</th>
<th>Reason</th>
<th>Page</th>
<th>Contents</th>
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Analog Input AIN1 & AIN2

- 50 -
X600 Frequency Check -> 24.576MHz
+ 1pin Socket (AK4118 Xtal)
Dual supply Translating Transceiver (3-state)

nOE nDIR nAn nBn
L L nAn=nBn input

0.01μF

74AVC4T245

nOE nDIR nAn nBn input
L H input nBn=nAn
H X Z Z

Dual supply Translating Transceiver (3-state)

0.01μF