GENERAL DESCRIPTION

AKD5720-A is an evaluation board for AK5720 which is a low voltage 24-bit analog-digital converter developed for digital audio systems. It supports Jacks for analog signal input. This board also has a digital interface and can achieve the interface with a digital audio system through an optical connector.

Ordering guide

AKD5720-A --- Evaluation board for AK5720

Figure 1. AKD5720-A Block Diagram
**Description**

(1) J1, J2 (Analog data)
   RCA jack, Used for Analog audio input.

(2) J3, J4, J5, J6, J7, J8 (Power supply)
   The Ak5720 can be powered by external power supply or by Regulator (T1, T2, T3, T4) on the evaluation board.

(3) PORT1 (10pin header)
   10pin header (MCLK, BICK, LRCK, SDTO, TDMI)

(4) PORT2 (Digital Data)
   SPDIF output (Optical output connector.)

(5) U1 (AK5720)
   Low voltage 24bit analog-digital converter.

(6) U2 (AK4118A)
   AK4118A is DIT, which transmits digital data of AK5720.

(7) SW1 (Toggle switch)
   Power down of AK5720
   “H” : PDN of AK5720 is Hi.
   “L” : PDN of AK5720 is Lo.

(8) SW2 (Toggle switch)
   Power down of AK4118A
   “H” : PDN of AK4118A is Hi.
   “L” : PDN of AK4118A is Lo.

(9) SW3 (Dip switch)
   Setting of AK5720 and AK4118A
   See Table4.
(10) JP1, JP2, JP3, JP4
    Setting of audio interface format of AK5720

(11) JP5
    Setting of digital filter of AK5720

(12) JP6
    Setting of input gain of AK5720

(13) JP7
    Setting of AK4118a

(14) JP8
    Setting of AK4118a

    Setting of power supply of AK5720 and AK4118a
Evaluation Board Manual

Operation Sequence

1) Set up the Power Supply Lines.

2) Setup the Audio I/F Evaluation Mode.

   (1) Evaluation of A/D using DIT of AK4118A.
       (1-1) Slave Mode (Default)
       (1-2) Master Mode
       (1-3) PLL Slave Mode

   (2) Evaluation of A/D using external clock.
       (2-1) Slave Mode
       (2-2) Master Mode
       (2-3) PLL Slave Mode

3) Jumper pins and SW Setting.

   (1) Setting of other jumper pins

   (2) Setting of SW

4) Power on
1) **Set up the power Supplies**

JP9 (SEL_VA): When VA is supplied from the regulator.
- **JP9 5V**: VA is supplied 5V. <Default>
- **3V**: VA is supplied 3V.

JP10 (SEL_VD): When VD is supplied from the regulator.
- **JP10 5V**: VD is supplied 5V. <Default>
- **3V**: VD is supplied 3V.

JP11 (VD): VD line and VA line are set common or separation.
- **JP11 VA**: VD line and VA line are set common.
- **VD**: VD line and VA line are set separation.
- **OPEN**: VD is not supplied from the regulator. <Default>

JP12 (VA): VA is supplied from the regulator.
- **JP12 OPEN**: VA is not supplied from the regulator. <Default>
- **SHORT**: VA is supplied from the regulator.

JP13 (4118a_3.3V): When power supply of AK4118A is supplied from the regulator.
- **JP13 OPEN**: Power supply of AK4118A is not supplied from the regulator. <Default>
- **SHORT**: Power supply of AK4118A is supplied from the regulator.

JP14: VSS and DGND are set common or separation.
- **JP14 OPEN**: VSS and DGND are set common.
- **SHORT**: VSS and DGND are set separation. <Default>

(1) **When VA, VD and 4118a_3.3V are supplied from the regulator. <Default>**

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Setting</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>VD</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>VSS</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK5720</td>
</tr>
<tr>
<td>4118a_3.3V</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>DGND</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK4118a</td>
</tr>
<tr>
<td>REG</td>
<td>Yellow</td>
<td>+7V</td>
<td>Power supply for the regulator.</td>
</tr>
</tbody>
</table>

Table 1  Setup of power supply (Used regulator)

Jumper Setting

<table>
<thead>
<tr>
<th>Name</th>
<th>Setting</th>
<th>Name</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP9</td>
<td>Short on 5V side</td>
<td>JP9</td>
<td>Short on 3V side</td>
</tr>
<tr>
<td>JP10</td>
<td>Short on 5V side</td>
<td>JP10</td>
<td>Short on 3V side</td>
</tr>
<tr>
<td>JP11</td>
<td>VA : VD line and VA line are set common. (Default)</td>
<td>JP11</td>
<td>VA : VD line and VA line are set common. (Default)</td>
</tr>
<tr>
<td></td>
<td>VD : VD line and VA line are set separation</td>
<td></td>
<td>VD : VD line and VA line are set separation</td>
</tr>
<tr>
<td>JP12</td>
<td>Short</td>
<td>JP12</td>
<td>Short</td>
</tr>
<tr>
<td>JP13</td>
<td>Short</td>
<td>JP13</td>
<td>Short</td>
</tr>
</tbody>
</table>

Table 2  Setting of VA=VD=5V  Table 3  Setting of VA=VD=3V

(2) **When VA, VD and 4118a_3.3V are supplied from the power supply connectors.**
Set up the power supply lines

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Setting</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>Red</td>
<td>+2.7～+5.5V</td>
<td>Power supply for VA of AK5720.</td>
</tr>
<tr>
<td>VD</td>
<td>Red</td>
<td>+2.7～-5V</td>
<td>Power supply for VD of AK5720.</td>
</tr>
<tr>
<td>VSS</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK5720.</td>
</tr>
<tr>
<td>4118a 3.3V</td>
<td>Red</td>
<td>+3.3V</td>
<td>Power supply for AK4118a.</td>
</tr>
<tr>
<td>DGND</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK4118a.</td>
</tr>
<tr>
<td>REG</td>
<td>Yellow</td>
<td>Open</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Table 4 Setup of power supply (Not used regulator)

Jumper Setting

<table>
<thead>
<tr>
<th>Name</th>
<th>Setting</th>
<th>Name</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP9</td>
<td>Open</td>
<td>JP9</td>
<td>Open</td>
</tr>
<tr>
<td>JP10</td>
<td>Open</td>
<td>JP10</td>
<td>Open</td>
</tr>
<tr>
<td>JP11</td>
<td>Short on VA side</td>
<td>JP11</td>
<td>Short on VD side</td>
</tr>
<tr>
<td>JP12</td>
<td>Short</td>
<td>JP12</td>
<td>Open</td>
</tr>
<tr>
<td>JP13</td>
<td>Open</td>
<td>JP13</td>
<td>Open</td>
</tr>
</tbody>
</table>

Table 5 Setting of VA=VD

Table 6 Setting of VA ≠ VD
2) Setup the Audio I/F Evaluation Mode

In case of using the AK4118A when evaluating the AK5720, the audio interface format of the AK5720 and AK4118A must be matched. Refer to audio interface format of AK5720 (Table 7, Table 8), and audio interface format of AK4118A (Table 10). The AK4118A operates at sampling frequency of 32 kHz or more. If the sampling frequency is lower than 32 kHz, please use other mode. Refer to the datasheet for register setting of the AK5720.

(1) Evaluation of A/D using DIT of AK4118A

(1-1) Slave Mode. (Default).

PORT2 (TOTX) is used

- PORT1: Open
- AK5720: Slave mode
- AK4118A: Master mode
- SW3(4118-DIF1) : “Lo”

<table>
<thead>
<tr>
<th>Mode</th>
<th>JP1 (VA/ GND)</th>
<th>JP2 (CKS)</th>
<th>JP4 (DIF/ TDMI)</th>
<th>JP3 (DIF)</th>
<th>SDTO</th>
<th>Master/ Slave</th>
<th>MCLK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>GND</td>
<td>Short on 1 side (Short to GND)</td>
<td>DIF</td>
<td>L</td>
<td>MSB</td>
<td>Slave</td>
<td>256/384fs (8k≤fs≤96k)</td>
<td>512/768fs (8k≤fs≤48k)</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 1 side (Short to VA)</td>
<td>DIF</td>
<td>L</td>
<td>MSB</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>64fs</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>Short on 2 side (4.7kΩ±10% to GND)</td>
<td>DIF</td>
<td>L</td>
<td>MSB</td>
<td>Master</td>
<td>384fs (8k≤fs≤96k)</td>
<td>64fs</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 2 side (4.7kΩ±10% to VA)</td>
<td>DIF</td>
<td>H</td>
<td>I’S</td>
<td>Master</td>
<td>512fs (8k≤fs≤48k)</td>
<td>64fs</td>
</tr>
<tr>
<td>TDM</td>
<td>GND</td>
<td>Short on 3 side (18kΩ±10% to GND)</td>
<td>TDMI</td>
<td></td>
<td>MSB</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>256fs</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 3 side (18kΩ±10% to VA)</td>
<td>TDMI</td>
<td></td>
<td>MSB</td>
<td>Slave</td>
<td>256fs (8k≤fs≤96k)</td>
<td>256fs</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>Short on 4 side (82kΩ±10% to GND)</td>
<td>TDMI</td>
<td></td>
<td>I’S</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>256fs</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 4 side (82kΩ±10% to VA)</td>
<td>TDMI</td>
<td></td>
<td>I’S</td>
<td>Slave</td>
<td>256fs (8k≤fs≤96k)</td>
<td>256fs</td>
</tr>
</tbody>
</table>

Table 7 Slave Mode (Setting of JP1, JP2, JP3, JP4)

MCLK, BICK and LRCK are supplied from AK4118A to AK5720. PORT2 outputs optical data of AK5720 through AK4118A. MCLK can be selected between 512fs and 256fs by JP7.
(1-2) Master Mode

PORT2 (TOTX) is used

- PORT1: Open
- AK5720: Master mode
- AK4118A: Slave mode
- SW3(4118-DIF1) : “Hi”

<table>
<thead>
<tr>
<th>Mode</th>
<th>JP1 (VA/ GND)</th>
<th>JP2 (CKS)</th>
<th>JP4 (DIF/ TDMI)</th>
<th>JP3 (DIF)</th>
<th>SDTO</th>
<th>Master/ Slave</th>
<th>MCLK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>GND</td>
<td>Short on 1 side (Short to GND)</td>
<td>DIF</td>
<td>L</td>
<td>MSB</td>
<td>Slave</td>
<td>256/384fs (8k≤fs≤96k)</td>
<td>512/768fs (8k≤fs≤48k)</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 1 side (Short to VA)</td>
<td>DIF</td>
<td>H</td>
<td>I$^S$</td>
<td>Master</td>
<td>256fs (8k≤fs≤96k)</td>
<td>64fs</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>Short on 2 side (4.7kΩ±10% to GND)</td>
<td>DIF</td>
<td>L</td>
<td>MSB</td>
<td>Master</td>
<td>384fs (8k≤fs≤96k)</td>
<td>64fs</td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 2 side (4.7kΩ±10% to VA)</td>
<td>DIF</td>
<td>H</td>
<td>I$^S$</td>
<td>Master</td>
<td>512fs (8k≤fs≤48k)</td>
<td>64fs</td>
</tr>
<tr>
<td>TDM</td>
<td>GND</td>
<td>Short on 3 side (18kΩ±10% to GND)</td>
<td>TDMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 3 side (18kΩ±10% to VA)</td>
<td>TDMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>Short on 4 side (82kΩ±10% to GND)</td>
<td>TDMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VA</td>
<td>Short on 4 side (82kΩ±10% to VA)</td>
<td>TDMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 8  Master Mode (Setting of JP1, JP2, JP3, JP4)

MCLK is supplied from AK4118A or external input to AK5720. LRCK, BICK, SDTO of AK5720 are outputs to AK4118A. PORT2 outputs optical data of AK5720 through AK4118A. MCLK can be selected between 512fs and 256fs by JP10.
(2) Evaluation of A/D using external clock.

(2-1) Slave Mode

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5720: Slave mode
- Setting of JP1, JP2, JP3, JP4 : See Table 7
- SW3(4118-DIF1) : “Lo”

MCLK, BICK and LRCK are supplied from PORT1 to AK5720. SDTO of AK5720 is output to PORT1.

(2-2) Master Mode

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5720: Master mode
- Setting of JP1, JP2, JP3, JP4 : See Table 8
- SW3(4118-DIF1) : “Lo”

MCLK is supplied from PORT1. LRCK, BICK, SDTO of AK5720 is output to PORT1.
3) Jumper pins and SW Setting

(1) Setting of other jumper pins.

  H : Short Delay Sharp Roll-Off.

JP6 (GSEL): Setting of input gain of AK5720.
- JP6  L : 0dB. < Default >
  H : +6dB.

JP8 : The selection of OPEN or SHORT of SDTO line, BICK line, LRCK line for AK4118A.
- JP8  SDTO : SHORT < Default >
  BICK : SHORT < Default >
  LRCK : SHORT < Default >

(2) Setting of SW

[SW3] (SW DIP-4): Mode setting for AK4118A.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4118-DIF1</td>
<td>See Table 10</td>
<td></td>
<td>OFF</td>
</tr>
<tr>
<td>2</td>
<td>4118-DIF0</td>
<td></td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>3</td>
<td>4118-OCKS0</td>
<td>See Table 11</td>
<td></td>
<td>OFF</td>
</tr>
<tr>
<td>4</td>
<td>4118-OCKS1</td>
<td></td>
<td></td>
<td>ON</td>
</tr>
</tbody>
</table>

Table 9 Mode setting for AK4118A

<table>
<thead>
<tr>
<th>4118- DIF1</th>
<th>4118- DIF0</th>
<th>Mode</th>
<th>DAUX</th>
<th>SDTO</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>Master Mode</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Master Mode</td>
<td>24bit, I$^\uparrow$S</td>
<td>24bit, I$^\uparrow$S</td>
<td>L/H</td>
<td>O</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>Slave Mode</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>I</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Slave Mode</td>
<td>24bit, I$^\uparrow$S</td>
<td>24bit, I$^\uparrow$S</td>
<td>L/H</td>
<td>I</td>
</tr>
</tbody>
</table>

Table 10 Audio I/F Format Setting for AK4118A

<table>
<thead>
<tr>
<th>No.</th>
<th>OCKS1</th>
<th>OCKS0</th>
<th>MCKO1</th>
<th>MCKO2</th>
<th>X’tal</th>
<th>fs (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>256fs</td>
<td>256fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>256fs</td>
<td>128fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>512fs</td>
<td>256fs</td>
<td>512fs</td>
<td>48 kHz</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>128fs</td>
<td>64fs</td>
<td>128fs</td>
<td>192 kHz</td>
</tr>
</tbody>
</table>

(Default)

Table 11 Master Clock setting for AK4118A
4) Power on

[SW1] (5720-PDN) : The AK5720 should be reset once bringing “L” upon power-up. Keep “H” during normal operation.

[SW2] (4118a-PDN) : The AK4118A should be reset once bringing “L” upon power-up. Keep “H” during normal operation.
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AKD5720-A Rev.1  Pattern View

Silk View of Component Side
(Perspective View of Component Side)

U4, C47, C48: No mount
AKD5720-A Rev.1  Pattern View

Silk View of Solder Side
(Perspective View of Component Side)
AKD5720-A Rev.1  Pattern View

Pattern View of Component Side
(Perspective View of Component Side)
AKD5720-A Rev.1 Pattern View

Pattern View of Solder Side
(Perspective View of Component Side)