AKD5720-A

AK5720 Evaluation Board Rev.1

GENERAL DESCRIPTION

AKD5720-A is an evaluation board for AK5720 which is low voltage 24bit analog-digital converter developed for digital audio system. It supports Jacks for analog signal input.
This board also has a digital interface and can achieve the interface with a digital audio system through an optical connector.

■ **Ordering guide**

AKD5720-A --- Evaluation board for AK5720

FUNCTION

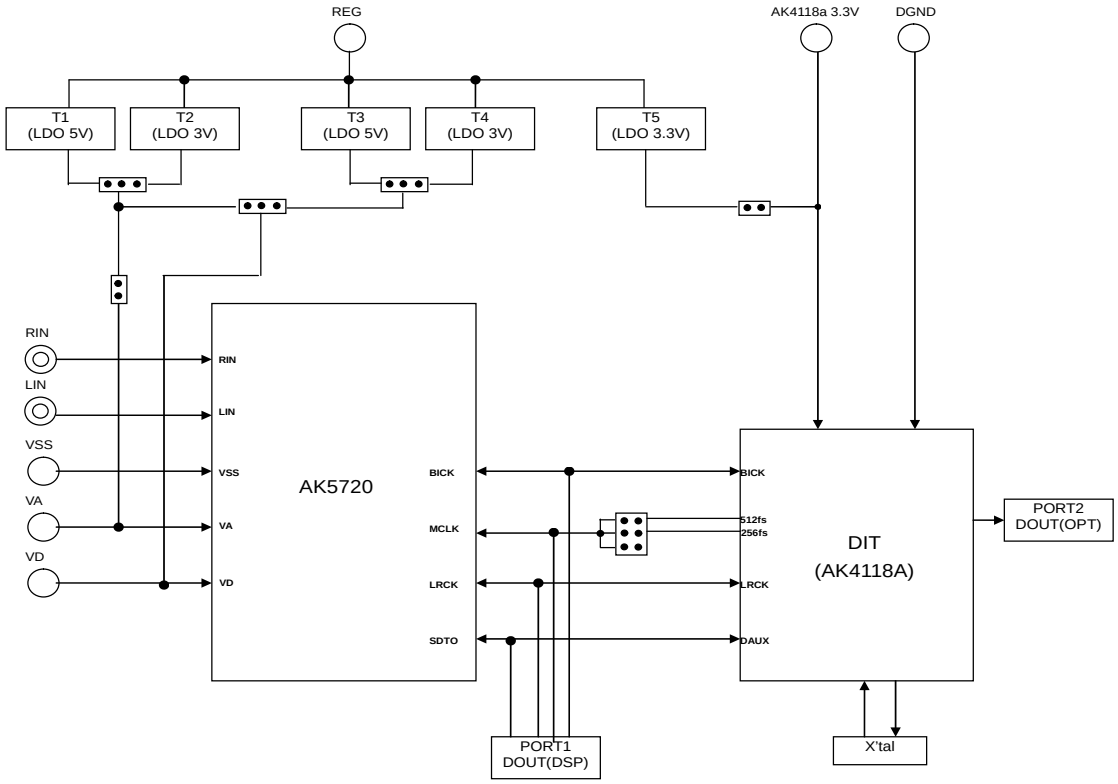


Figure 1. AKD5720-A Block Diagram

Board Outline Chart

■ Outline Chart

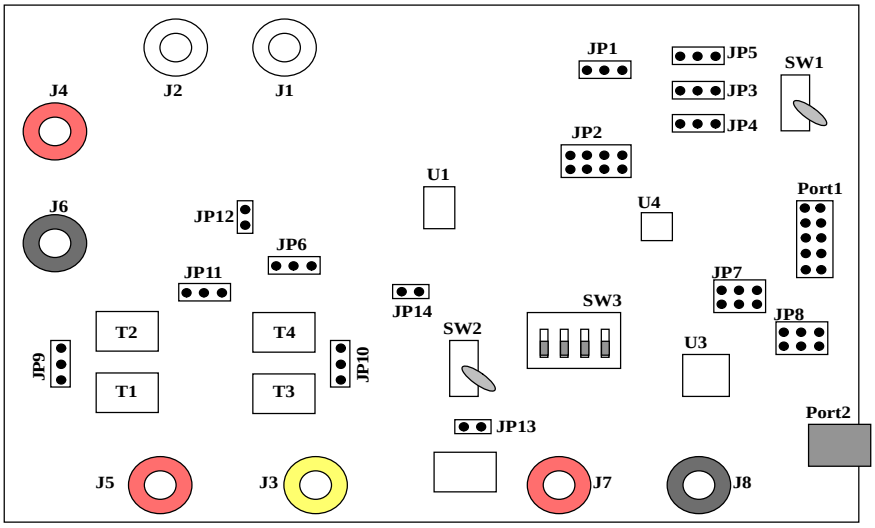


Figure 2. Outline Chart

■Description

(1) J1,J2（Analog data ）
RCA jack, Used for Analog audio input.

(2) J3,J4, J5, J6, J7,J8(Power supply)
The Ak5720 can be powered by external power supply or by Regulator (T1, T2, T3, T4) on the evaluation board.

(3) PORT1（10pin header）
10pin header (MCLK, BICK, LRCK, SDTO, TDMI)

(4) PORT2（Digital Data）
SPDIF output (Optical output connector.)

(5) U1(AK5720)
Low voltage 24bit analog-digital converter.

(6) U2（AK4118A）
AK4118A is DIT, which transmits digital data of AK5720.

(7) SW1(Toggle switch)
Power down of AK5720
"H" : PDN of AK5720 is Hi.
"L" : PDN of AK5720 is Lo.

(8) SW2(Toggle switch)
Power down of AK4118A
"H" : PDN of AK4118A is Hi.
"L" : PDN of AK4118A is Lo.

(9) SW3(Dip switch)
Setting of AK5720 and AK4118A
See Table4.

(10) JP1, JP2, JP3, JP4
Setting of audio interface format of AK5720

(11) JP5
Setting of digital filter of Ak5720

(12) JP6
Setting of input gain of AK5720

(13) JP7
Setting of AK4118a

(14) JP8
Setting of AK4118a

(15) JP9, JP10, JP11, JP12, JP13, JP14
Setting of power supply of AK5720 and AK4118a

Evaluation Board Manual

■ Operation Sequence

1) Set up the Power Supply Lines.

2) Setup the Audio I/F Evaluation Mode.

(1) Evaluation of A/D using DIT of AK4118A.
(1-1) Slave Mode (Default)
(1-2) Master Mode
(1-3) PLL Slave Mode

(2) Evaluation of A/D using external clock.
(2-1) Slave Mode
(2-2) Master Mode
(2-3) PLL Slave Mode

3) Jumper pins and SW Setting.

(1) Setting of other jumper pins

(2) Setting of SW

4) Power on

1) Set up the power Supplies

JP9 (SEL_VA): When VA is supplied from the regulator.
・JP9 5V : VA is supplied 5V. <Default>
3V : VA is supplied 3V.

JP10 (SEL_VD): When VD is supplied from the regulator.
・JP10 5V : VD is supplied 5V. <Default>
3V : VD is supplied 3V.

JP11 (VD): VD line and VA line are set common or separation.
・JP11 VA : VD line and VA line are set common.
VD : VD line and VA line are set separation.
OPEN : VD is not supplied from the regulator. <Default>

JP12 (VA): VA is supplied from the regulator.
・JP12 OPEN : VA is not supplied from the regulator. <Default>
SHORT : VA is supplied from the regulator.

JP13 (4118a_3.3V): When power supply of AK4118A is supplied from the regulator.
・JP13 OPEN : Power supply of AK4118A is not supplied from the regulator. <Default>
SHORT : Power supply of AK4118A is supplied from the regulator.

JP14 : VSS and DGND are set common or separation.
・JP14 OPEN : VSS and DGND are set common.
SHORT : VSS and DGND are set separation. <Default>

(1) When VA, VD and 4118a_3.3V are supplied from the regulator. <Default>

Set up the power supply lines

Name	Color	Setting	Comments
VA	Red	Open	Not used. Supplied through regulator
VD	Red	Open	Not used. Supplied through regulator
VSS	Black	0V	Ground for AK5720
4118a_3.3V	Red	Open	Not used. Supplied through regulator
DGND	Black	0V	Ground for AK4118a
REG	Yellow	+7V	Power supply for the regulator.

Table 1 Setup of power supply (Used regulator)

Jumper Setting

Name	Setting
JP9	Short on 5V side
JP10	Short on 5V side
JP11	VA : VD line and VA line are set common. VD : VD line and VA line are set separation .
JP12	Short
JP13	Short

Table 2 Setting of VA=VD=5V

Name	Setting
JP9	Short on 3V side
JP10	Short on 3V side
JP11	VA : VD line and VA line are set common. VD : VD line and VA line are set separation .
JP12	Short
JP13	Short

Table 3 Setting of VA=VD=3V

(2) When VA, VD and 4118a_3.3V are supplied from the power supply connectors.

Set up the power supply lines

Name	Color	Setting	Comments
VA	Red	+2.7～+5.5V	Power supply for VA of AK5720.
VD	Red	+2.7～VA V	Power supply for VD of AK5720.
VSS	Black	0V	Ground for AK5720.
4118a_3.3V	Red	+3.3V	Power supply for AK4118a.
DGND	Black	0V	Ground for AK4118a.
REG	Yellow	Open	Not used.

Table 4 Setup of power supply (Not used regulator)

Jumper Setting

Name	Setting
JP9	Open
JP10	Open
JP11	Short on VA side
JP12	Short
JP13	Open

Table 5 Setting of VA=VD

Name	Setting
JP9	Open
JP10	Open
JP11	Short on VD side
JP12	Open
JP13	Open

Table 6 Setting of VA≠VD

2) Setup the Audio I/F Evaluation Mode

In case of using the AK4118A when evaluating the AK5720, the audio interface format of the AK5720 and AK4118A must be matched.
Refer to audio interface format of AK5720 (Table 7, Table 8), and audio interface format of AK4118A (Table 10).
The AK4118A operates at sampling frequency of 32 kHz or more. If the sampling frequency is lower than 32 kHz, please use other mode.
Refer to the datasheet for register setting of the AK5720.

(1) Evaluation of A/D using DIT of AK4118A

(1-1) Slave Mode. (Default).

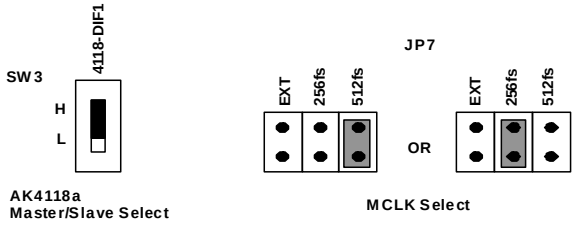
PORT2 (TOTX) is used

- PORT1: Open
- AK5720: Slave mode
- Setting of JP1, JP2, JP3, JP4 : See Table 7.
- AK4118A: Master mode
- SW3(4118-DIF1) : "Lo"

Mode	JP1 (VA/ GND)	JP2 (CKS)	JP4 (DIF/ TDMI)	JP3 (DIF)	SDTO	Master/ Slave	MCLK	BICK
Normal	GND	Short on 1 side (Short to GND)	DIF	L	MSB	Slave	256/384fs (8k≤fs≤96k) 512/768fs (8k≤fs≤48k)	≥ 48fs or 32fs
			DIF	H	I^2S			
	VA	Short on 1 side (Short to VA)	DIF	L	MSB	Master	256fs (8k≤fs≤96k)	64fs
			DIF	H	I^2S			
	GND	Short on 2 side (4.7kΩ±10% to GND)	DIF	L	MSB	Master	384fs (8k≤fs≤96k)	64fs
			DIF	H	I^2S			
	VA	Short on 2 side (4.7kΩ±10% to VA)	DIF	L	MSB	Master	512fs (8k≤fs≤48k)	64fs
			DIF	H	I^2S			
TDM	GND	Short on 3 side (18kΩ±10% to GND)	TDMI		MSB	Master	256fs (8k≤fs≤96k)	256fs
	VA	Short on 3 side (18kΩ±10% to VA)	TDMI		MSB	Slave	256fs (8k≤fs≤96k)	256fs
	GND	Short on 4 side (82kΩ±10% to GND)	TDMI		I^2S	Master	256fs (8k≤fs≤96k)	256fs
	VA	Short on 4 side (82kΩ±10% to VA)	TDMI		I^2S	Slave	256fs (8k≤fs≤96k)	256fs

Table 7 Slave Mode (Setting of JP1,JP2, JP3, JP4)

MCLK, BICK and LRCK are supplied from AK4118A to AK5720. PORT2 outputs optical data of AK5720 through AK4118A. MCLK can be selected between 512fs and 256fs by JP7.



(1-2) Master Mode

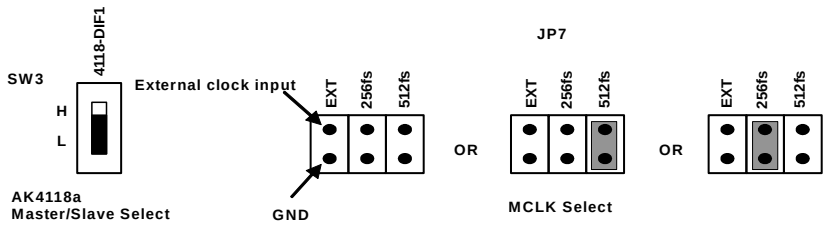
PORT2 (TOTX) is used

- PORT1: Open
- AK5720: Master mode
- Setting of JP1, JP2, JP3, JP4 : See Table 8.
- AK4118A: Slave mode
- SW3(4118-DIF1) : “Hi”

Mode	JP1 (VA/ GND)	JP2 (CKS)	JP4 (DIF/ TDMI)	JP3 (DIF)	SDTO	Master/ Slave	MCLK	BICK
Normal	GND	Short on 1 side (Short to GND)	DIF	L	MSB	Slave	256/384fs (8k≤fs≤96k) 512/768fs (8k≤fs≤48k)	≥ 48fs or 32fs
			DIF	H	I^2S			
	VA	Short on 1 side (Short to VA)	DIF	L	MSB	Master	256fs (8k≤fs≤96k)	64fs
			DIF	H	I^2S			
	GND	Short on 2 side (4.7kΩ±10% to GND)	DIF	L	MSB	Master	384fs (8k≤fs≤96k)	64fs
			DIF	H	I^2S			
	VA	Short on 2 side (4.7kΩ±10% to VA)	DIF	L	MSB	Master	512fs (8k≤fs≤48k)	64fs
			DIF	H	I^2S			
TDM	GND	Short on 3 side (18kΩ±10% to GND)	TDMI		MSB	Master	256fs (8k≤fs≤96k)	256fs
	VA	Short on 3 side (18kΩ±10% to VA)	TDMI		MSB	Slave	256fs (8k≤fs≤96k)	256fs
	GND	Short on 4 side (82kΩ±10% to GND)	TDMI		I^2S	Master	256fs (8k≤fs≤96k)	256fs
	VA	Short on 4 side (82kΩ±10% to VA)	TDMI		I^2S	Slave	256fs (8k≤fs≤96k)	256fs

Table 8 Master Mode (Setting of JP1,JP2, JP3, JP4)

MCLK is supplied from AK4118A or external input to AK5720. LRCK, BICK, SDTO of AK5720 are outputs to AK4118A. PORT2 outputs optical data of AK5720 through AK4118A. MCLK can be selected between 512fs and 256fs by JP10.



(2) Evaluation of A/D using external clock.

(2-1) Slave Mode

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5720: Slave mode
- Setting of JP1, JP2, JP3, JP4 : See Table 7
- SW3(4118-DIF1) : “Lo”

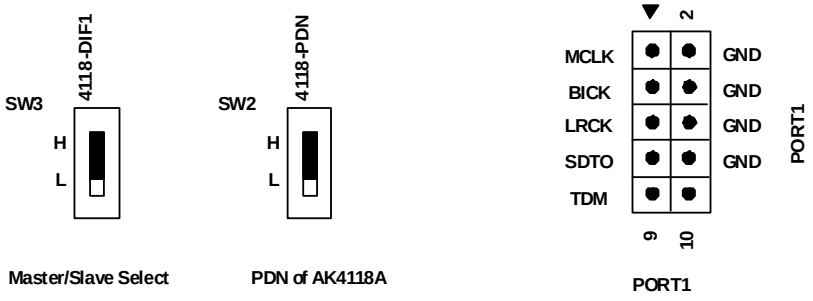
MCLK, BICK and LRCK are supplied from PORT1 to AK5720. SDTO of AK5720 is output to PORT1

(2-2) Master Mode

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5720: Master mode
- Setting of JP1, JP2, JP3, JP4 : See Table 8
- SW3(4118-DIF1) : “Lo”

MCLK is supplied from PORT1. LRCK, BICK , SDTO of AK5720 is output to PORT1.



3) Jumper pins and SW Setting

(1) Setting of other jumper pins.

JP5 (FSEL): Setting of digital-filter of AK5720.
・JP5 L : Sharp Roll-Off. < Default >
H : Short Delay Sharp Roll-Off.

JP6 (GSEL): Setting of input gain of AK5720.
・JP6 L : 0dB. < Default >
H : +6dB.

JP8 : The selection of OPEN or SHORT of SDTO line, BICK line, LRCK line for AK4118A.
・JP8 SDTO : SHORT < Default >
BICK : SHORT < Default >
LRCK : SHORT < Default >

(2) Setting of SW

[SW3] (SW DIP-4): Mode setting for AK4118A.

No.	Name	ON ("H")	OFF ("L")	Default
1	4118-DIF1	See Table 10		OFF
2	4118-DIF0			ON
3	4118-OCKS0	See Table 11		OFF
4	4118-OCKS1			ON

Table 9 Mode setting for AK4118A

4118-DIF1	4118-DIF0	Mode	DAUX	SDTO	LRCK		BICK	
						I/O		I/O
L	L	Master Mode	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O
L	H	Master Mode	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O
H	L	Slave Mode	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I
H	H	Slave Mode	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I

Table 10 Audio I/F Format Setting for AK4118A

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	(Default)
3	1	1	128fs	64fs	128fs	192 kHz	

Table 11 Master Clock setting for AK4118A

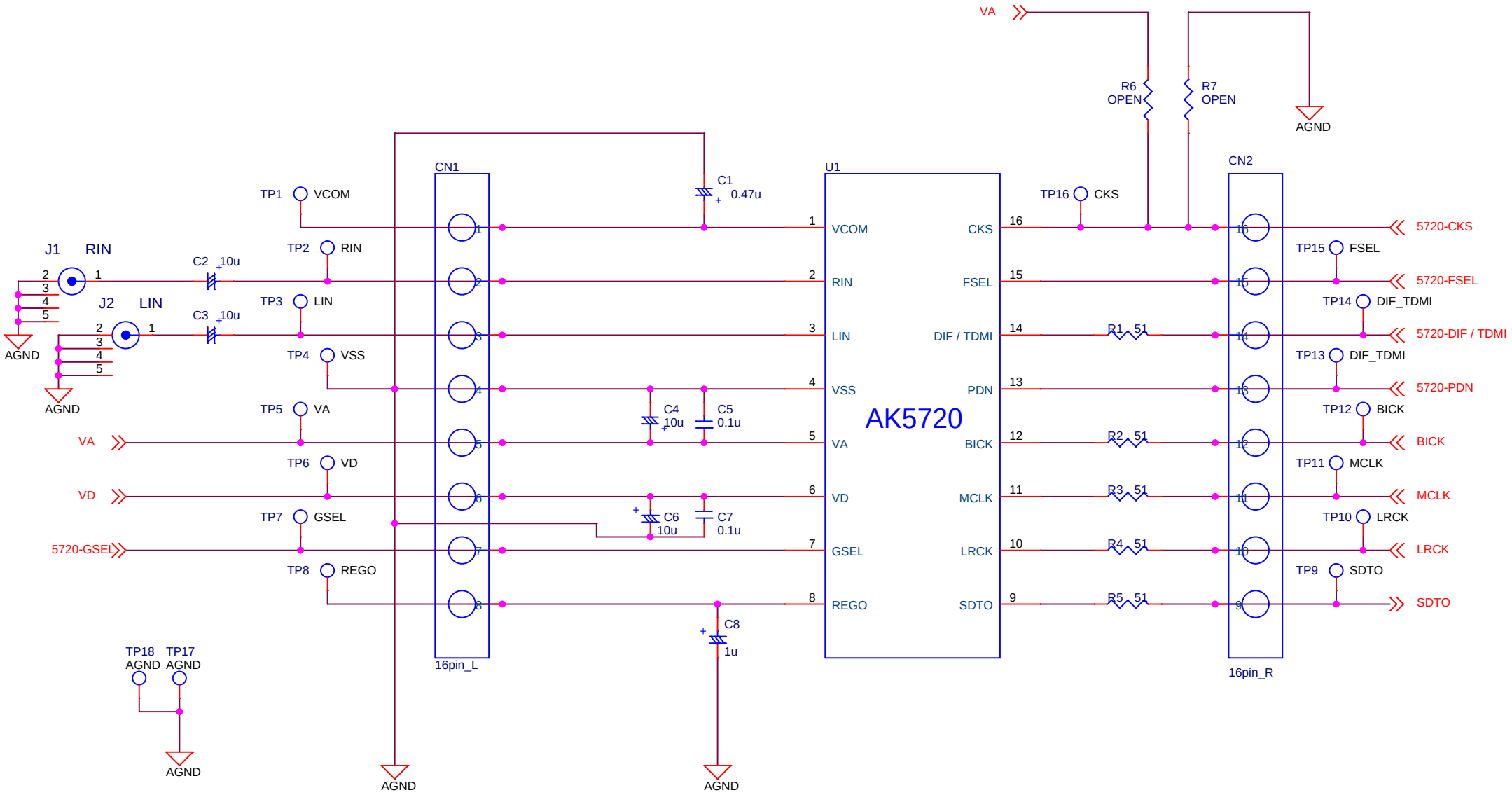
4) Power on

[SW1] (5720-PDN) : The AK5720 should be reset once bringing “L” upon power-up.
Keep “H” during normal operation.

[SW2] (4118a-PDN) : The AK4118A should be reset once bringing “L” upon power-up.
Keep “H” during normal operation.

Revision History

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
13/10/09	KM113600	0	First Edition		
13/10/15	KM113601	1	Specifications change	7,8	CKS Setting Changed



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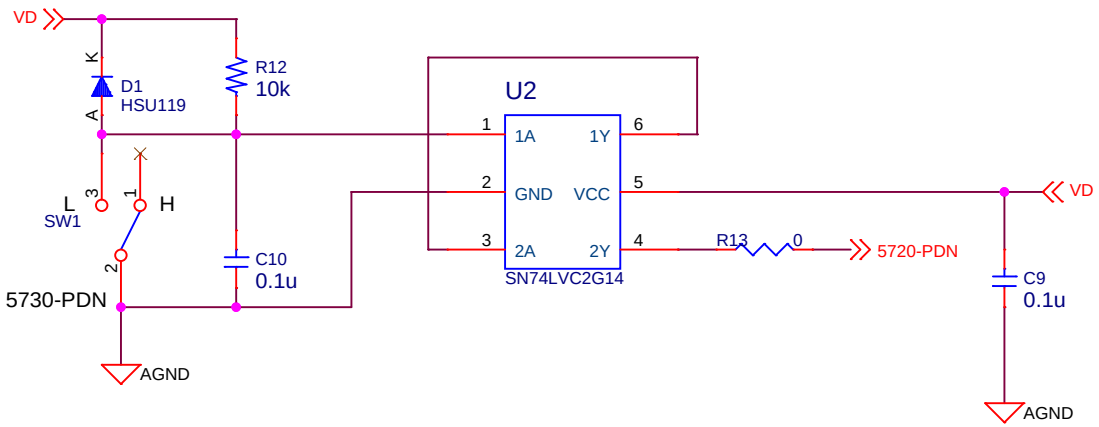

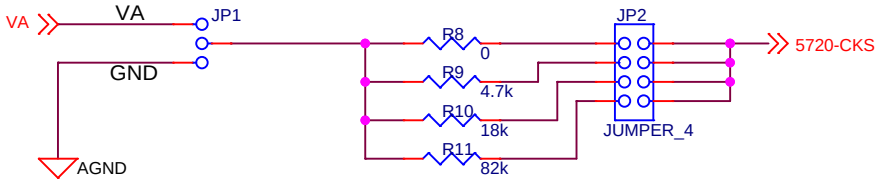

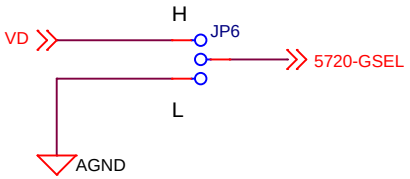

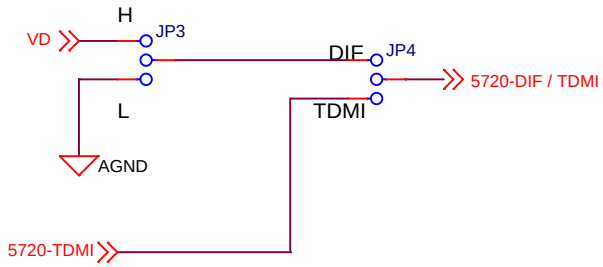

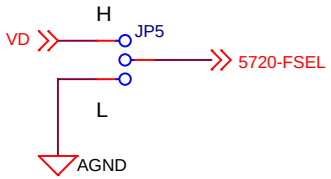

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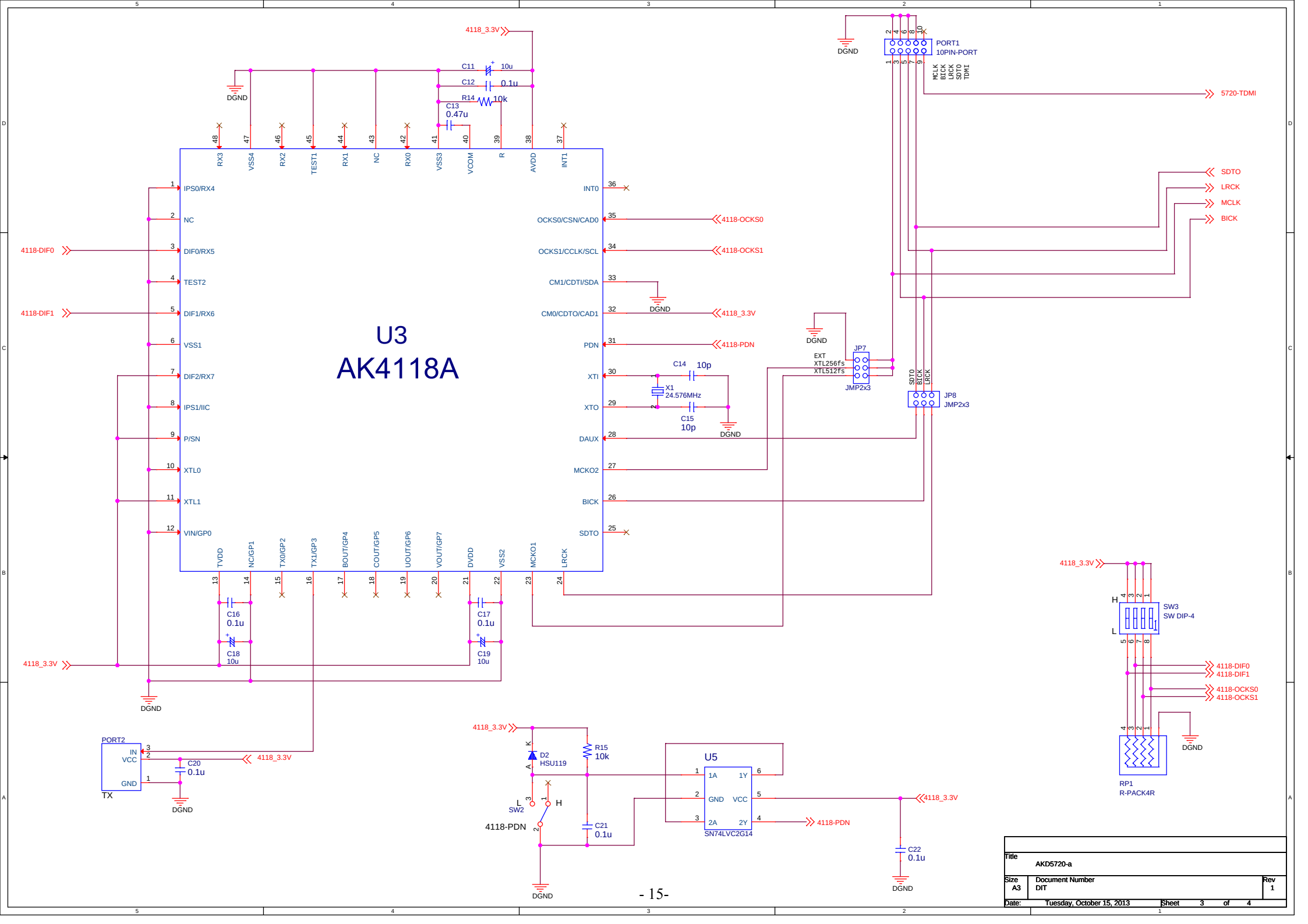

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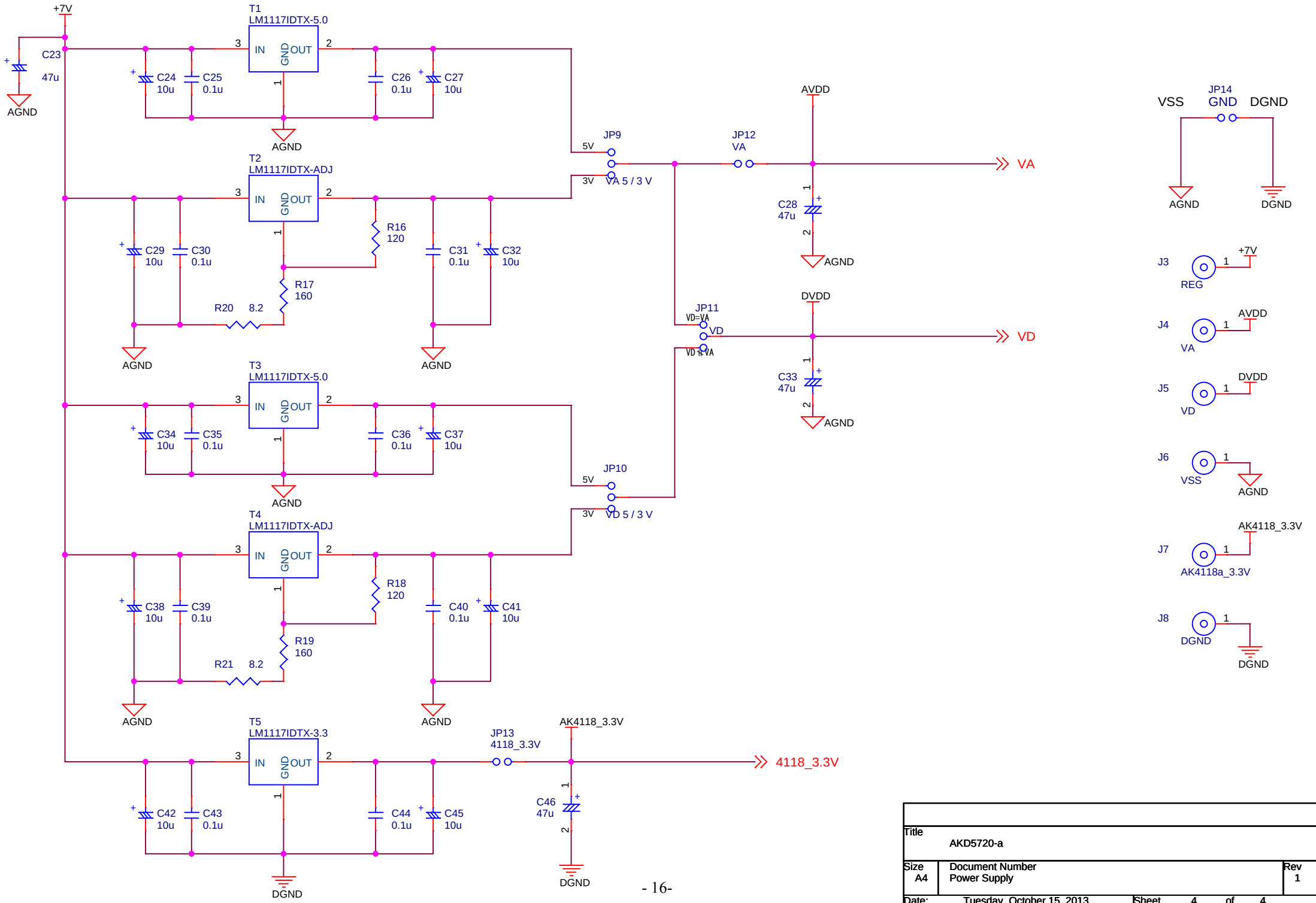

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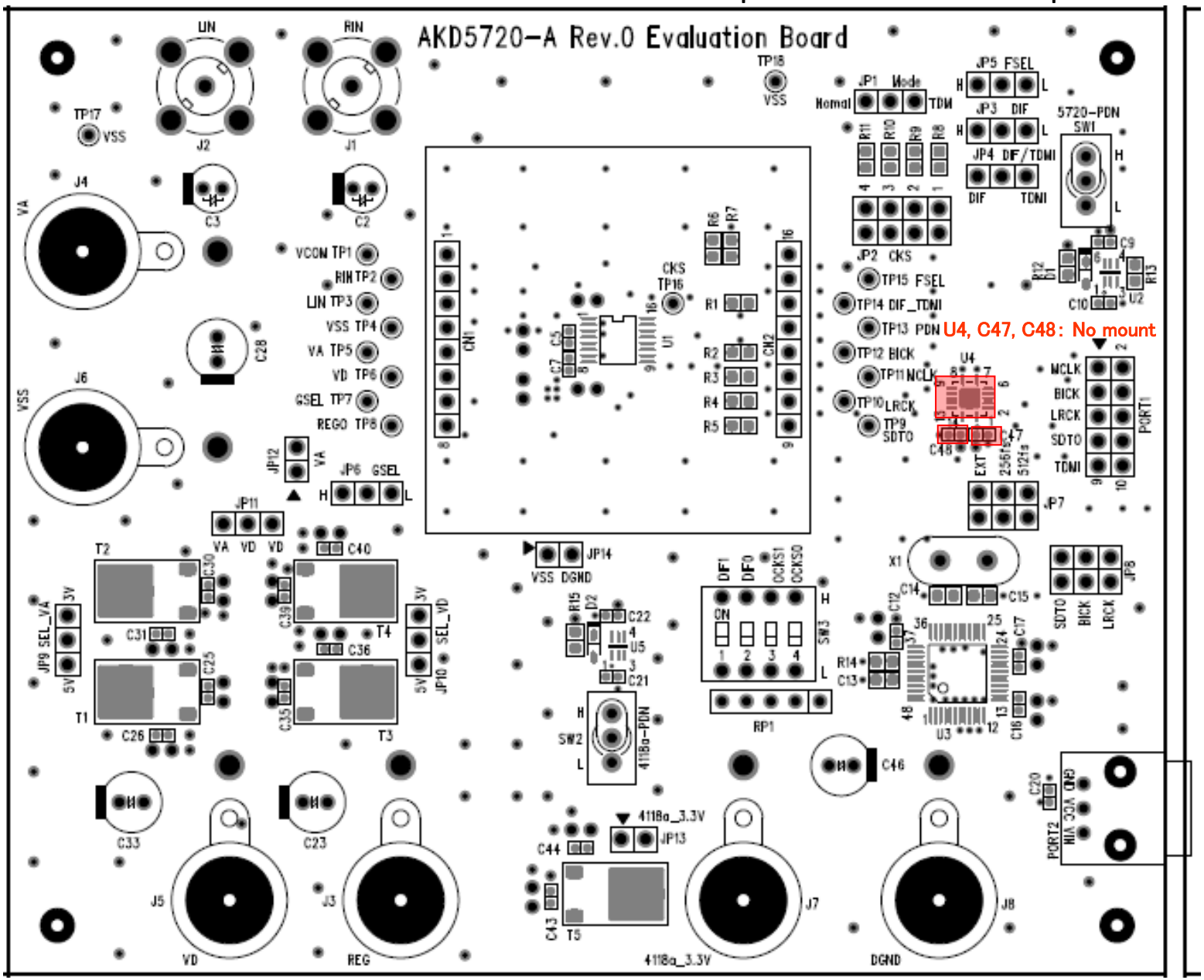
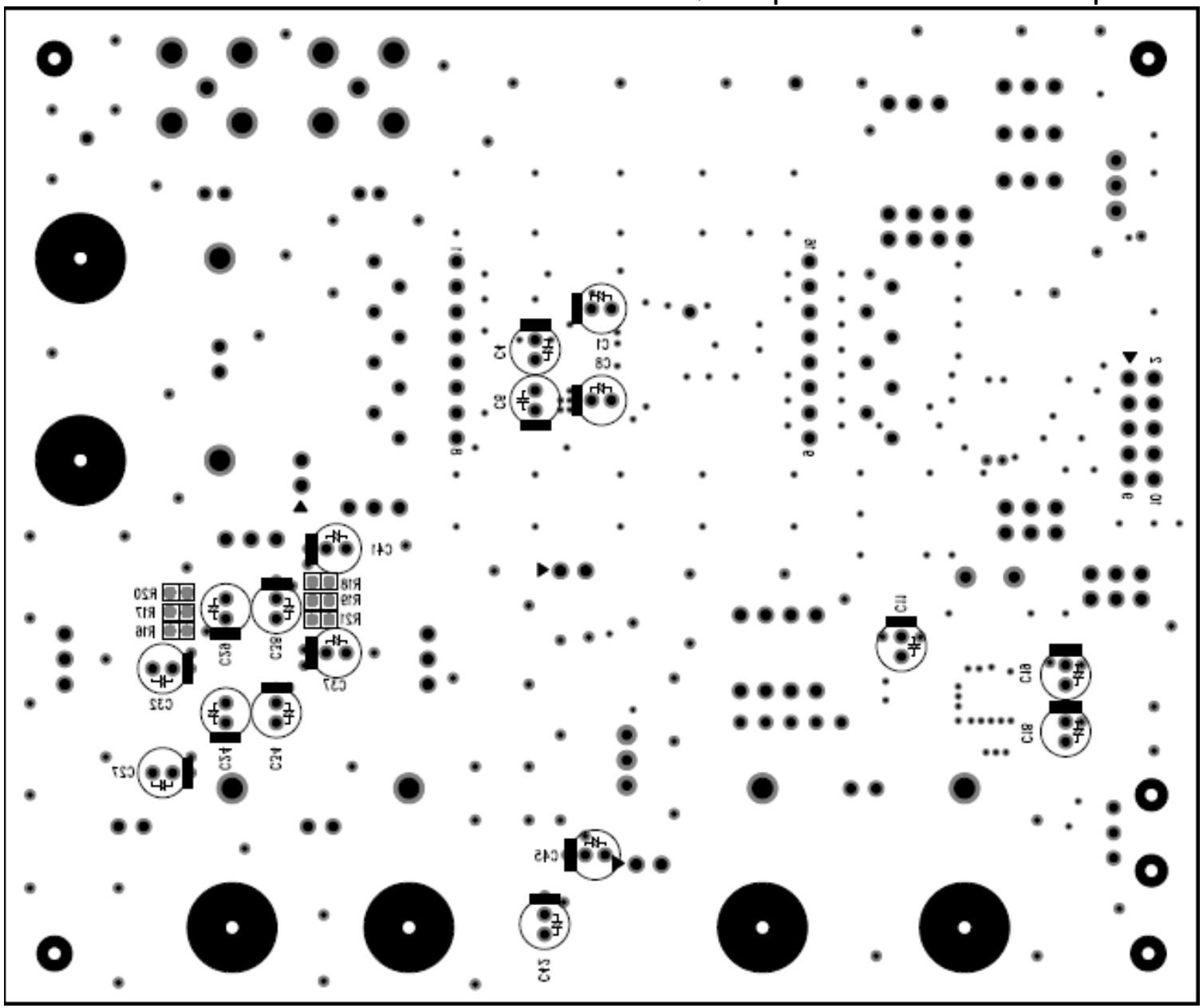
AKD5720-A Rev.1　Pattern View

Silk View of Component Side
（Perspective View of Component Side）

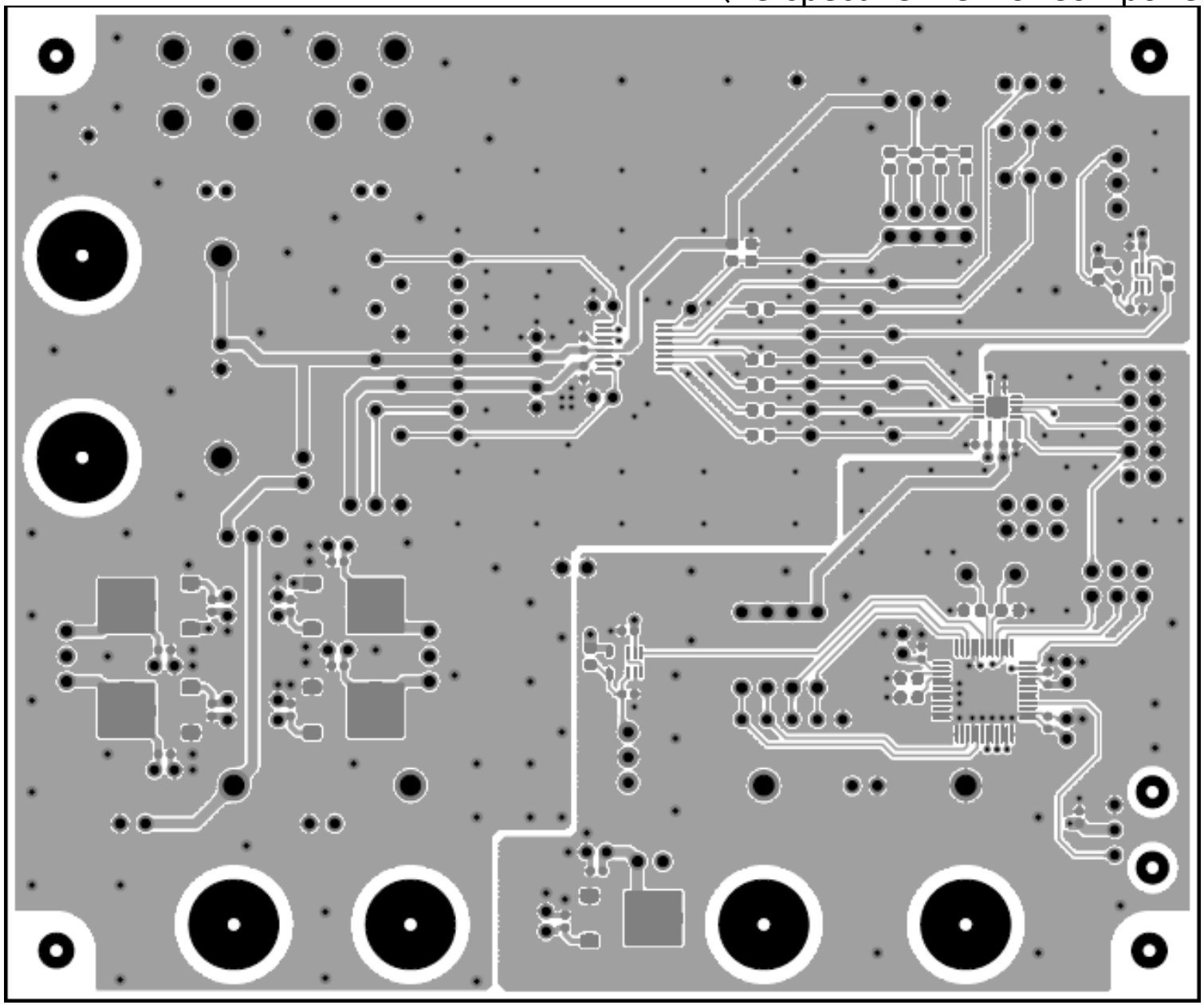


AKD5720-A Rev.1　Pattern View　　Silk View of Solder Side
（Perspective View of Component Side）



AKD5720-A Rev.1　Pattern View

Pattern View of Component Side
（Perspective View of Component Side）



AKD5720-A Rev.1　Pattern View

Pattern View of Solder Side
（Perspective View of Component Side ）