GENERAL DESCRIPTION

The AKD5730-A is an evaluation board for AK5730VQ which have a 4-channel differential ADC with SAR ADC for DC measurement. It is possible to control the setting of the board via an USB port. Stereo mini jack supports inputs of Line and Microphone. This board also has a digital interface and can achieve the interface with a digital audio system through an optical connector.

Ordering guide

AKD5730-A --- Evaluation board for AK5730VQ
USB cable and control software are packed with this board

FUNCTION

- Analog audio input: Stereo-mini jack (x4)
- Digital audio output: Optical (x1), External (x1)
- USB port for the board control

figure 1.AKD5730-A Block Diagram
**Description**

1. J1,J2,J3,J4 (Analog data)
   Stereo-mini jack. Used for Analog audio input.

2. J6,J7,J8,J9,J10 (Power supply)
   The AK5730 can be powered by external power supply or by Regulator (T1,T2) on the evaluation board.

3. PORT1/PORT2 (Digital Data)
   PORT1 : DSP output connector
   PORT2 : Optical output connector

4. PORT3 (USB Port)
   A computer can control AK5730 with the AK5730 control software through this USB port.

5. U1 (AK5730)
   4-Channel Differential Audio ADC for Mic & Line Inputs
(6) U2 (AK4118A)
AK4118A is DIT, which transmits digital data of AK5730.

(7) U5 (PIC18F4550)
USB control chip. It is possible to set up the registers of AK5730 with PC via the USB port.

(8) SW1 (Toggle switch)
“H” : PDN of AK5730 is Hi
“L” : PDN of AK5730 is Lo

(9) SW2 (Toggle switch)
“H” : PDN of AK4118A is Hi
“L” : PDN of AK4118A is Lo

(10) SW3 (Dip switch)
Setting of AK5730 and AK4118A
Refer to Table 4.

(11) LE1 (Red LED)
LE1 is the sign of output for INT pin.
“H” : Turn off
“L” : Turn on
Evaluation Board Manual

■ Operation Sequence

1) Set up the Power Supply Lines.

2) Setup the Audio I/F Evaluation Mode.

   (1) Evaluation of A/D using DIT of AK4118A.
   (1-1) Slave Mode (Default)
   (1-2) Master Mode
   (1-3) PLL Slave Mode

   (2) Evaluation of A/D using DSP.
   (2-1) Slave Mode
   (2-2) Master Mode
   (2-3) PLL Slave Mode

3) Jumper pins and SW Setting.

   (1) Setting of other jumper pins.

   (2) Setting of SW.

4) Power on.
1) Set up the power Supplies

(1) When AVDD, DVDD, and D3.3V are supplied from the regulator. <Default>

Set up the power supply lines.

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Setting</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>Yellow</td>
<td>Open</td>
<td>+5V Power supply for the regulator.</td>
</tr>
<tr>
<td>AVDD</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>DVDD</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>+D3.3V</td>
<td>Red</td>
<td>Open</td>
<td>Not used. Supplied through regulator</td>
</tr>
<tr>
<td>AGND</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK5730</td>
</tr>
<tr>
<td>DGND</td>
<td>Black</td>
<td>0V</td>
<td>Digital ground for Logic circuit.</td>
</tr>
</tbody>
</table>

Table 1 Setup of power supply

(2) When AVDD, DVDD, and D3.3V are supplied from the power supply connectors.

Set up the power supply lines.

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Setting</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>Yellow</td>
<td>Open</td>
<td>Not used.</td>
</tr>
<tr>
<td>AVDD</td>
<td>Red</td>
<td>+3.3V</td>
<td>Power supply for AVDD of AK5730</td>
</tr>
<tr>
<td>DVDD</td>
<td>Red</td>
<td>+3.3V</td>
<td>Power supply for DVDD of AK5730.</td>
</tr>
<tr>
<td>+D3.3V</td>
<td>Red</td>
<td>+3.3V</td>
<td>Power supply for logic circuit</td>
</tr>
<tr>
<td>AGND</td>
<td>Black</td>
<td>0V</td>
<td>Ground for AK5730</td>
</tr>
<tr>
<td>DGND</td>
<td>Black</td>
<td>0V</td>
<td>Digital ground for Logic circuit.</td>
</tr>
</tbody>
</table>

Table 2 Setup of power supply
2) Setup the Audio I/F Evaluation Mode.

In case of using the AK4118A when evaluating the AK5730, the audio interface format of the AK5730 and AK4118A must be matched. Refer to the datasheet for audio interface format of AK5730, and audio interface format of AK4118A. (Table 4) The AK4118A operates at sampling frequency of 32 kHz or more. If the sampling frequency is lower than 32 kHz, please use other mode. Refer to the datasheet for register setting of the AK5730.

(1) Evaluation of A/D using DIT of AK4118A.

(1-1) Slave Mode. (Default).

PORT2 (TOTX) is used.

- PORT1: Open
- AK5730: Slave mode
- AK4118A: Master mode
- SW3(4118-DIF/ 5730-MSN) : “Lo”

MCLK, BICK and LRCK are supplied from AK4118A to AK5730. PORT2 outputs optical data of AK5730 through AK4118A. MCLK can be selected between 512fs and 256fs by JP10. SDTO1 and SDTO2 can be selected by JP11.

(1-2) Master Mode

PORT2 (TOTX) is used.

- PORT1: Open
- AK5730: Master mode
- AK4118A: Slave mode
- SW3(4118-DIF/ 5730-MSN) : “Hi”

MCLK is supplied from AK4118A or X1 to AK5730. LRCK, BICK, SDTO1 and SDTO2 of AK5730 are outputs to AK4118A. PORT2 outputs optical data of AK5730 through AK4118A. MCLK can be selected between 512fs and 256fs by JP10. SDTO1 and SDTO2 can be selected by JP11.
(1-3) PLL Slave Mode (BICK 64fs input mode only)

PORT2 (TOTX) is used.

- PORT1: Open
- AK5730: PLL slave mode
- AK4118A: Master mode
- SW3(4118-DIF/ 5730-MSN): “Lo”

BICK and LRCK are supplied from AK4118A to AK5730. PORT2 outputs optical data of AK5730 through AK4118A. MCLK is generated from BICK. SDTO1 and SDTO2 can be selected by JP11.

(2) Evaluation of A/D using PORT1 (DSP)

(2-1) Slave Mode.

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5730: Slave mode
- SW3(4118-DIF/ 5730-MSN): “Lo”

MCLK, BICK and LRCK are supplied from PORT1 to AK5730. SDTO1 and SDTO2 of AK5730 are outputs to PORT1.
(2-2) Master Mode.

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5730: Master mode
- SW3(4118-DIF/ 5730-MSN) : “Hi”

MCLK is supplied from PORT1. LRCK, BICK, SDTO1 and SDTO2 of AK5730 are outputs to PORT1.

(2-3) PLL Slave Mode.

PORT1 (DSP) is used.

- SW2: “Lo” (AK4118A is not used)
- AK5730: PLL slave mode
- SW3(4118-DIF/ 5730-MSN) : “Lo”

BICK and LRCK are supplied from PORT1. SDTO1 and SDTO2 of AK5730 are outputs to PORT1. MCLK is generated from BICK.
3) Jumper pins and SW Setting.

(1) Setting of other jumper pins.

JP1, JP2 (AIN1 selector): The selection of input signal to IN1P pin and IN1N pin.
- • JP1 dif : Full differential mode. < Default >
  sin : Single-ended mode.
- • JP2 open : Full differential mode. < Default >
  short : Single-ended mode.

JP3, JP4 (AIN2 selector): The selection of input signal to IN2P pin and IN2N pin.
- • JP3 dif : Full differential mode. < Default >
  sin : Single-ended mode.
- • JP4 dif : Full differential mode. < Default >
  sin : Single-ended mode.

JP5, JP6 (AIN3 selector): The selection of input signal to IN3P pin and IN3N pin.
- • JP5 dif : Full differential mode. < Default >
  sin : Single-ended mode.
- • JP6 open : Full differential mode. < Default >
  short : Single-ended mode.

JP7, JP8 (AIN4 selector): The selection of input signal to IN4P pin and IN4N pin.
- • JP7 dif : Full differential mode. < Default >
  sin : Single-ended mode.
- • JP8 dif : Full differential mode. < Default >
  sin : Single-ended mode.

JP9 (TDM selector): The selection of TDM mode.
- • JP9 open : When using TDM-mode.
  short : When not using TDM-mode. < Default >

(2) Setting of SW.

Upper-side is “ON(H)” and lower-side is “OFF(L)”.

[SW3] (SW DIP-6): Mode setting for AK5730 and AK4118A.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5730-SPI</td>
<td>SPI</td>
<td>I2C</td>
<td>OFF</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>4118DIF1/</td>
<td></td>
<td>See Table 4</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>5730-MSN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4118-DIF0</td>
<td></td>
<td>See Table 5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>4118-OCKS0</td>
<td></td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>6</td>
<td>4118-OCKS1</td>
<td></td>
<td>See Table 6</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Table 3. Mode setting for AK5730 and AK4118A
Table 4. Audio I/F Format Setting for AK4118A

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>ON (&quot;H&quot;)</th>
<th>OFF (&quot;L&quot;)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4118DIF/5730-MSN</td>
<td>AK5730 : “Master Mode”</td>
<td>AK5730 : “Slave Mode”</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AK4118A : “Slave Mode”</td>
<td>AK4118A : “Master Mode”</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. Master Clock setting for AK4118A

<table>
<thead>
<tr>
<th>No.</th>
<th>OCKS1</th>
<th>OCKS0</th>
<th>MCKO1</th>
<th>MCKO2</th>
<th>X’tal</th>
<th>fs (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>256fs</td>
<td>256fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>256fs</td>
<td>128fs</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>512fs</td>
<td>256fs</td>
<td>512fs</td>
<td>48 kHz</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>128fs</td>
<td>64fs</td>
<td>128fs</td>
<td>192 kHz</td>
</tr>
</tbody>
</table>

Table 6. Master Clock setting for AK4118A

4) Power on.

Upper-side is “H” and lower-side is “L”.

[SW1] (5730-PDN) : The AK5730 should be reset once bringing “L” upon power-up. Keep “H” during normal operation.

[SW2] (4118-PDN) : The AK4118A should be reset once bringing “L” upon power-up. Keep “H” during normal operation.
Control Soft Manual

Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect Evaluation board to PC with USB cable.
   USB control is recognized as HID (Human Interface Device) on the PC.  
   When it can not be recognized correctly please reconnect Evaluation board to PC with USB cable.
3. Proceed evaluation by following the process below.

[Support OS]
Windows XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
64bit OS’s are not supported

Operation Screen

1. Start up the control program following the process above.
2. After the evaluation board’s power is supplied, the AK5730 must be reset once bring S1 (AK5730-PDN) “L” to “H”.
3. The operation screen is shown below
Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to PC with USB cable
   Click this button after the control soft starts up when connecting to PC with USB cable.

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: [All Reg Write] dialog box is popped up.

8. [Data R/W]: [Data R/W] dialog box is popped up.

9. [Read]: Reading current register settings and display on to the Register area (on the right of the main window).
   This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.
# Tab Functions

## 1. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray).

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

![Figure 3. Window of [REG]](attachment:image.png)
1-1. [Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When the checkbox is checked, the data will be “H” or “1”. When the checkbox is not checked, the data will be “L” or “0”. Click [OK] to write setting values to the registers, or click [Cancel] to cancel this setting.

![Register Set](image)

Figure 4. Window of [Register Set]

1-2. [Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute a register read.

After register reading, the display will be updated regarding to the register status. Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red). Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray).

Please be aware that button statuses will be changed by a Read command.
2. [Tool]: Testing Tools

Evaluation testing tools are available in this tab. Click buttons for each testing tool.

Figure 5. Window of [Tool]
2-1. [Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button in the Test tab to open a repeat test dialog shown below. Repeat writing test can be executed by this dialog.

Figure 6. Window of [Repeat Test]

[Start] Button: Starts the repeat test.
A dialog for saving a file of the test result will open when clicking this button.
Name the file.
Test will start after specifying a saving file.

[Close] Button: Closes this dialog and finishes the process.

[Address] Box: Data writing address in hexadecimal numbers.

[Start Data] Box: Start data in hexadecimal numbers.

[End Data] Box: End data in hexadecimal numbers.

[Step] Box: Data write step interval.

[Repeat Count] Box: Repeat count of the test writing.

[Up and Down] Box: Data write flow is changed as below.

- Checked: Writes in step interval from the start data to the end data and turn back from the end data to the start data.
  [Example] Start Data = 00, End Data = 05, Step = 1, [...] for 1 count.
  Data flow: [00→01→02→03→04→05→04→03→02→01→00] × Repeat Count Number

- Not checked: Writes in step interval from the start data to the end data and finishes writing.
  [Example] Start Data = 00, End Data = 05, Step = 1, [...] for 1 count.
  Data flow: [00→01→02→03→04→05] × Repeat Count Number

[Sampling Frequency] Box: Selects sampling frequency 44.1kHz/48kHz

[Count] Box: Indicates the count number during a repeat test.

[Lch Level] Box: Indicates the Lch Level during a repeat test.
2-2. [Loop Setting]: Loop Dialog

Click [Loop Setting] button in the Tool tab to open loop setting dialog as shown below. Writing test can be executed.

![Loop Dialog](image)

Figure 7. Window of [ Loop ]

- **[ OK ] Button**: Starts the test.
- **[ Cancel ] Button**: Closes the dialog and finishes the process.
- **[ Address ] Box**: Data writing address in hexadecimal numbers.
- **[ Start Data ] Box**: Start data in hexadecimal numbers.
- **[ End Data ] Box**: End data in hexadecimal numbers.
- **[ Interval ] Box**: Data write interval time.
- **[ Step ] Box**: Data write step interval.
- **[ Mode Select ] Box**: Mode select check box.

*Checked*: Writes in step interval from the start data to the end data and turn back from the end data to the start data.

[Example] Start Data = 00, End Data = 05, Step = 1
Data flow: 00→01→02→03→04→05→04→03→02→01→00

*Not Checked*: Writes in step interval from the start data to the end data and finishes writing.

[Example] Start Data = 00, End Data = 05, Step = 1
Data flow: 00→01→02→03→04→05
1. [All Req Write]: All Reg Write dialog box

Click [All Reg Write] button in the main window to open register setting files. Register setting files saved by [SAVE] button can be applied.

[Open (left)]: Selects a register setting file (*.akr).
[Write]: Executes register writing by the setting of selected file.
[Write All]: Executes all register writings. Selected files are executed in descending order.

[Help]: Opens a help window.
[Save]: Saves a register setting file assignment. The file name is “*.mar”.
[Open (right)]: Opens a saved register setting file assignment “*. mar”.
[Close]: Closes the dialog box and finish the process.
~ Operating Suggestions ~

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

![Data Read/Write dialog box](image)

- [Address] Box: Input data address in hexadecimal numbers for data writing.
- [Data] Box: Input data in hexadecimal numbers.
- [Mask] Box: Input mask data in hexadecimal numbers. This is “AND” processed input data.
- [Write]: Writes the data generated from Data and Mask values to the address specified by “Address” box.
- [Read]: Reads data from the address specified by “Address” box. The result will be shown in the Read Data Box in hexadecimal numbers.
- [Close]: Closes the dialog box and finishes the process. Data writing can be cancelled by this button instead of executing a write command.

*The register map will be updated after executing [Write] or [Read] commands.
## MEASUREMENT RESULT

### Measurement condition
- Measuring instrument: Audio Precision System Two Cascade
- **MCLK**: 512fs
- **BICK**: 64fs
- **fs**: 48 kHz
- **Bit**: 24bit
- Power Supply (REG): AVDD = 3.3V, DVDD = 3.3V
- Measurement mode: Slave mode
- Temperature: Room temperature

### Measurement result

<table>
<thead>
<tr>
<th></th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>ADC1</th>
<th>ADC2</th>
<th>ADC3</th>
<th>ADC4</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S/N (N+D)$ (72dBFS Differential)</td>
<td>86</td>
<td>92</td>
<td>-</td>
<td>93.6</td>
<td>93.1</td>
<td>94.0</td>
<td>94.0</td>
<td>dB</td>
</tr>
<tr>
<td>$S/N (N+D)$ (72dBFS Single-ended)</td>
<td>86</td>
<td>92</td>
<td>-</td>
<td>92.0</td>
<td>93.0</td>
<td>92.8</td>
<td>93.0</td>
<td>dB</td>
</tr>
<tr>
<td>$S/N (D+D)$ (72dBFS Gain mode)</td>
<td>86</td>
<td>92</td>
<td>-</td>
<td>93.1</td>
<td>93.2</td>
<td>93.5</td>
<td>93.4</td>
<td>dB</td>
</tr>
<tr>
<td>D-Range (60dBFS, A-weighted Differential)</td>
<td>93</td>
<td>100</td>
<td>-</td>
<td>100.0</td>
<td>100.3</td>
<td>100.2</td>
<td>100.0</td>
<td>dB</td>
</tr>
<tr>
<td>D-Range (60dBFS, A-weighted Gain mode)</td>
<td>92</td>
<td>98</td>
<td>-</td>
<td>99.0</td>
<td>99.1</td>
<td>99.0</td>
<td>99.0</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted Differential)</td>
<td>93</td>
<td>100</td>
<td>-</td>
<td>100.0</td>
<td>100.3</td>
<td>100.1</td>
<td>100.3</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (10mVrms input, A-weighted Gain mode)</td>
<td>57</td>
<td>63</td>
<td>-</td>
<td>63.9</td>
<td>64.2</td>
<td>64.1</td>
<td>63.9</td>
<td>dB</td>
</tr>
</tbody>
</table>
[ADC Plots]

Differential mode

Red: IN1P/IN1N → ADC1 → SDTO1
Blue: IN2P/IN2N → ADC2 → SDTO1

FFT (fin=1 kHz, Input level = -0.5dBFS)

FFT (fin=1 kHz, Input level = -60dBFS)
FFT (fin=1 kHz, Input level = No Input)

THD+N VS. Input level (fin=1 kHz)
THD+N VS. Input Freq (Input level = -0.5dBFS)

Linearity (fin=1 kHz)
Frequency Response (Input level = -0.5dBFS)

Crosstalk (Input level = -0.5dBFS)
Single-ended mode
Red: IN1P → ADC1 → SDTO1
Blue: IN2P → ADC2 → SDTO1

FFT (fin=1 kHz, Input level = -0.5dBFS)

FFT (fin=1 kHz, Input level = -60dBFS)
FFT (fin=1 kHz, Input level = No Input)

THD+N VS. Input level (fin=1 kHz)
THD+N VS. Input Freq (Input Level = -0.5dBFS)

Linearity (fin=1 kHz)
Frequency Response (Input level = -0.5dBFS)

Crosstalk (Input level = -0.5dBFS)
Gain mode
Red: IN1P/ IN1N → ADC1 → SDTO1
Blue: IN2P/ IN2N → ADC2 → SDTO1

FFT (fin=1 kHz, Input level = -0.5 dBFS)

FFT (fin=1 kHz, Input level = -6 dBFS)
FFT (fin=1 kHz, Input level =10mVrms)

THD+N VS. Input level (fin=1 kHz)
THD+N VS. Input Freq (Input Level = -0.5dBFS)

Linearity (fin=1 kHz)
Frequency Response (Input level = -0.5dBFS)

Crosstalk (Input level = -0.5dBFS)
IMPORTANT NOTICE

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  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.

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**Revision History**

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