AK4621

24-Bit 192kHz Stereo Audio CODEC

GENERAL DESCRIPTION

The AK4621 is a high performance 24-bit CODEC that supports up to 192kHz recording and playback. The on-board analog-to-digital converter has a high dynamic range due to AKM's Enhanced Dual-Bit architecture. The DAC utilizes AKM's Advanced Multi-Bit architecture that achieves low out-of-band noise and high jitter tolerance through the use of Switched Capacitor Filter (SCF) technology. The AK4621 is ideal for Pro Audio sound cards, Digital Audio Workstations, DVD-R, hard disk, CD-R recording/playback systems, and musical instrument recording.

FEATURES

□ 24-bit 2-channel ADC
- **Full Differential Inputs**
- **Selectable Digital Filter**
  1. **ADC Sharp Roll Off Filter (GD=39/fs)**
     Passband: 0 ~ 21.8kHz (@fs=48kHz)
     Stopband Attenuation: 100dB
  2. **ADC Short Delay Sharp Roll Off Filter (GD=14/fs)**
     Passband: 0 ~ 21.7kHz (@fs=48kHz)
     Stopband Attenuation: 80dB
- **S/(N+D): 102dB**
- **S/N: 115dB**
- **Digital High-pass Filter for Offset Cancellation**
- **Overflow Flag**
- **Audio Interface Format: MSB justified or I^2S**

□ 24-bit 2-channel DAC
- **Selectable Digital Filter**
  1. **DAC Sharp Roll Off Filter (GD=27/fs)**
     Passband: 0 ~ 21.8kHz (@fs=48kHz)
     Stopband Attenuation: 70dB
  2. **DAC Slow Roll Off Filter (GD=27/fs)**
     Passband: 0 ~ 8.9kHz (@fs=48kHz)
     Stopband Attenuation: 73dB
  3. **DAC Short Delay Sharp Roll Off Filter (GD=7/fs)**
     Passband: 0 ~ 21.8kHz (@fs=48kHz)
     Stopband Attenuation: 70dB
- **Switched-cap Low Pass Filter**
- **Differential Outputs**
- **S/(N+D): 100dB**
- **S/N: 115dB**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz Sampling**
- **Output Digital Attenuator: 0dB ~ – 72dB, Linear 256 + 16steps**
- **Zero Detection Function**
- **Audio Interface Format: MSB justified, LSB justified, I^2S**

□ High Jitter Tolerance
□ Sampling Rate: 32kHz ~ 216kHz
□ μP Interface: 3-wire Serial Interface
□ Master Clock: 128fs/192fs/256fs/384fs/512fs/768fs/1024fs

□ **Power Supply**
Analog: 4.75 ~ 5.25V (typ. 5.0V)
Digital: 3.0 ~ 3.6V (typ. 3.3V)
Digital I/O: DVDD ~ 5.25V (typ. 5.0V)
□ **Package: 30-pin VSOP**
□ **Ta: -10 ~ 70 °C**

■ Block Diagram

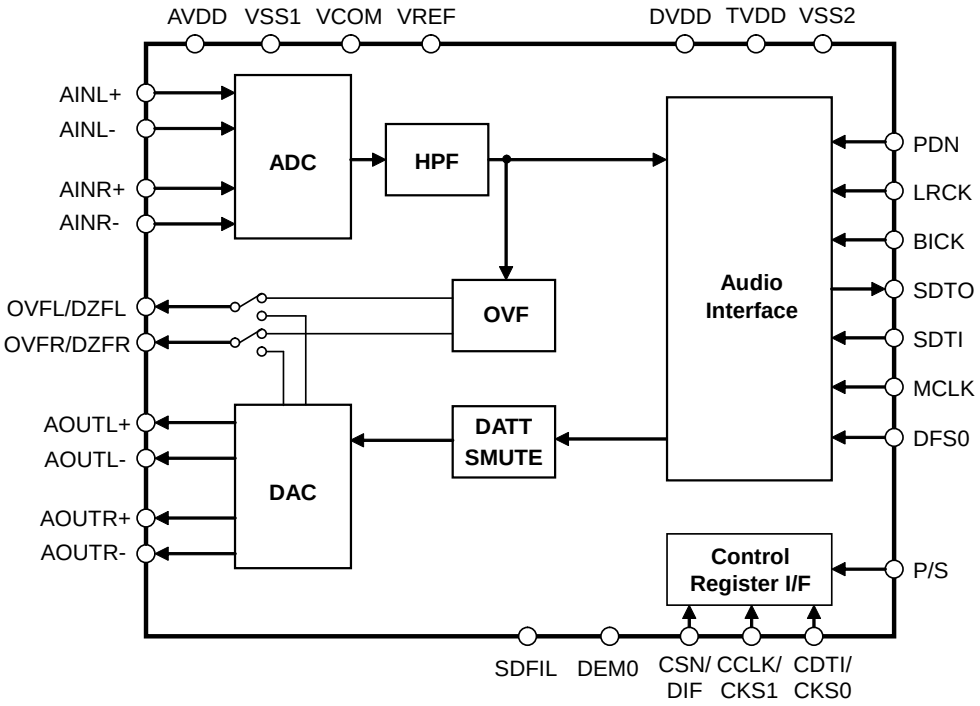
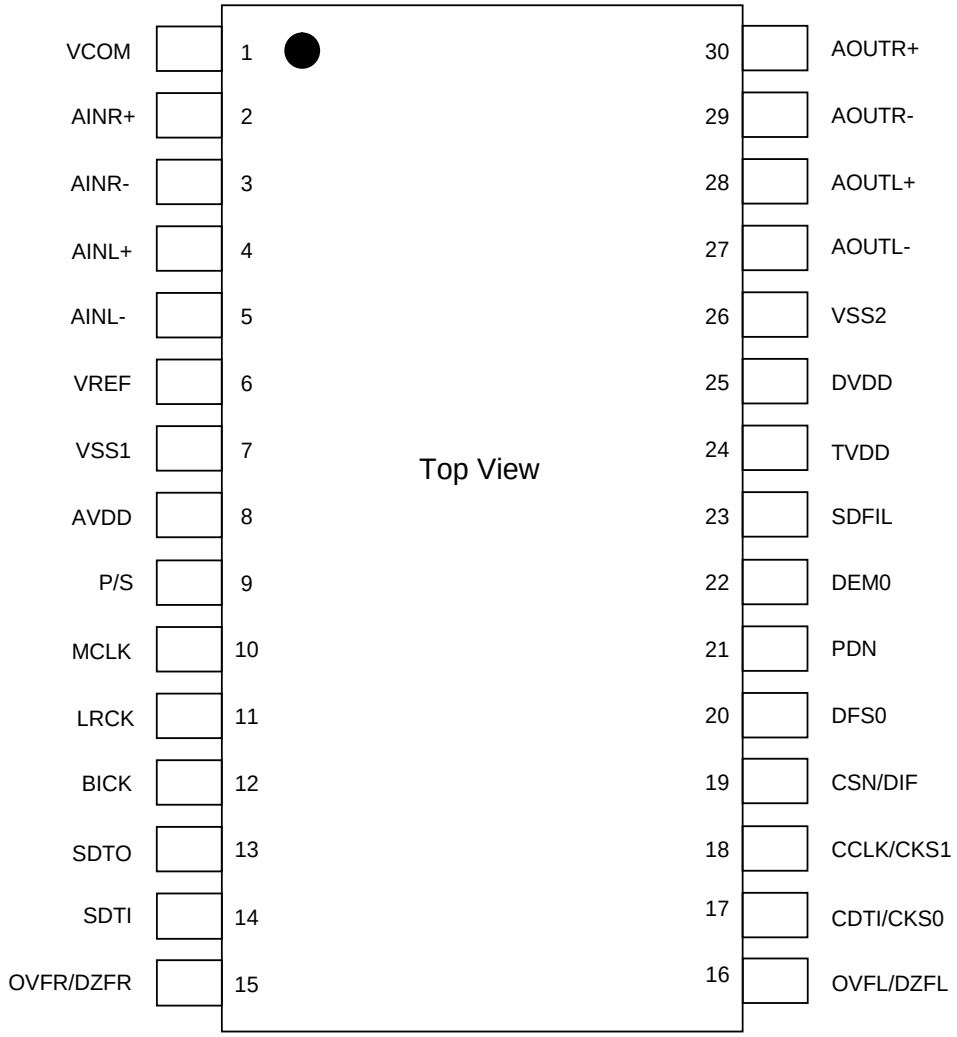


Figure 1. Block Diagram

■ Ordering Guide

AK4621EF	–10 ~ +70°C	30-pin VSOP (0.65mm pitch)
AKD4621	Evaluation board for AK4621	

■ Pin Layout



■ Compatibility with AK4620B

1. Function

Function	AK4620B		AK4621		
Max fs	216kHz		←		
ADC Inputs	Single-ended	Differential	Differential		
Input analog PGA	0 ~ +18dB 0.5dB/step	-	-		
Input digital ATT	Mute,-63.5dB ~ 0dB 0.5dB/step	Mute,-63.5dB ~ 0dB 0.5dB/step	-		
ADC S/(N+D)	90dB	100dB	102dB		
ADC DR, S/N	110dB	113dB	115dB		
ADC Digital Filter Type	Sharp Roll-off		Sharp Roll-off		Short Delay Sharp Roll-off
ADC Digital Filter SA	100dB		100dB		80dB
ADC Digital Filter GD	43.2/fs		39/fs		14/fs
DAC S/(N+D)	97dB (0dBFS)		100dB (-1dBFS)		
DAC DR, S/N	115dB		←		
DAC Digital Filter Type	Sharp Roll-off	Slow Roll-off	Sharp Roll-off	Slow Roll-off	Short Delay Sharp Roll-off
DAC Digital Filter SA	75dB	72dB	70dB	73dB	70dB
DAC Digital Filter GD	28/fs	28/fs	27/fs	27/fs	7/fs
Output digital Attenuator	Mute, -48dB ~ 0dB Linear 256 steps	Mute, -48dB ~ 0dB Linear 256 steps	Mute, -72dB ~ 0dB Linear 16 + 256 steps		
DAC DSD mode	X		-		
DAC Zero-data detection	X		←		
Parallel Mode	X		←		

X: Available, -: Not Available

2. Register (difference from AK4620B)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	SLOW	DZFB	ZOE	ZOS	SDDA	PWVR	PWAD	PWDA
01H	Reset Control	~~D/P~~	~~DCKS~~	~~DCKB~~	SDAD	~~AML~~	~~AMR~~	RSTAD	RSTDA
02H	Clock and Format Control	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0
03H	Deem and Volume Control	SMUTE	HPRN	HPLN	~~ZCEI~~	~~ZTM1~~	~~ZTM0~~	DEM1	DEM0
04H	Reserved	~~IATTL7~~	~~IATTL6~~	~~IATTL5~~	~~IATTL4~~	~~IATTL3~~	~~IATTL2~~	~~IATTL1~~	~~IATTL0~~
05H	Reserved	~~IATTR7~~	~~IATTR6~~	~~IATTR5~~	~~IATTR4~~	~~IATTR3~~	~~IATTR2~~	~~IATTR1~~	~~IATTR0~~
06H	Lch DATT Control	DATTL7	DATTL6	DATTL5	DATTL4	DATTL3	DATTL2	DATTL1	DATTL0
07H	Rch DATT Control	DATTR7	DATTR6	DATTR5	DATTR4	DATTR3	DATTR2	DATTR1	DATTR0
08H	Lch Extension DATT Control	0	0	EXTE	0	EATTL3	EATTL2	EATTL1	EATTL0
09H	Rch Extension DATT Control	0	0	0	0	EATTR3	EATTR2	EATTR1	EATTR0

These bits were added in the AK4621.
These bits were deleted in the AK4621.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, (AVDD)/2 Bias voltage of ADC inputs and DAC outputs.
2	AINR+	I	Rch Positive Input Pin
3	AINR-	I	Rch Negative Input Pin
4	AINL+	I	Lch Positive Input Pin
5	AINL-	I	Lch Negative Input Pin
6	VREF	I	Voltage Reference Input Pin, AVDD Used as a voltage reference by ADC & DAC. VREF is connected externally to AVDD.
7	VSS1	-	Analog Ground Pin
8	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
9	P/S	I	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
10	MCLK	I	Master Clock Input Pin
11	LRCK	I	Input/Output Channel Clock Pin
12	BICK	I	Audio Serial Data Clock Pin
13	SDTO	O	Audio Serial Data Output Pin
14	SDTI	I	Audio Serial Data Input Pin
15	OVFR	O	Rch Over Flow Flag Pin (in Parallel mode or when ZOS bit="0" in Serial Mode)
	DZFR	O	Rch Zero Detection Flag Pin (when ZOS bit="1" in Serial Mode)
16	OVFL	O	Lch Over Flow Flag Pin (in Parallel mode or when ZOS bit="0" in Serial Mode)
	DZFL	O	Lch Zero Detection Flag Pin (when ZOS bit="1" in Serial Mode)
17	CDTI	I	Control Data Input Pin (in Serial Mode)
	CKS0	I	Master Clock Select Pin (in Parallel Mode)
18	CCLK	I	Control Data Clock Pin (in Serial Mode)
	CKS1	I	Master Clock Select Pin (in Parallel Mode)
19	CSN	I	Chip Select Pin in Serial Mode (in Serial Mode)
	DIF	I	Digital Audio Interface Select Pin (in Parallel Mode) "L": 24bit MSB justified, "H": I2S compatible
20	DFS0	I	Double Speed Sampling Mode Pin
21	PDN	I	Power-Down Mode Pin "L": Power down reset and initialize the control register, "H": Power up
22	DEM0	I	De-emphasis Control Pin
23	SDFIL	I	Digital Filter Select Pin "L": Short Delay Sharp Roll Off Filter (ADC), Short Delay Sharp Roll Off Filter (DAC) "H": Sharp Roll Off Filter (ADC), Sharp Roll Off Filter (DAC)
24	TVDD	-	Digital I/O Power Supply Pin, DVDD ~ 5.25V
25	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
26	VSS2	-	Digital Ground Pin
27	AOUTL-	O	Lch Negative Analog Output Pin
28	AOUTL+	O	Lch Positive Analog Output Pin
29	AOUTR-	O	Rch Negative Analog Output Pin
30	AOUTR+	O	Rch Positive Analog Output Pin

Note 1. All digital input pins (P/S, MCLK, LRCK, BICK, SDTI, CDTI/CKS0, CCLK/CKS1, CSN/DIF, DFS0, PDN, DEM0 and SDFIL) must not be left floating.

■ Handling of Unused Pin

The unused I/O pin must be processed appropriately as below.

Classification	Pin Name	Setting
Analog Input	AINL+, AINL-	AINL+ pin is connected to AINL- pin.
	AINR+, AINR-	AINR+ pin is connected to AINR- pin.
Analog Output	AOUTL+, AOUTL-, AOUTR+, AOUTR-	These pins must be open.
Digital Output	OVFL/DZFL, OVFR/DZFR	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 2, Note 3)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	Digital I/O	TVDD	-0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 4. AINL+, AINL-, AINR+ and AINR- pins

Note 5. P/S, MCLK, LRCK, BICK, SDTI, CDTI/CKS0, CCLK/CKS1, CSN/DIF, DFS0, PDN, DEM0 and SDFIL pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 6)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	3.0	3.3	3.6	V
	Digital I/O	TVDD	DVDD	5.0	5.25	V
Voltage Reference		VREF	-	AVDD	-	V

Note 2. All voltages with respect to ground.

Note 6. The power up sequence among AVDD, DVDD and TVDD is not critical.
VREF is connected externally to AVDD.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5V, DVDD=3.3V, TVDD=5V; VSS1=VSS2=0V; VREF=AVDD; fs=48kHz; Signal Frequency =1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics:						
Resolution			-	-	24	Bits
Input Voltage		(Note 7)	±2.62	±2.82	±3.02	Vpp
Input Resistance		fs=48kHz	-	13	-	kΩ
		fs=96kHz	-	13	-	kΩ
		fs=192kHz	-	13	-	kΩ
S/(N+D)	fs=48kHz	-1dBFS	92	102	-	dB
	BW=20kHz	-60dBFS	-	52	-	dB
	fs=96kHz	-1dBFS	-	101	-	dB
	BW=40kHz	-60dBFS	-	48	-	dB
	fs=192kHz	-1dBFS	-	101	-	dB
	BW=40kHz	-60dBFS	-	48	-	dB
Dynamic Range	(-60dBFS with A-weighted)		-	115	-	dB
S/N	(A-weighted)		105	115	-	dB
Interchannel Isolation			90	110	-	dB
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 12)	-	20	-	ppm/°C
Power Supply Rejection		(Note 8)	-	50	-	dB
DAC Analog Output Characteristics:						
Parameter			**min**	**typ**	**max**	**Units**
Resolution			-	-	24	Bits
Dynamic Characteristics						
S/(N+D)	fs=48kHz	–1dBFS	90	100	-	dB
	BW=20kHz	–60dBFS	-	52	-	dB
	fs=96kHz	–1dBFS	-	97	-	dB
	BW=40kHz	–60dBFS	-	49	-	dB
	fs=192kHz	–1dBFS	-	97	-	dB
	BW=40kHz	–60dBFS	-	49	-	dB
Dynamic Range (–60dBFS with A-weighted)		(Note 9, Note 10)	-	115	-	dB
S/N	(A-weighted)	(Note 10, Note 11)	107	115	-	dB
Interchannel Isolation (1kHz)			90	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 12)	-	20	-	ppm/°C
Output Voltage		(Note 13)	±2.6	±2.8	±3.0	Vpp
Load Capacitance			-	-	25	pF
Load Resistance		(Note 14)	2	-	-	kΩ

Note 7. Full scale (0dB) of the input voltage. Vin (typ) = ±2.82Vpp x VREF/5.
Note 8. PSR is applied to AVDD, DVDD, TVDD with 1kHz, 50mVpp. VREF pin is held a constant voltage.
Note 9. 100dB at 16bit data and 114dB at 20bit data.
Note 10. By Figure 20. External LPF Circuit Example 2.
Note 11. S/N does not depend on input bit length.
Note 12. The voltage on VREF is held +5V externally.
Note 13. Full scale voltage (0dB). Output voltage scales with the voltage of VREF.
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = 5.6Vpp x VREF/5.
Note 14. For AC-load.

Parameter			min	typ	max	Units
Power Supplies						
Power Supply Current						
	Normal Operation (PDN pin = "H")					
		AVDD	-	34	51	mA
		DVDD+TVDD (fs=48kHz)	-	11	-	mA
		(fs=96kHz)	-	20	30	mA
		(fs=192kHz)	-	27	41	mA
	Power-down mode (PDN pin = "L") (Note 15)					
		AVDD	-	10	100	μA
		DVDD+TVDD	-	10	100	μA

Note 15. All digital input pins are held TVDD or VSS2.

ADC SHARP ROLL OFF FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Normal Speed Mode; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.005dB	PB	0	-	21.8	kHz
	–0.02dB		-	22.0	-	kHz
	–0.06dB		-	22.3	-	kHz
	–6.0dB		-	24.0	-	kHz
Stopband (Note 16)		SB	26.5	-	-	kHz
Passband Ripple		PR	-	-	±0.005	dB
Stopband Attenuation		SA	100	-	-	dB
Group Delay (Note 17)		GD	-	39	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	1.0	-	Hz
	–0.1dB		-	6.5	-	Hz

ADC SHARP ROLL OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Double Speed Mode; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.005dB	PB	0	-	43.7	kHz
	–0.02dB		-	44.1	-	kHz
	–0.06dB		-	44.5	-	kHz
	–6.0dB		-	48.0	-	kHz
Stopband (Note 16)		SB	53.0	-	-	kHz
Passband Ripple		PR	-	-	±0.005	dB
Stopband Attenuation		SA	100	-	-	dB
Group Delay (Note 17)		GD	-	39	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	2.0	-	Hz
	–0.1dB		-	13.0	-	Hz

ADC SHARP ROLL OFF FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Quad Speed Mode; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.005dB	PB	0	-	87.0	kHz
	–0.02dB		-	88.2	-	kHz
	–0.06dB		-	89.0	-	kHz
	–6.0dB		-	96.0	-	kHz
Stopband (Note 16)		SB	106.0	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	100	-	-	dB
Group Delay (Note 17)		GD	-	36	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	4.0	-	Hz
	–0.1dB		-	26.0	-	Hz

Note 16: The passband and stopband frequencies scale with fs. Each response refers to that of 1kHz

Note 17: The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC. If the signal is outputted to the SDTO pin, group delay is increased 0.5/fs from the above value.

ADC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Normal Speed Mode; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.01dB	PB	0	-	21.7	kHz
	–0.1dB		-	22.1	-	kHz
	–3.0dB		-	23.8	-	kHz
	–6.0dB		-	24.4	-	kHz
Stopband (Note 16)		SB	28.2	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	14	-	1/fs
Group Delay Distortion		ΔGD	-	±0.01	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	1.0	-	Hz
	–0.1dB		-	6.5	-	Hz

ADC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Double Speed Mode; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.01dB	PB	0	-	43.3	kHz
	–0.1dB		-	44.2	-	kHz
	–3.0dB		-	47.6	-	kHz
	–6.0dB		-	48.9	-	kHz
Stopband (Note 16)		SB	55.9	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	14	-	1/fs
Group Delay Distortion		ΔGD	-	±0.013	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	2.0	-	Hz
	–0.1dB		-	13.0	-	Hz

ADC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Quad Speed Mode; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	–0.01dB	PB	0	-	76.1	kHz
	–0.1dB		-	81.1	-	kHz
	–3.0dB		-	99.9	-	kHz
	–6.0dB		-	106.7	-	kHz
Stopband (Note 16)		SB	141.1	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	79	-	-	dB
Group Delay (Note 17)		GD	-	11	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 16)	–3dB	FR	-	4.0	-	Hz
	–0.1dB		-	26.0	-	Hz

DAC SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 48kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Normal Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.04dB	PB	0	-	21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 18)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	± 0.2	-	dB

DAC SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Double Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.04dB	PB	0	-	43.5	kHz
	-6.0dB		-	48.0	-	kHz
Stopband (Note 18)		SB	52.4	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	± 0.3	-	dB

DAC SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Quad Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "0")

Parameter		symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.02B	PB	0	-	87.0	kHz
	-6.0dB		-	95.9	-	kHz
Stopband (Note 18)		SB	105	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/-1	-	dB

Note 18. The passband and stopband frequencies scale with fs. Each response refers to that of 1kHz.

Note 19. Delay time caused by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

DAC SLOW ROLL OFF FILTER CHARACTERISTICS (fs = 48kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Normal Speed Mode; DEM = OFF; SLOW bit = "1", SDDA bit = "0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.07dB	PB	0	-	8.9	kHz
	-3.0dB		-	19.8	-	kHz
Stopband (Note 18)		SB	42.6	-	-	kHz
Passband Ripple		PR	-	-	±0.07	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	+0/-5	-	dB

DAC SLOW ROLL OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Double Speed Mode; DEM = OFF; SLOW bit = "1", SDDA bit = "0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.07dB	PB	0	-	17.7	kHz
	-3.0dB		-	39.5	-	kHz
Stopband (Note 18)		SB	85.1	-	-	kHz
Passband Ripple		PR	-	-	±0.07	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	+0/-4	-	dB

DAC SLOW ROLL OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Quad Speed Mode; DEM = OFF; SLOW bit = "1", SDDA bit = "0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.07dB	PB	0	-	35.5	kHz
	-3.0dB		-	79.0	-	kHz
Stopband (Note 18)		SB	170.7	-	-	kHz
Passband Ripple		PR	-	-	±0.07	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 19)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/-5	-	dB

DAC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 48kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Normal Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.04dB	PB	0	-	21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 18)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	± 0.2	-	dB

DAC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Double Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.03dB	PB	0	-	43.5	kHz
	-6.0dB		-	48.0	-	kHz
Stopband (Note 18)		SB	52.4	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	± 0.3	-	dB

DAC SHORT DELAY SHARP ROLL OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta = 25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; Quad Speed Mode; DEM = OFF; SLOW bit = "0", SDDA bit = "1")

Parameter		symbol	min	typ	max	Units
Digital Filter						
Passband (Note 18)	-0.02dB	PB	0	-	87.0	kHz
	-6.0dB		-	96.2	-	kHz
Stopband (Note 18)		SB	104.9	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 19)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/-1	-	dB

DC CHARACTERISTICS

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	TVDD	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=-100μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 3.6V, TVDD=DVDD ~ 5.25V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	8.192	-	55.296	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
LRCK Frequency (Note 20)					
Normal Speed Mode (DFS0="0", DFS1="0")	fsn	32	-	54	kHz
Double Speed Mode (DFS0="1", DFS1="0")	fsd	54	-	108	kHz
Quad Speed Mode (DFS0="0", DFS1="1")	fsq	108	-	216	kHz
Duty Cycle		45	-	55	%
PCM Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn	-	-	ns
Double Speed Mode	tBCK	1/64fsd	-	-	ns
Quad Speed Mode	tBCK	1/64fsq	-	-	ns
BICK Pulse Width Low	tBCKL	33	-	-	ns
Pulse Width High	tBCKH	33	-	-	ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	20	-	-	ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	20	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)	tLRS	-	-	20	ns
BICK "↓" to SDTO	tBSD	-	-	20	ns
SDTI Hold Time	tSDH	20	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns

Note 20. When the normal/double/quad speed modes are switched, the AK4621 must be reset by the PDN pin or RSTN bit.
Note 21. BICK rising edge must not occur at the same time as LRCK edge.

Parameter		Symbol	min	typ	max	Units
Control Interface Timing						
CCLK Period		tCCK	200	-	-	ns
CCLK Pulse Width Low		tCCKL	80	-	-	ns
Pulse Width High		tCCKH	80	-	-	ns
CDTI Setup Time		tCDS	50	-	-	ns
CDTI Hold Time		tCDH	50	-	-	ns
CSN "H" Time		tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"		tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"		tCSH	50	-	-	ns
Reset Timing						
PDN Pulse Width	(Note 22)	tPD	150	-	-	ns
RSTAD "↑" to SDTO Valid	(Note 23)	tPDV	-	516	-	1/fs

Note 22. The AK4621 can be reset by bringing the PDN pin "L".
Note 23. These cycles are the number of LRCK rising from RSTAD bit.

■ Timing Diagram

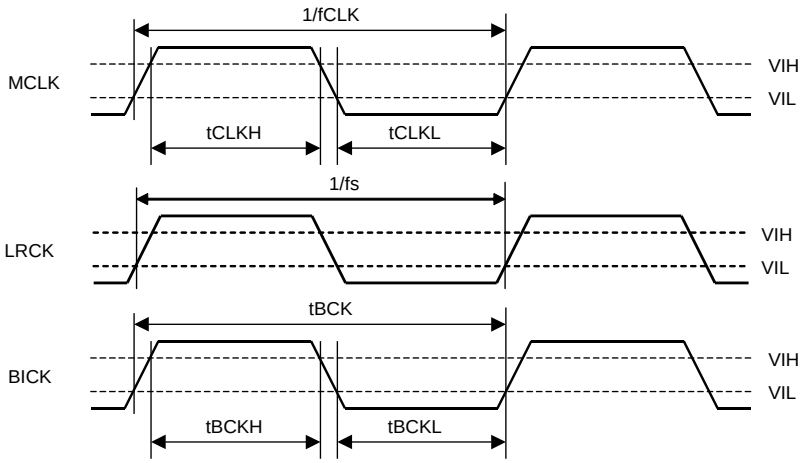


Figure 2. Clock Timing

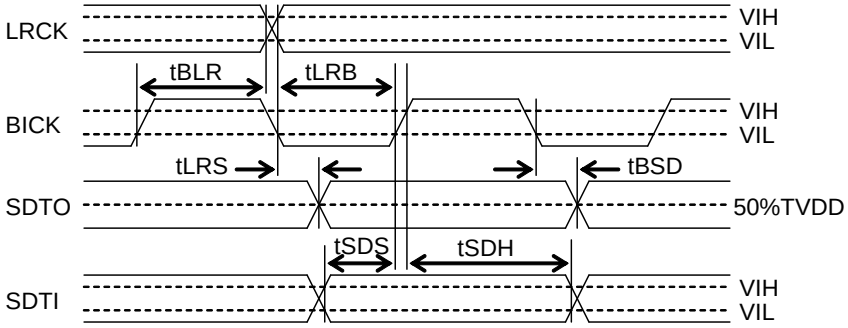


Figure 3. Audio Interface Timing

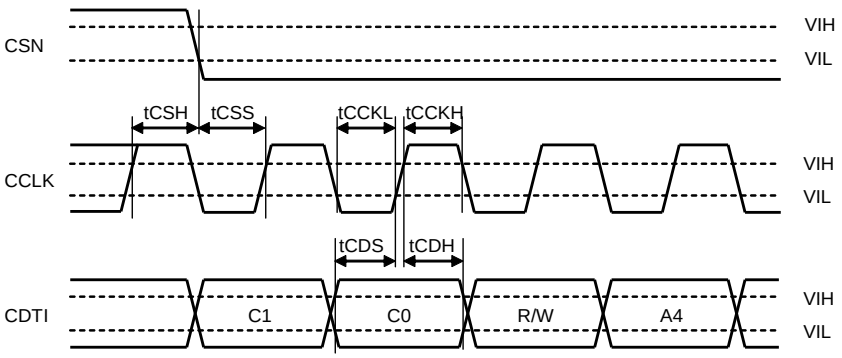


Figure 4. WRITE Command Input Timing

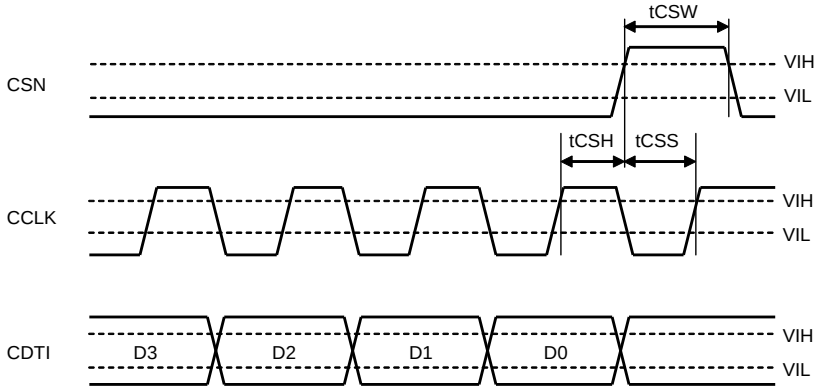


Figure 5. WRITE Data Input Timing

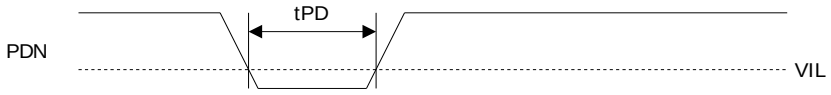


Figure 6. Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The AK4621 requires MCLK, BICK and LRCK external clocks. MCLK must be synchronized with LRCK but the phase is not critical. The AK4621 is automatically placed in power-down state when MCLK is stopped more than 9.38μs during a normal operation (PDN pin ="H"), then the digital output becomes "0" data and the analog output becomes Hi-Z. When MCLK and LRCK are input again, the AK4621 exit power-down state and starts the operation. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4621 is in power-down mode until MCLK is supplied.

As the AK4621 includes the phase detect circuit for LRCK, the AK4621 is reset automatically when the synchronization is out of phase by changing the clock frequencies.

1. Serial mode (P/S pin= "L")

As shown in Table 1, Table 2 and Table 3, select the MCLK frequency by setting CMODE, CKS1-0 and DFS1-0 bits. These registers are changed when RSTAD bit = RSTDA bit = "0".

DFS1 bit	DFS0 bit	Mode	Sampling Rate	
0	0	Normal speed	32kHz-54kHz	(default)
0	1	Double speed	54kHz-108kHz	
1	0	Quad speed	108kHz-216kHz	
1	1	N/A	-	

Table 1. Sampling Speed in Serial Mode (N/A: Not Available)

CMODE bit	CKS1 bit	CKS0 bit	MCLK Normal Speed (DFS1-0 = "00")	MCLK Double Speed (DFS1-0 = "01")	MCLK Quad Speed (DFS1-0 = "10")	
0	0	0	256fs	N/A	N/A	(default)
0	0	1	512fs	256fs	128fs	
0	1	0	1024fs	512fs	256fs	
0	1	1	N/A	Auto Setting Mode (*)	N/A	
1	0	0	384fs	N/A	N/A	
1	0	1	768fs	384fs	192fs	

Table 2. Master Clock frequency in Serial Mode ("*"; refer to Table 3.) (N/A: Not Available)

The Auto Setting Mode detects MCLK/LRCK ratio and selects Normal/Double/Quad speed mode automatically (Table 3).

MCLK/LRCK ratio	Mode	Sampling Rate
512 or 768	Normal speed	32kHz-54kHz
256 or 384	Double speed	54kHz-108kHz
128 or 192	Quad speed	108kHz-216kHz

Table 3. Auto Setting Mode in Serial Mode (DFS1-0 bits = "01", CMODE bit = "0", CKS1-0 bits = "11")

2. Parallel mode (P/S pin= “H”)

As shown in Table 4, Table 5 and Table 6, select the MCLK frequency with the CKS0-1 and DFS0 pins. These pins must be changed when the PDN pin = “L”.

DFS0 pin	Mode	Sampling Rate
L	Normal speed	32kHz-54kHz
H	Double speed	54kHz-108kHz

Table 4. Sampling Speed in Parallel Mode

CKS1 pin	CKS0 pin	MCLK Normal Speed (DFS0 pin = “L”)	MCLK Double Speed (DFS0 pin = “H”)
L	L	256fs	N/A
L	H	512fs	256fs
H	L	384fs	Auto Setting Mode (*)
H	H	1024fs	512fs

Table 5. Master Clock Frequency in Parallel Mode (“*”; refer to Table 6.) (N/A: Not Available)

The Auto Setting Mode detects MCLK/LRCK ratio and selects Normal/Double/Quad speed mode automatically. (Table 6).

MCLK/LRCK ratio	Mode	Sampling Rate
512 or 768	Normal speed	32kHz-54kHz
256 or 384	Double speed	54kHz-108kHz
128 or 192	Quad speed	108kHz-216kHz

Table 6. Auto Setting Mode in Parallel Mode (DFS0 pin = “H”, CKS1 pin = “H”, CKS0 pin = “L”)

MCLK (Normal speed)	fs=44.1kHz	fs=48kHz
256fs	11.2896MHz	12.288MHz
512fs	22.5792MHz	24.576MHz
1024fs	45.1584MHz	49.152MHz
384fs	16.9344MHz	18.432MHz
768fs	33.8688MHz	36.864MHz

MCLK (Double speed)	fs=88.2kHz	fs=96kHz
N/A	N/A	N/A
256fs	22.5792MHz	24.576MHz
512fs	45.1584MHz	49.152MHz
N/A	N/A	N/A
384fs	33.8688MHz	36.864MHz

MCLK (Quad speed)	fs=176.4kHz	fs=192kHz
128fs	22.5792MHz	24.576MHz
256fs	45.1584MHz	49.152MHz
192fs	33.8688MHz	36.864MHz

Table 7. Master Clock Frequency Example (N/A: Not Available)

■ Audio Serial Interface Format

Five serial modes are supported and selected by the DIF2-0 bits in Serial Mode (two modes by DIF pin in Parallel Mode) as shown in Table 8 and Table 9. In all modes the serial data has MSB first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. Mode2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTO	SDTI	LRCK	BICK	
0	0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 48fs	
1	0	0	1	24bit, MSB justified	20bit, LSB justified	H/L	≥ 48fs	
2	0	1	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	(default)
3	0	1	1	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs	
4	1	0	0	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 8. Audio Data Format (Serial Mode)

Mode	DIF pin	SDTO	SDTI	LRCK	BICK
2	L	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs
3	H	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs

Table 9. Audio Data Format (Parallel Mode)

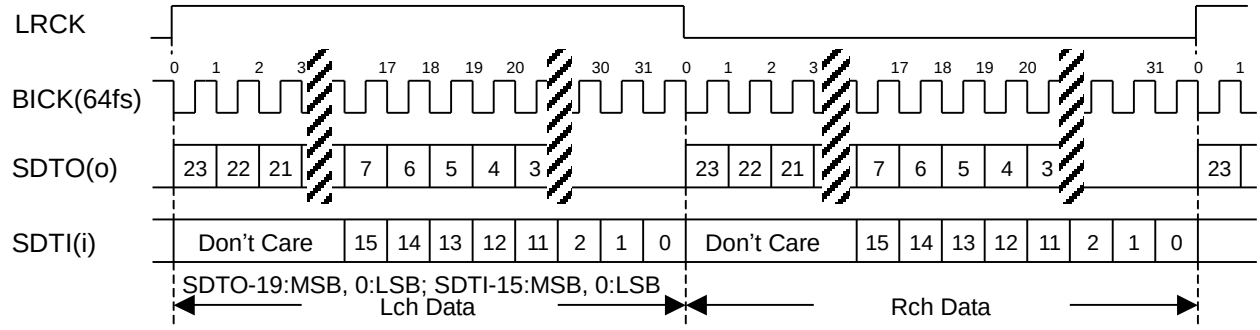


Figure 7. Mode 0 Timing

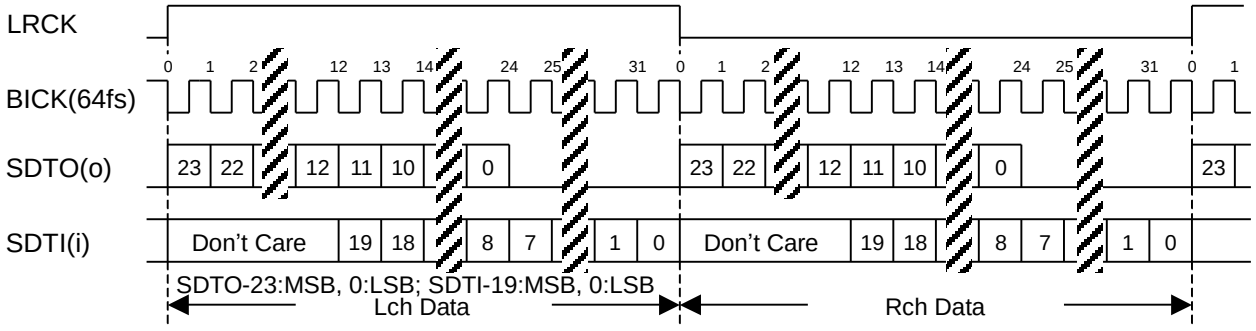


Figure 8. Mode 1 Timing

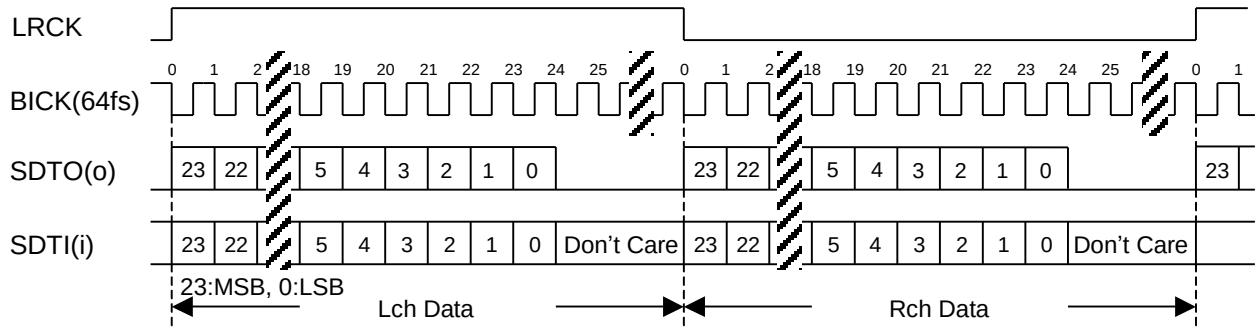


Figure 9. Mode 2 Timing

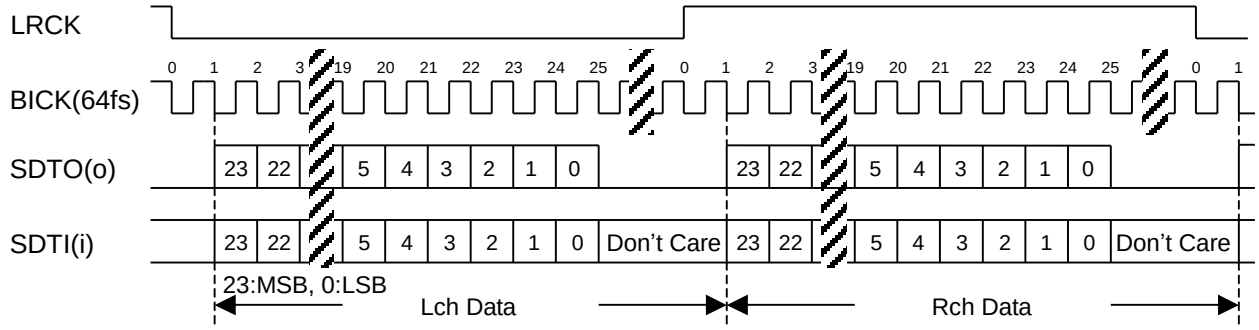


Figure 10. Mode 3 Timing

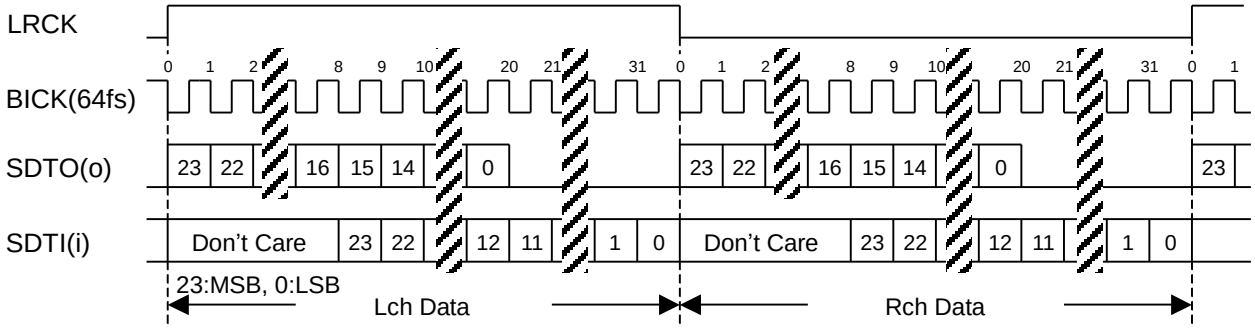


Figure 11. Mode 4 Timing

■ Output Volume

The AK4621 includes channel independent digital output volumes (DATT) with 256 levels and extension digital output volumes (EATT) with 16 levels at linear steps including MUTE. When EXTE bit = "1", the extension digital output volumes are enabled. These volumes are in front of the DAC. If the extension digital output volumes are disabled, the volumes can attenuate the input data from 0dB to −48dB and mute. If the extension digital output volumes are enabled, the volumes can attenuate the input data from 0dB to −72dB and mute. When changing levels, transitions are executed via soft changes, eliminating any switching noises. The transition time of 1 level, all 256 levels and all 256+16 is shown in Table 10. Volume calculating formula is shown in Table 13.

Sampling Speed	Transition Time		
	1 Level	255 to 0 (EXTE bit = "0")	255+15 to 0 (EXTE bit = "1")
Normal Speed Mode	4LRCK	1020LRCK	1080LRCK
Double Speed Mode	8LRCK	2040LRCK	2160LRCK
Quad Speed Mode	16LRCK	4080LRCK	4320LRCK

Table 10. Output Digital Volume Transition Time

DATTL7-0 bits DATTR7-0 bits	DATT_DATA	EATTL3-0 bits EATTR3-0 bits	GAIN(0dB)	
FFH	255	FH	+0	(default)
FEH	254		-0.034	
FDH	253		-0.068	
:	:		:	
02H	2		-42.11	
01H	1		-48.13	
00H	-		Mute	

Table 11. Output Digital Volume Setting (EXTE bit = "0")

DATTL7-0 bits DATTR7-0 bits	DATT_DATA	EATTL3-0 bits EATTR3-0 bits	EATT_DATA	GAIN(0dB)
FFH	255	FH	-	+0
FEH	254			-0.034
FDH	253			-0.068
:	:			:
02H	2			-42.11
01H	1			-48.13
00H	-	FH	15	-48.72
		EH	14	-49.32
		:	:	:
		2H	2	-66.22
		1H	1	-72.25
		0H	-	Mute

Note 24. If the volume is set from DATT gain to EATT gain or from EATT gain to DATT gain, these register must be wrote continuously within 4LRCK cycles in Normal Speed Mode. When the volume setting is not complete within 4LRCK cycles, the volume transition may stop.

Table 12. Output Digital Volume Setting (EXTE bit = "1")

DATTL7-0 bits DATTR7-0 bits	EATTL3-0 bits EATTR3-0 bits	GAIN(dB)
FFH : 01H	FH	$20 \log_{10}$ (DATT_DATA / 255)
00H	FH : 1H	$20 \log_{10}$ (EATT_DATA / 4095)

Table 13. Output Digital Volume Formula

■ Overflow Detection

The ADC has a channel independent overflow detection function. This function is enabled in parallel control mode, or when the ZOS bit = ZOE bit = "0" in serial control mode. OVFL/R pins go to "H" if each Lch/Rch analog input overflows (exceeds -0.3dBFS). The output of each OVFL/R pin has same group delay as ADC against analog inputs. OVFL/R pin is "L" for 516/fs (=10.8ms @fs=48kHz) after the PDN pin = "↑", and then overflow detection is enabled.

■ Zero Detection

The DAC has a channel-independent zero detect function. The zero detect function is enabled when the ZOS bit = "1" and the ZOE bit = "0" in serial control mode. When the input data at both channels is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately returns to "L" if the input data of each channel is not zero after DZF "H". If the RSTDA bit is "0", the DZF pins of both channels go to "H". The DZF pins of both channels return to "L" in 2~3fs if the input data of each channel is not zero. Zero detect function can be disabled by the ZOE bit. In this case, the DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz. The digital high pass filter cut-off frequency scales with the sampling rate (fs). In parallel mode, the HPF is always enabled. In serial mode, the HPF can control each channel by HPLN/HPRN bits.

■ Digital Filter

The AK4621 has two kinds of Digital Filter for ADC and three kinds of Digital Filter for DAC. The outputs of ADC and DAC can be controlled by using the SDFIL pin or SDAD/SDDA/SLOW bits.

SDFIL pin	ADC	DAC
L	Short Delay Sharp Roll Off Filter	Short Delay Sharp Roll Off Filter
H	Sharp Roll Off Filter	Sharp Roll Off Filter

Table 14. Digital Filter Selection in Parallel Mode

SDAD bit	ADC	
0	Sharp Roll Off Filter	(default)
1	Short Delay Sharp Roll Off Filter	

Table 15. ADC Digital Filter Selection in Serial Mode

SDDA bit	SLOW bit	DAC	
0	0	Sharp Roll Off Filter	(default)
0	1	Slow Roll Off Filter	
1	0	Short Delay Sharp Roll Off Filter	
1	1	N/A	

Table 16. DAC Digital Filter Selection in Serial Mode (N/A: Not Available)

■ De-emphasis Filter

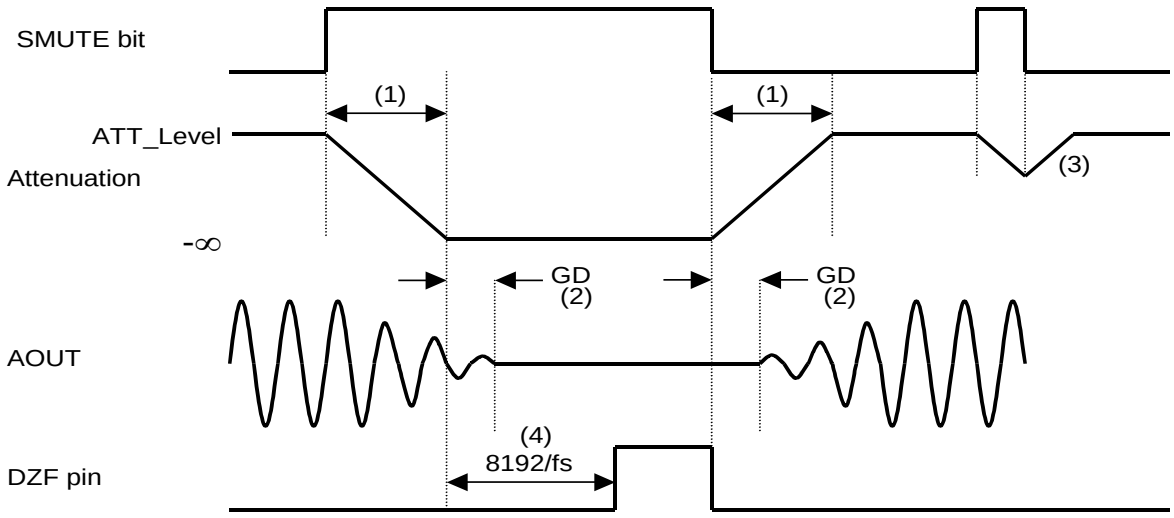
The DAC includes a digital de-emphasis filter (tc=50/15μs for 32kHz, 44.1kHz or 48kHz sampling rates) by an integrated IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter. This filter is always OFF in double and quad speed modes. The DEM0 pin and DEM0 bit are OR'd in serial control mode. In parallel control mode, the DEM1 bit is fixed to "0" and only the DEM0 pin can be controlled (44.1kHz or OFF).

No	DEM1	DEM0	Mode	
0	0	0	44.1kHz	
1	0	1	OFF	(default)
2	1	0	48kHz	
3	1	1	32kHz	

Table 17. De-emphasis control (Normal Speed Mode)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the DAC input. When the SMUTE bit goes to "1", the output signal is attenuated by −∞ during ATT_DATA × ATT transition time (Table 10) from the current ATT level. When SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and returns to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time (Table 10). For example, in Normal Speed Mode, if the EATT is disabled, this time is 1020LRCK cycles (1020/fs). If the EATT is enabled, this time is 1080LRCK cycles (1080/fs).

(2) Analog output corresponding to digital input has group delay (GD).

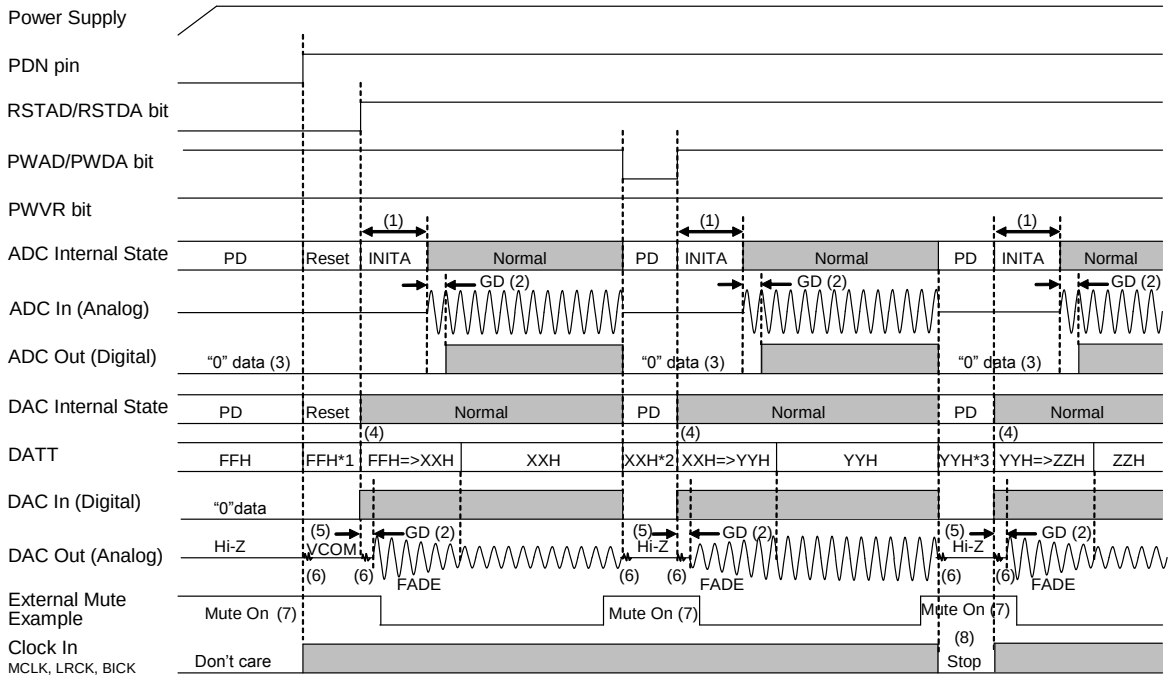
(3) If the soft mute is cancelled before attenuating −∞, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at each channel is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin immediately returns to "L" if input data are not zero after going to "H".

Figure 12. Soft Mute and Zero Detection

■ Power Down & Reset

The ADC and DAC of AK4621 are placed in power-down mode by bringing the PDN pin = "L". Each digital filter is also reset at the same time. The internal register values are initialized by bringing the PDN pin to "L". This reset must always be done after power-up. As both control registers of the ADC and the DAC go to the reset state (RSTAD bit = RSTDA bit = "0"), each register must be cleared after executing the reset. In the case of the ADC, an analog initialization cycle starts after exiting the power-down or reset state. The output data (SDTO) is available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Power down mode can be also controlled by the registers (PWAD bit, PWDA bit).



Notes:

(1) After exiting power down and reset state, the analog part of ADC is initialized (516/fs).

(2) Digital output corresponding to analog input and analog input corresponding to digital input have group delay (GD).

(3) ADC output is "0" data in power-down state.

(4) After exiting power down and reset state, ATT value fades in/out.

*1 When RSTDA is "L" and DATT value is written to "XXH", DATT value changes from FFH to XXH according to fade operation.

*2 When PWDA is "L" and DATT value is written to "YYH", DATT value changes from XXH to YYH according to fade operation.

*3 When the external clocks (MCLK, SCLK, LRCK) are stopped and DATT value is written to "ZZH", DATT value changes from YYH to ZZH according to fade operation.

(5) In the power-down mode, the DAC output is VCOM level. In the reset state, the DAC output is floating (Hi-z).

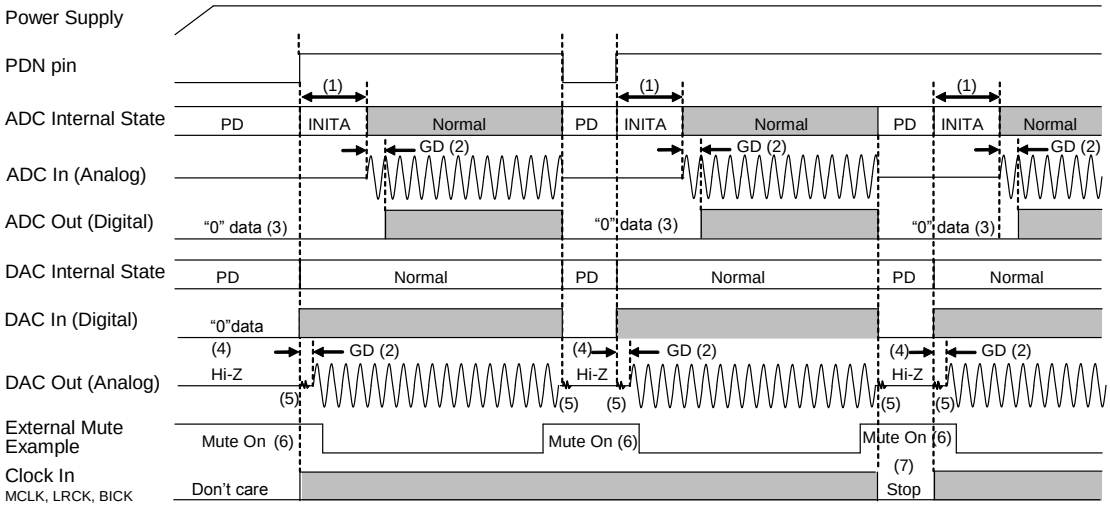
(6) Click noise occurs after RSTDA bit or PWDA bit is changed.

(7) Mute the analog output externally if the click noise (6) influences system application.

(8) When MCLK is stopped more than 9.38μs, the AK4621 becomes power down mode. Then ADC output is "0" data and DAC output is floating (Hi-Z).

Figure 13. Reset & Power down sequence in serial mode

In parallel mode, both ADC and DAC are powered up when releasing internal reset state by the PDN pin = "H". When the PDN pin is "L", after exiting power down mode ADC s output "0" during first 516/fs cycles. DAC does not have the initialization cycle and the operation of fade-in.



Notes:

(1) After exiting power down and reset state, the analog part of ADC is initialized (516/fs).
(2) Digital output corresponding to analog input and analog input corresponding to digital input have group delay (GD).
(3) ADC output is "0" data in power-down state.
(4) DAC output is floating (Hi-z) in power-down state.
(5) Click noise occurs at the rising/falling edge of PDN.
(6) Mute the analog output externally if the click noise (5) influences system application.
(7) When MCLK is stopped more than 9.38μs, the AK4621 becomes power down mode. Then ADC output is "0" data and DAC output is floating (Hi-Z).

Figure 14. Reset & Power Down Sequence in parallel mode

■ Serial Control Interface

The internal registers may be written by the 3-wire μP interface pins: CSN, CCLK, CDTI. The data on this interface consists of Chip address (2bits, C0/1) Read/Write (1 bit), Register address (MSB first, 5 bits) and Control data (MSB first, 8 bits). Address and data are clocked in on the rising edge of CCLK and data is latched after the 16th rising edge of CCLK, following a high-to-low transition of CSN. Operation of the control serial port may be completely asynchronous with the audio sample rate. The maximum clock speed of the CCLK is 5MHz. The chip address is fixed to "10". The access to the chip address except for "10" is invalid. PDN pin = "L" resets the registers to their default values.

Function	Parallel mode	Serial mode
Overflow detection	X	X
DAC Slow Roll Off Filter	-	X
Zero detection	-	X
Soft Mute	-	X
DATT	-	X
HPF OFF	-	X
16/20/24 bit LSB justified format of DAC	-	X
MCLK = 256fs @ Quad Speed	-	X
De-emphasis: 32kHz, 48kHz	-	X

Table 18. Function List (X: available, -: not available)

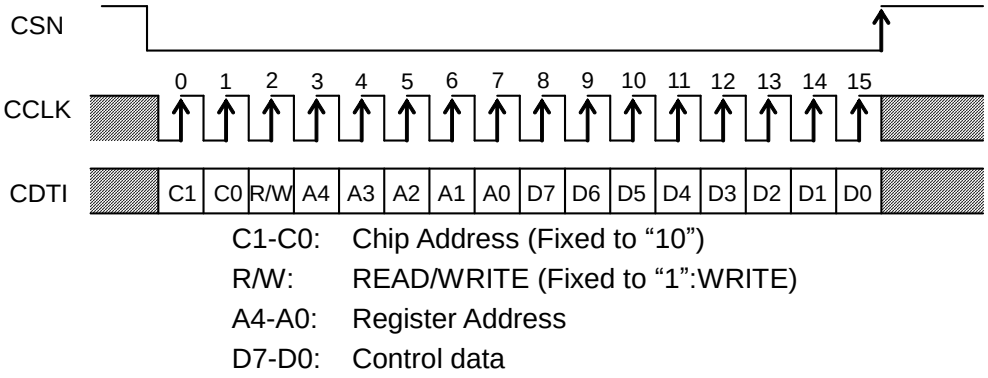


Figure 15. Control I/F Timing

* READ command is not supported.
* The control data can not be written when the CCLK rising edge is 15times or less or 17times or more during CSN is "L".

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	SLOW	DZFB	ZOE	ZOS	SDDA	PWVR	PWAD	PWDA
01H	Reset Control	0	0	0	SDAD	0	0	RSTAD	RSTDA
02H	Clock and Format Control	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0
03H	Deem and Volume Control	SMUTE	HPRN	HPLN	0	0	0	DEM1	DEM0
04H	Reserved	0	0	0	0	0	0	0	0
05H	Reserved	0	0	0	0	0	0	0	0
06H	Lch DATT Control	DATTL7	DATTL6	DATTL5	DATTL4	DATTL3	DATTL2	DATTL1	DATTL0
07H	Rch DATT Control	DATTR7	DATTR6	DATTR5	DATTR4	DATTR3	DATTR2	DATTR1	DATTR0
08H	Lch Extension DATT Control	0	0	EXTE	0	EATTL3	EATTL2	EATTL1	EATTL0
09H	Rch Extension DATT Control	0	0	0	0	EATTR3	EATTR2	EATTR1	EATTR0

Note 25: Data must not be written to addresses 0AH through 1FH.

PDN pin = “L” resets the registers to their default values.

■ Control Register Setup Sequence

When the PDN pin goes “L” to “H” upon power-up etc., the AK4621 will be ready for normal operation by the sequence below. In this case, all control registers are set to default values and the AK4621 is in the reset state.

(1) Set the clock mode and the audio data interface mode.
(2) Cancel the reset state by setting RSTAD bit or RSTDA bit to “1”. Refer to Reset Contorl Register (01H).
(3) ADC output and DAC output must be muted externally until canceling each reset state.

The clock mode must be changed after setting RSTAD bit and RSTDA bit to “0”. At that time, ADC outputs and DAC outputs must be muted externally.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	SLOW	DZFB	ZOE	ZOS	SDDA	PWVR	PWAD	PWDA
Default		0	0	0	0	0	1	1	1

PWDA: DAC power down
0: Power down
1: Power up (default)
When PWDA bit = "0", only the DAC block is powered down and the AOUT becomes Hi-z immediately. In this time, all registers are not initialized, and register writings are valid. After exiting power down mode, the OATT fades in/out the setting value of the control register (06H, 07H, 08H, 09H). The analog output must be muted externally as a pop noise may occur when entering and exiting this mode.

PWAD: ADC power down
0: Power down
1: Power up (default)
When PWAD bit = "0", only the ADC block is powered-down and the SDTO pin becomes "L" immediately. After exiting power down mode, the ADC outputs "0" during first 516 LRCK cycles.

PWVR: Vref power down
0: Power down
1: Power up (default)
When PWVR bit = "0", all blocks are powered down. Both ADC and DAC cannot operate. In this time, all registers are not initialized, and register writings are valid. Only the VRFE block can be powered up by setting PWAD = PWDA bit = "0" and PWVR bit = "1".

SDDA: DAC Short Delay Sharp Roll Off Filter Enable (Table 16)
Default: Disable

ZOS: Zero-detection/ Overflow-detection control for OVFL/DZFL and OVFR/DZFR pins.
0: Overflow detection for ADC input (default)
1: Zero detection for DAC input.

ZOE: Zero-detection / Overflow-detection Disable
0: Enable (default)
1: Disable. Outputs "L".

DZFB: Inverting Enable of DZF
0: DZF goes "H" at Zero Detection (default)
1: DZF goes "L" at Zero Detection

SLOW: DAC Slow Roll Off Filter Enable (Table 16)
Default: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Reset Control	0	0	0	SDAD	0	0	RSTAD	RSTDA
Default		0	0	0	0	0	0	0	0

RSTDA: DAC reset
0: Reset (default)
1: Normal Operation
When RSTDA bit ="0", the internal timing of DAC is reset and the AOUT becomes VCOM voltage immediately. In this time, all registers are not initialized, and register writings are valid. After exiting the power down mode, the OATT fades in the setting values of the control register (06H, 07H, 08H, 09H). The analog outputs must be muted externally since a pop noise may occur when entering to and exiting from this mode.

RSTAD: ADC reset
0: Reset (default)
1: Normal Operation
When RSTAD bit ="0", the internal timing of ADC is reset and the SDTO pin becomes "L" immediately. In this time, all registers are not initialized, and register writings are valid. After exiting the power down mode, the ADCs output "0" during first 516 LRCK cycles.

SDAD: ADC Short Delay Sharp Roll Off Filter Enable (Table 15)
Default: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock and Format Control	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0
Default		0	1	0	0	0	0	0	0

DFS1-0: Sampling Speed Control (Table 1)
Default: Normal speed

CMODE, CKS1-0: Master Clock Frequency Select (Table 2)
Default: 256fs

DIF2-0: Audio data interface modes (Table 8)
000: Mode 0
001: Mode 1
010: Mode 2 (default)
011: Mode 3
100: Mode 4
Default: 24bit MSB justified for both ADC and DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Deem and Volume Control	SMUTE	HPRN	HPLN	0	0	0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis response (Table 17)
- 00: 44.1kHz
- 01: OFF (default)
- 10: 48kHz
- 11: 32kHz

HPLN/RN: Left/Right channel Digital High Pass Filter Disable
- 0: Enable (default)
- 1: Disable

SMUTE: DAC Input Soft Mute control
- 0: Normal operation (default)
- 1: DAC outputs soft-muted
  The soft mute is independent of the output ATT and performed digitally.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Lch DATT Control	DATTL7	DATTL6	DATTL5	DATTL4	DATTL3	DATTL2	DATTL1	DATTL0
07H	Rch DATT Control	DATTR7	DATTR6	DATTR5	DATTR4	DATTR3	DATTR2	DATTR1	DATTR0
Default		1	1	1	1	1	1	1	1

DATT7-0: DAC Output Attenuation Level, Linear step. (Table 12, Table 13)
Default: 00H (0dB)

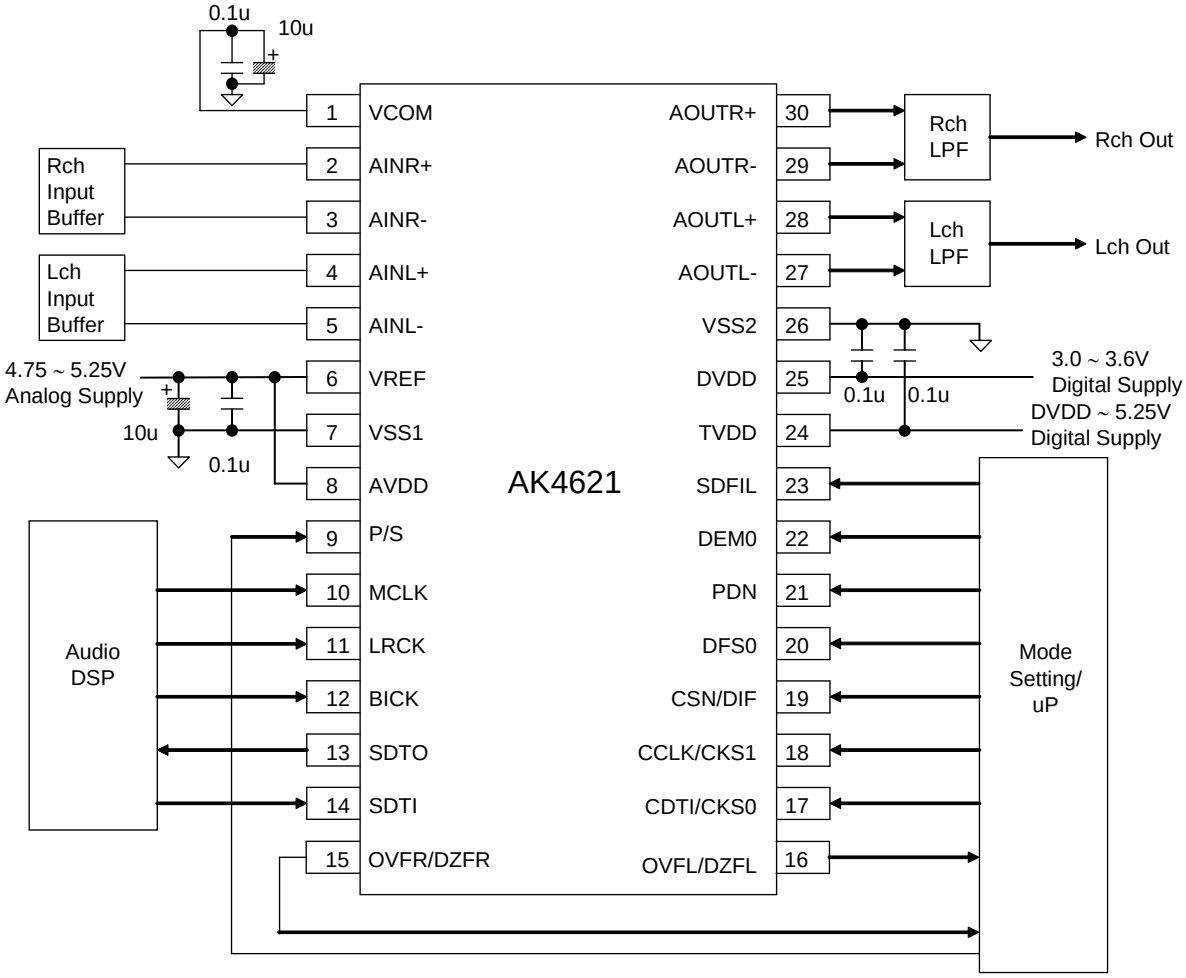
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lch Extension DATT Control	0	0	EXTE	0	EATTL3	EATTL2	EATTL1	EATTL0
09H	Rch Extension DATT Control	0	0	0	0	EATTR3	EATTR2	EATTR1	EATTR0
Default		0	0	0	0	1	1	1	1

EATT3-0: DAC Output Extension Attenuation Level; Linear step. (Table 12, Table 13)
Default: FH

EXTE: Extension DATT Enable
- 0: Disable (default)
- 1: Enable

SYSTEM DESIGN

Figure 16 shows the system connection diagram. An evaluation board (AKD4621) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1 and VSS2 must be connected to the same analog ground plane.
- When AOUT+/- drives some capacitive load, some resistance must be added in series between AOUT+/- and capacitive load.
- All digital input pins must not be left floating.

Figure 16. Typical Connection Diagram

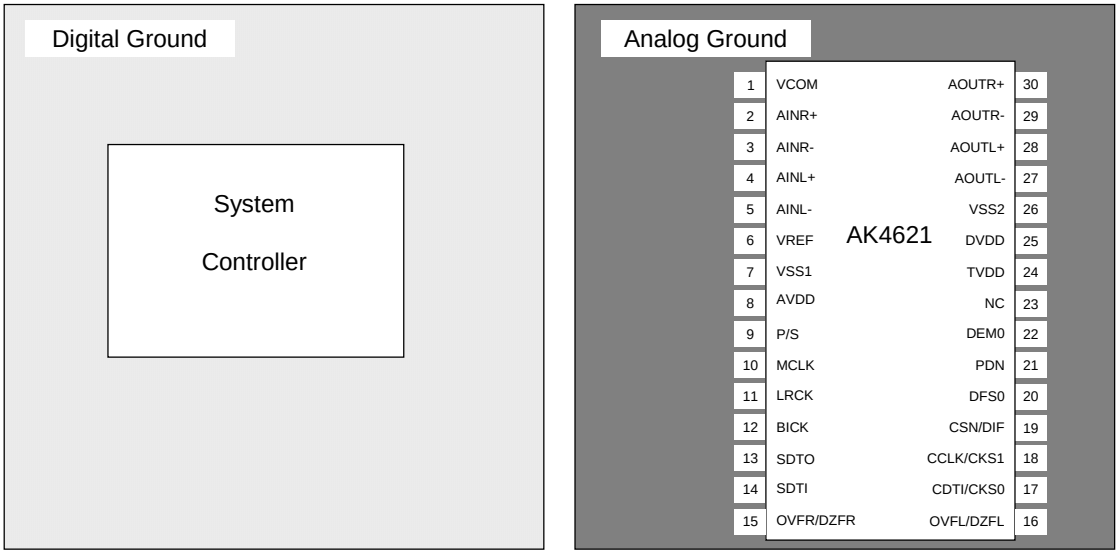


Figure 17. Ground Layout

1. Ground and Power Supply Decoupling

The AK4621 requires careful attention to power supply and grounding layout. To minimize coupling from digital noise, decoupling capacitors must be connected to AVDD, DVDD and TVDD respectively. AVDD is supplied from the analog supply in the system, and DVDD and TVDD are supplied from the digital supply in the system. Power lines of AVDD, DVDD and TVDD must be distributed separately from the point with low impedance of regulator etc. The power up sequence is not critical among AVDD, DVDD and TVDD. **VSS1 and VSS2 must be connected to one analog ground plane.** Decoupling capacitors must be as near to the AK4621 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The differential voltage between VREF and VSS1 sets the analog input/output range. The VREF pin is normally connected to AVDD with a 0.1μF ceramic capacitor. VCOM is the signal ground of this chip. A 10μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, must be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4621.

3. ADC Output

The ADC output data format is 2's complement. The DC offset, including the ADC's own DC offset, is removed by the internal HPF (fc=1.0Hz@fs=48kHz). The AK4621 samples the analog inputs at 128fs (@Normal Speed Mode), 64fs (@Double Speed Mode) or 32fs (@Quad Speed Mode). The digital filter rejects noise above the stopband except for multiples of 128fs (@Normal Speed Mode), 64fs (@Double Speed Mode) or 32fs (@Quad Speed Mode).

4. Analog Inputs

The AK4621 can accept input voltages from VSS1 to AVDD. The input signal range scales with the VREF voltage and is nominally 2.82Vpp (VREF = 5V), centered around the internal common voltage (about VA/2). Figure 18 shows an input buffer circuit example. This is a fully differential input buffer circuit with an inverted amplifier (gain: –10dB). The capacitor of 10nF between AINL+/– (AINR+/–) decreases the clock feedthrough noise of the modulator, and it composes a 1st order LPF (fc=360kHz) with a 22Ω resistor before the capacitor. This circuit also has a 1st order LPF (fc=370kHz) composed of op-amp. Refer to an evaluation board for details.

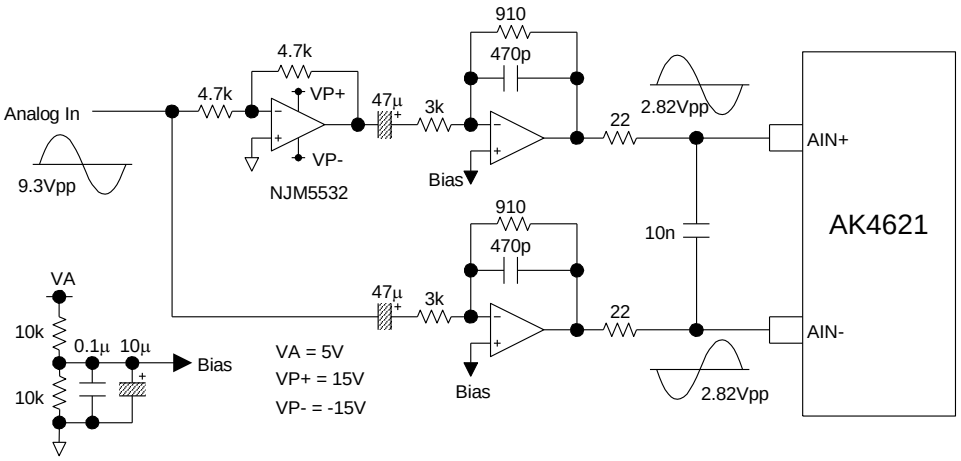


Figure 18. Input Buffer Example

5. Analog Outputs

The analog outputs are fully differential and 2.8Vpp (typ. VREF = 5V), centered around VCOM. The differential outputs are summed externally: Vout = (AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.6Vpp (typ. VREF = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal AOUT is 0V for 000000H(@24bit).

The internal switched-capacitor filter and the external LPF attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 19 shows an example of external LPF circuit summing the differential outputs by an op-amp. Figure 20 shows an example of differential outputs and LPF circuit example by three op-amps.

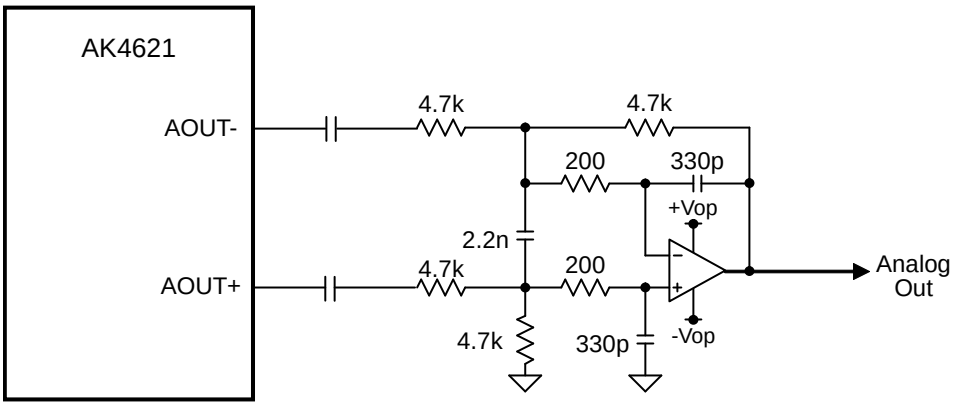


Figure 19. External LPF Circuit Example 1 (fc = 136kHz, Q=0.694)

Frequency Response	Gain
20kHz	–0.01dB
40kHz	–0.06dB
80kHz	–0.59dB

Table 19. Frequency Response of External LPF Circuit Example 1

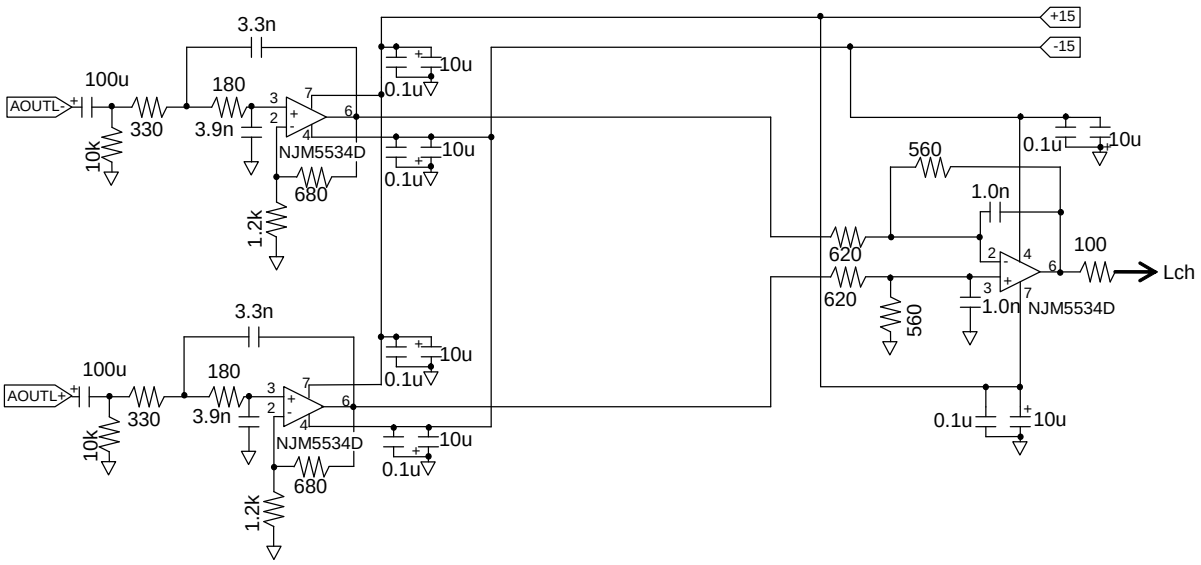


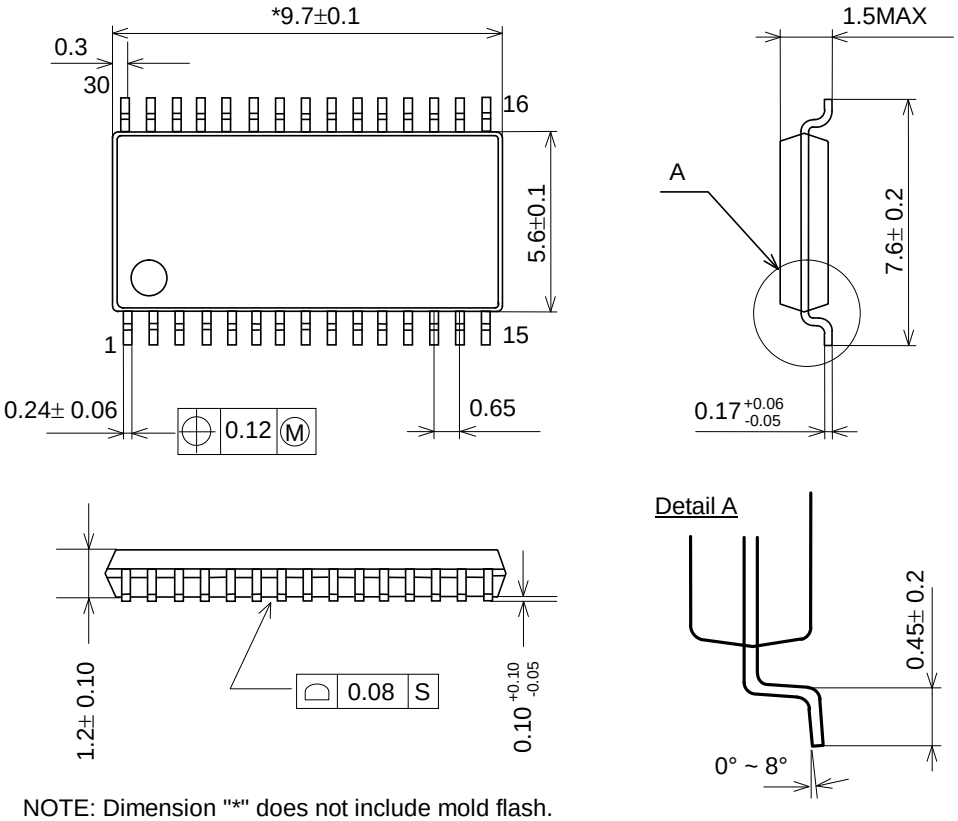
Figure 20. External LPF Circuit Example 2

		1st Stage	2nd Stage	Total
Cut-off Frequency		182kHz	284kHz	-
Q		0.637	-	-
Gain		+3.9dB	-0.88dB	+3.02dB
Frequency Response	20kHz	-0.025	-0.021	-0.046dB
	40kHz	-0.106	-0.085	-0.191dB
	80kHz	-0.517	-0.331	-0.848dB

Table 20. Frequency Response of External LPF Circuit Example 2

PACKAGE

30pin VSOP (Unit: mm)

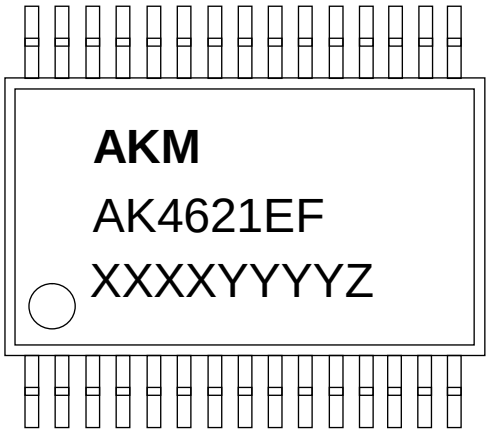


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound: Epoxy Resin, Halogen (bromine and chlorine) free
Lead frame material: Cu Alloy
Lead frame surface treatment: Solder (Pb free) plate

MARKING



YYYY: Date code
XXXX, Z: Internal control code

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page/Line	Contents
10/12/07	00	First Edition		
11/01/26	01	Description Change		Digital filter names were changed.
17/09/06	02	Specification Change	5	"filtered" were removed from the function explanation of the VREF pin.
			6	A comment was added to Note 6 as follows. "VREF is connected externally to AVDD."
			6	The Recommended Operating Condition for the Voltage Reference was changed.