AKD4621-B
AK4621 Evaluation board Rev.2

GENERAL DESCRIPTION

The AKD4621-B is an evaluation board for the AK4621, the 24Bit A/D & D/A converter. The AKD4621-B can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D→D/A). The AKD4621-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4621-B --- Evaluation board for AK4621
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

☐ Digital interface
- **DIT (AK4114): optical or BNC**
- **DIR (AK4114): optical or BNC**

☐ 10pin header for serial control interface

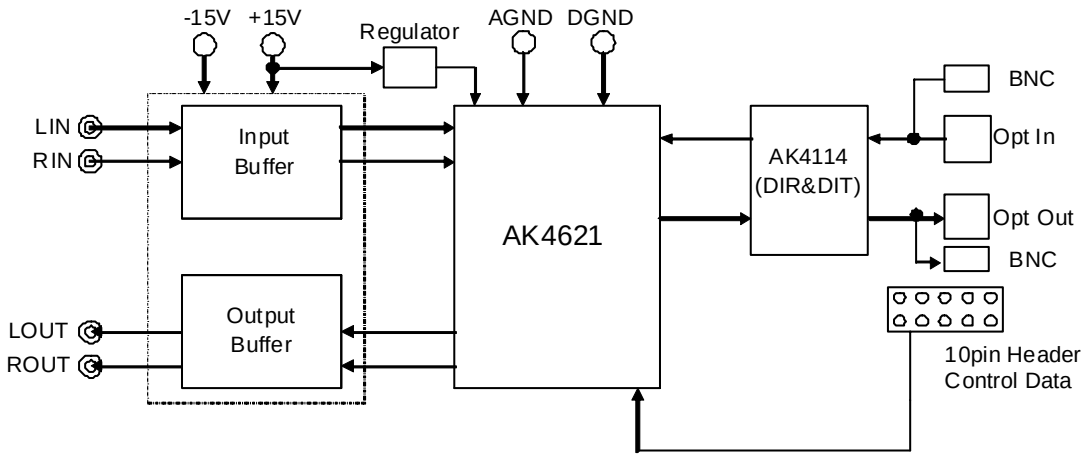


Figure 1. AKD4621-B Block Diagram

* Circuit diagram are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up of the power supply lines

Each of the power supply lines should be distributed from the power supply units.

Name of jack	Color of jack	Typ Voltage	Using	Default setting
+15V	Green	+15V	Power supply for the plus terminal of OPAmp Power supply for the regulator: T1: +15V→+5V (Power supply for AVDD and VREF of AK4621, power supply for Bias of OPAmp, and power supply for the Regulator: T2: +5V→+3.3V (Power supply for DVDD and TVDD of AK4621)) Power supply for the regulator: T3: +15V→+3.3V (Power supply for AVDD, DVDD, TVDD of AK4114, Power supply for logic)	Connect to +15V (Must be connected)
-15V	Blue	-15V	Power supply for the minus terminal of OPAmp	Connect to -15V (Must be connected)
GND	Black	0V	Analog ground Digital ground	Connect to GND (Must be connected)

Table 1. Set up of the power supply lines

2) Set up the evaluation modes, jumper pins and DIP switch. (See the followings.)

3) Power on

The AK4621 should be reset once bringing SW2 (PDN) “L” upon power-up.

■ Evaluation modes

Applicable evaluation modes

(1) Evaluation of A/D-D/A Loop back (Default)
(2) Evaluation of DAC
(3) Evaluation of ADC

1) Evaluation of A/D-D/A Loop back (Default)

1-1) Sampling speed & MCLK frequency

a) Parallel mode (Default)

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621	
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs	(Default)
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs	

Table 2. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) Serial mode

SW1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621
OFF	0	0	0	0	1	ON	OFF	Normal Speed	512fs
OFF	0	1	0	0	1	OFF	OFF	Double Speed	256fs
OFF	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 3. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4 (DFS0), SW1-6 (CKS1) and SW1-7 (CSK0) should be always “OFF”, and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4621 should be set via the printer port (PORT3).

1-2) AK4114's master clock mode & reference X'tal frequency

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO	
1	OFF	ON	OFF	ON	X'tal	DAUX	(Default)

Table 4. AK4114'S Clock Operation Mode

SW3-1 (XTL1)	SW3-2 (XTL0)	X'tal Frequency	
ON	OFF	24.576MHz	(Default)

Table 5. Reference X'tal frequency

1-3) Set up the digital filter

a) Parallel mode (Default)

SW1-2 (SDFIL)	Digital Filter	
OFF	Short Delay	
ON	Sharp Roll-off	(Default)

Table 6. Digital Filter Selection in parallel mode

b) Serial mode

SW1-2 (SDFIL)	SDAD bit	Digital Filter
OFF	0	Sharp Roll-off
OFF	1	Short Delay

Table 7. Digital Filter Selection in serial mode

2) Evaluation of D/A using DIR. (Optical link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1). PORT1 is also used for the evaluation using such as CD test disk.

BNC connector is recommended for an evaluation of the Sound quality.

2-1) DIR input interface (Default: JP2 (RX3)="OPT")

Jumper	JP2 (RX3)
Normal Speed & Double Speed	OPT (Default) or BNC
Quad Speed	BNC

Table 8. DIR Input Interface

2-2) Sampling speed & MCLK frequency

a) Parallel mode (Default)

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621	
ON	OFF	OFF	OFF	OFF	OFF	Normal Speed	256fs	
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs	(Default)
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs	

Table 9. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) Serial mode

SW1-1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621
OFF	0	0	0	0	0	OFF	OFF	Normal Speed	256fs
OFF	0	0	0	0	1	ON	OFF	Normal Speed	512fs
OFF	0	1	0	0	1	OFF	OFF	Double Speed	256fs
OFF	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 10. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4 (DFS0), SW1-6 (CKS1) and SW1-7 (CSK0) should be always “OFF”, and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4621 should be set via the printer port (PORT3).

2-3) AK4114's master clock mode & reference X'tal frequency

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO
0	OFF	OFF	ON	OFF	PLL	RX

Table 11. Clock Operation Mode

SW3-1 (XTL1)	SW3-2 (XTL0)	X'tal Frequency
ON	ON	OFF

Table 12. Reference X'tal frequency

2-4) Set up the digital filter

a) Parallel mode (Default)

SW1-2 (SDFIL)	Digital Filter
OFF	Minimum Delay
ON	Sharp Roll-off

Table 13. Digital Filter Selection in parallel mode

b) Serial mode

Set up the register of the AK4621 via the pint port (PORT3).

SW1-2 (SDFIL)	SDAD bit	SLOW bit	Digital Filter
OFF	0	0	Sharp Roll-off
OFF	0	1	Slow Roll-off
OFF	1	0	Minimum Delay

Table 14. Digital Filter Selection in serial mode

3) Evaluation of A/D using DIT. (Optical link)

DIT generates audio bi-phase signal from received data and which is output through optical connector (PORT2). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input.

3-1) DIT output interface (Default: JP7 (TX) ="OPT")

Jumper	JP7 (TX)
Normal Speed & Double Speed	OPT (Default) or BNC
Quad Speed	BNC

Table 15. DIT Output Interface

3-2) Sampling speed & MCLK frequency

a) Parallel mode (Default)

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621	
ON	OFF	OFF	OFF	OFF	OFF	Normal Speed	256fs	
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs	(Default)
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs	

Table 16. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) Serial mode

SW1-1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4621	MCLK Frequency of AK4621
OFF	0	0	0	0	0	OFF	OFF	Normal Speed	256fs
OFF	0	0	0	0	1	ON	OFF	Normal Speed	512fs
OFF	0	1	0	0	1	OFF	OFF	Double Speed	256fs
OFF	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 17. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4 (DFS0), SW1-6 (CKS1) and S1-7 (CSK0) should be always “OFF”, and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4621 should be set via the printer port (PORT3).

3-3) AK4114’s master clock mode & reference X’tal frequency

3-3-1) PLL is used as clock source

Synchronized signal should be set via PORT1 (optical) or J6 (BNC).

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO
0	OFF	OFF	ON	OFF	PLL	RX

Table 18. Clock Operation Mode (PLL)

SW3-1 (XTL1)	SW3-2 (XTL0)	X’tal Frequency
ON	ON	OFF

Table 19. Reference X’tal frequency (PLL)

3-3-2) X’tal is used as clock source (Default)

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO	
1	OFF	ON	OFF	ON	X’tal	DAUX	(Default)

Table 20. Clock Operation Mode (X’tal)

SW3-1 (XTL1)	SW3-2 (XTL0)	X’tal Frequency	
ON	OFF	24.576MHz	(Default)

Table 21. Reference X’tal frequency (X’tal)

3-4) Set up the digital filter

a) Parallel mode (Default)

SW1-2 (SDFIL)	Digital Filter
OFF	Short Delay
ON	Sharp Roll-off

(Default)

Table 22. Digital Filter Selection in parallel mode

b) Serial mode

SW1-2 (SDFIL)	SDAD bit	Digital Filter
OFF	0	Sharp Roll-off
OFF	1	Short Delay

Table 23. Digital Filter Selection in serial mode

■ Set up of DIP Switch: SW1, SW3

1) Set-up of SW1 (Mode set-up of AK4621)

1-1) Audio data format in parallel mode

Mode	DIF (SW1-5)	SDTO	SDTI	LRCK	BICK	
2	OFF	24bit MSB Justified	24bit MSB Justified	H/L	≥48fs	(Default)
3	ON	I^2S Compatible	I^2S Compatible	L/H	≥48fs	

Table 24. Audio data format (Parallel mode)

1-2) De-emphasis control in parallel mode

DEM0 pin (SW1-3)	MODE	
OFF	ON (44.1KHz)	
ON	OFF	(Default)

Table 25. De-emphasis control (Parallel mode)

1-3) Parallel mode/ serial mode

P/S pin (SW1-1)	MODE	
OFF	Serial	
ON	Parallel	(Default)

Table 26. Set up P/S pin

2) Set-up of SW3 (AK4114's mode set-up)

2-1) Audio data format

Mode	DIF0 (SW3-3)	SDTO	SDTI	LRCK	BICK	
4	OFF	24bit MSB Justified	24bit MSB Justified	H/L	≥48fs	(Default)
5	ON	I^2S Compatible	I^2S Compatible	L/H	≥48fs	

Table 27. Audio data format

* DIF1=L and DIF2=H are fixed in AKD4621-B evaluation board.

■ Other Jumper pin set up

JP3, JP4, JP5, JP6: Input mode selection of A/D converter.
DIFF: Analog differential input mode. <Default>
SINGLE: Analog single-end mode can not be selected on this board.

JP2, JP7: The interface selection of digital input and output.
OPT: Select the optical connector.
BNC: Select the BNC connector. <Default>

■ Toggle Switch: SW2

[SW2]: Resets the AK4621 and the AK4114. Keep "H" during normal operation.
However, "L" must be input once after power supply is done.

■ Serial control mode

The AK4621 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CR-I/F) with PC by 10-wire flat cable packed with the AKD4621-B.

Take care of the direction of connector. There is a mark at pin#1.

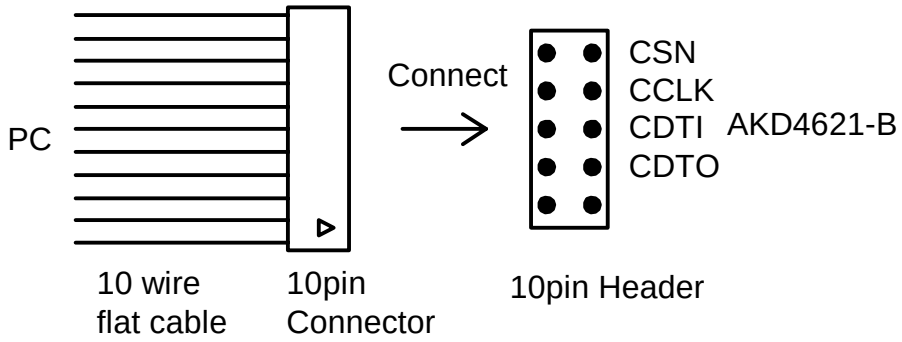


Figure 2. Connect of 10 wire flat cable

■ Analog Input Buffer Circuit

The AK4621 can accept input voltages from AGND to AVDD. The input signal range scales with the VREF voltage and is nominally 2.82Vpp (VREF = 5V). Figure 3 shows an input buffer circuit example. This is a fully differential input buffer circuit with an inverted amplifier (fc=370KHz,gain: −10dB).
The capacitor of 10nF between AINL+/− (AINR+/−) decreases the clock feed through noise of the modulator, and composes a 1st order LPF (fc=360kHz) with a 22Ω resistor before the capacitor.

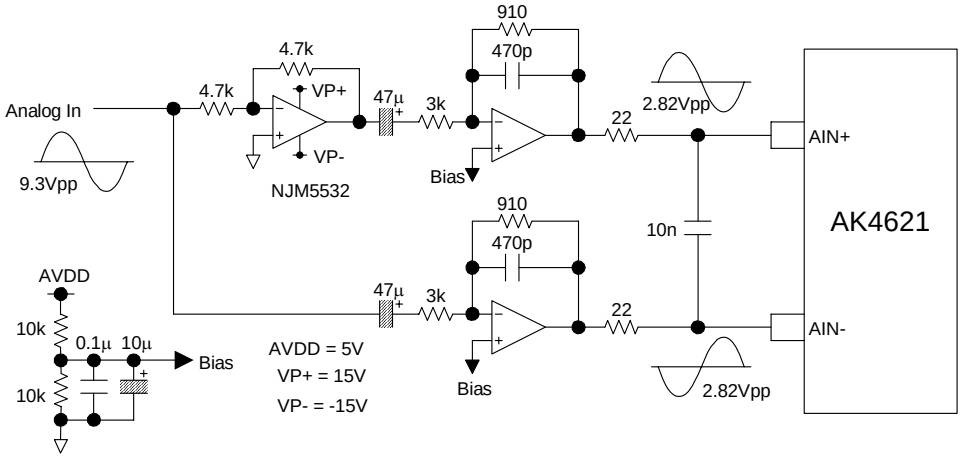


Figure 3. Input buffer circuit in differential input mode

■ Analog Output Buffer Circuit

The differential output circuit (2nd order LPF,fc=182KHz,Q=0.637,G=+3.9dB) and LPF(1st order LPF, fc=284KHz, G=-0.84dB) is implemented on board. The differential outputs of AK4621 is buffered by non-inverted circuit and output via Cannon connector (differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via BNC connectors on the board. The output level is about 2.8Vrms (typ@VREF=5.0V) by BNC.

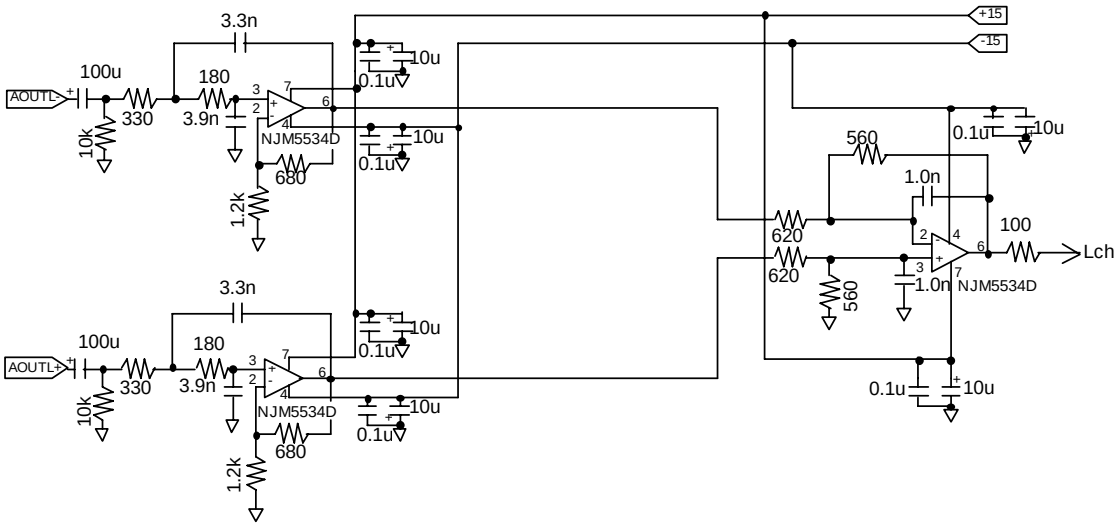


Figure 4. Output buffer circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.

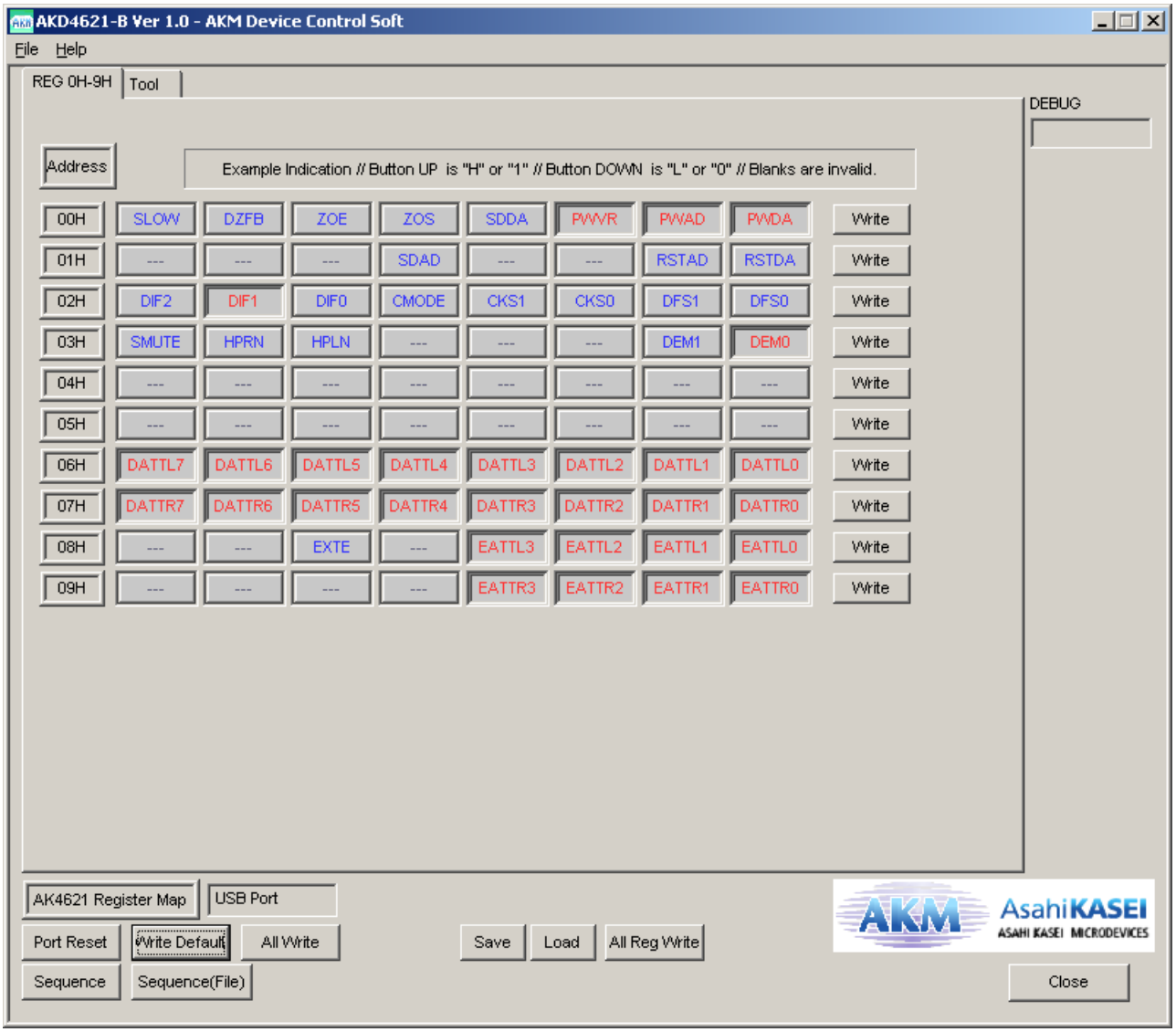


Figure 5. Window of [FUNCTION]

■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write]: Executing write commands for all registers displayed.
4. [Save]: Saving current register settings to a file.
5. [Load]: Executing data write from a saved file.
6. [Data R/W]: “Data R/W” dialog box is popped up.

■ Tab Functions

[Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

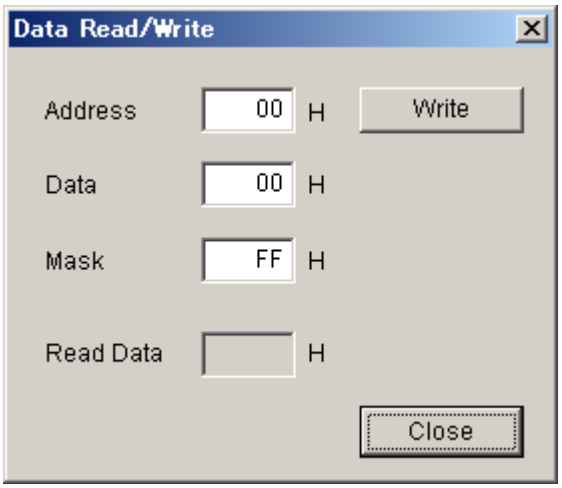


Figure 6. Window of [Data R/W]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write] : Writing to the address specified by “Address” box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

[REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

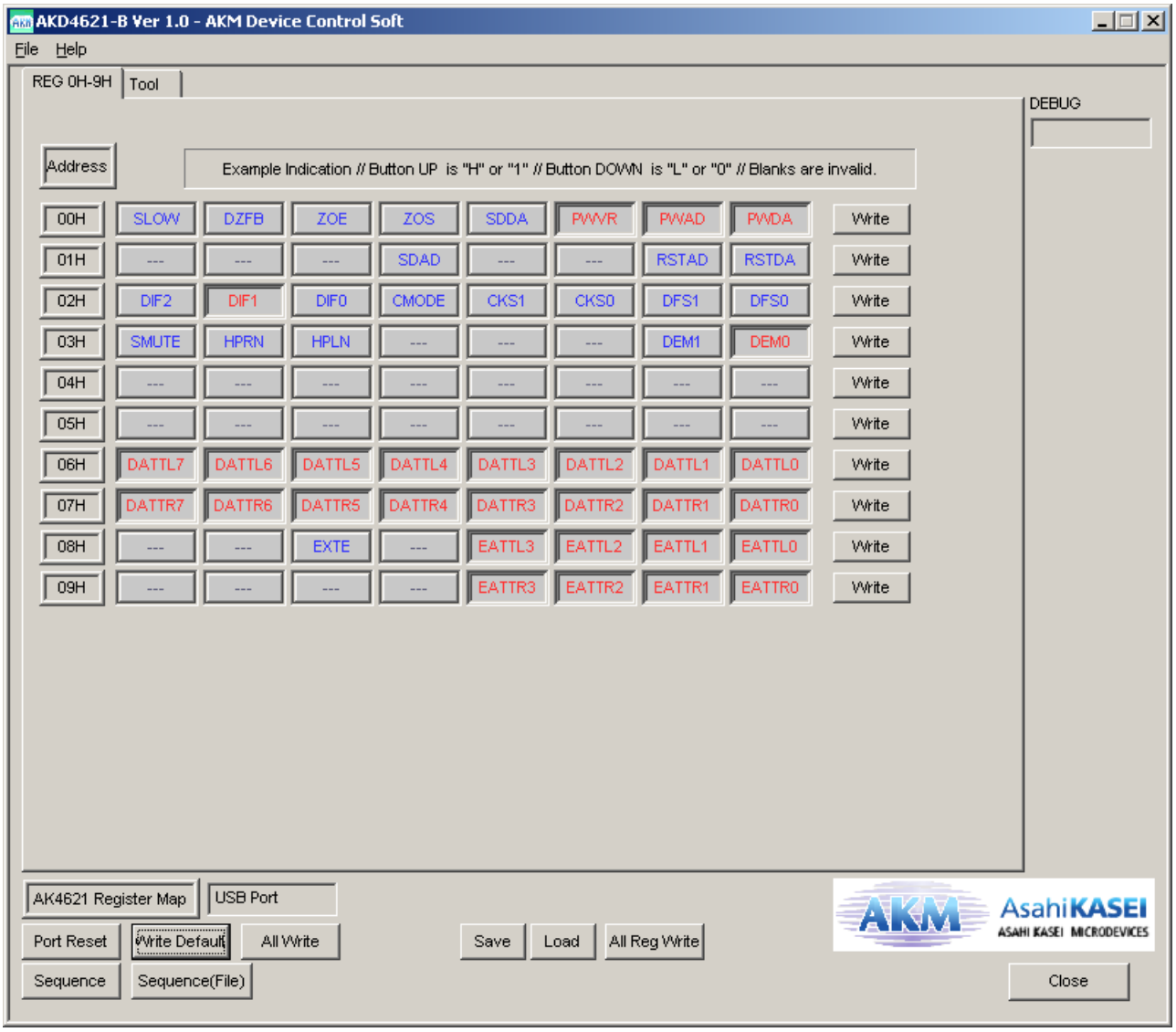


Figure 7. Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.
When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

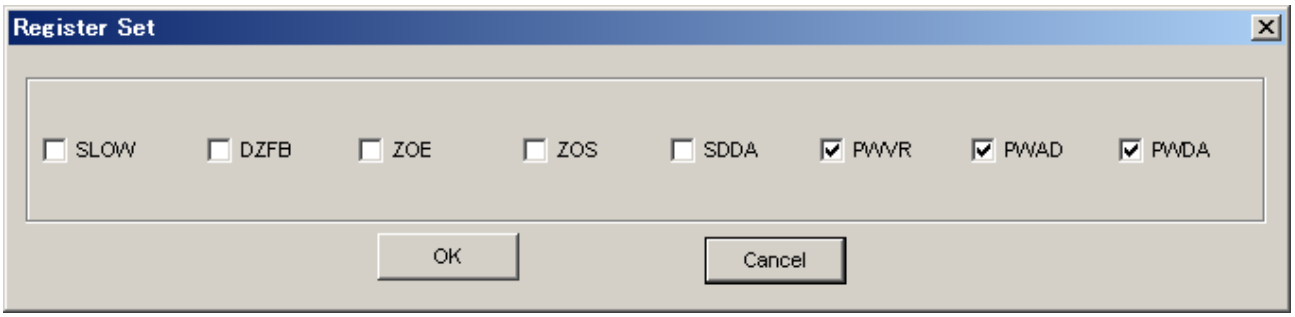


Figure 8. Window of [Register Set]

[Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

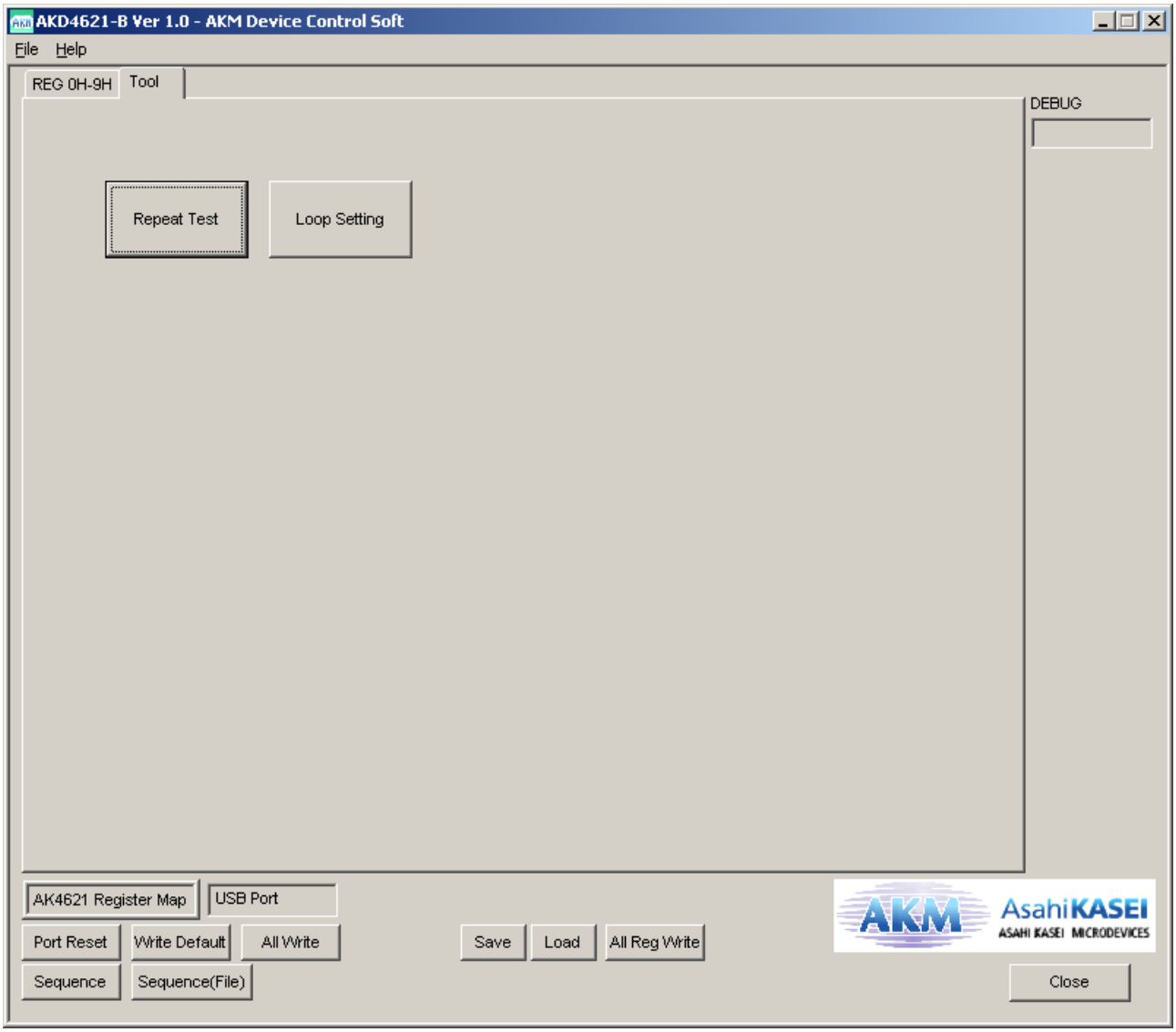


Figure 9. Window of [Tool]

[Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

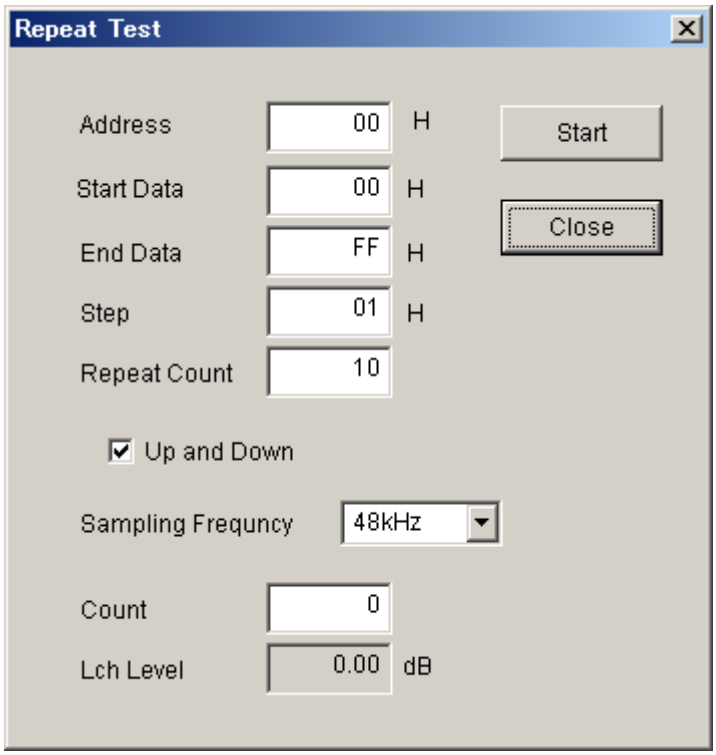


Figure 10. Window of [Repeat Test]

[Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

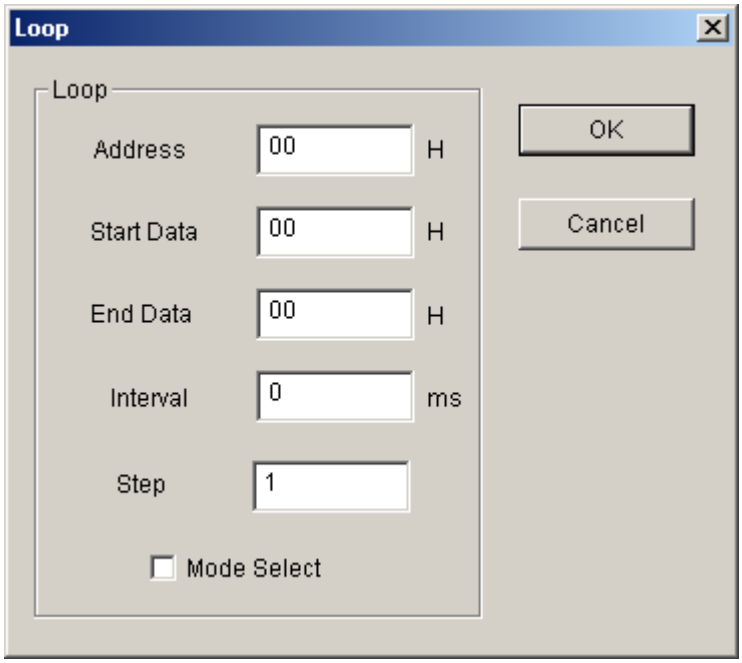


Figure 11. Window of [Loop]

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (fs = 48kHz), 256fs (fs = 96kHz), 128fs (fs = 192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD=5V, DVDD=TVDD=3.3V
- Interface : DIT or DIR
- Temperature : Room

1. ADC (Differencial)

fs=48kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	20kHzLPF	104.0	104.0
S/(N+D)	1kHz, -60dB	20kHzLPF	53.7	53.8
DR	1kHz, -60dB	20kHzLPF, A-weighted	116.1	116.1
S/N	“0” data	20kHzLPF, A-weighted	116.1	116.1

fs=96kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kHzLPF	102.8	102.8
S(N+D)	1kHz, -60dB	40kHzLPF	49.5	49.6
DR	1kHz, -60dB	40kHzLPF, A-weighted	115.1	115.2
S/N	“0” data	40kHzLPF, A-weighted	115.2	115.4

fs=192kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kHzLPF	102.7	102.8
S(N+D)	1kHz, -60dB	40kHzLPF	49.9	50.1
DR	1kHz, -60dB	40kHzLPF, A-weighted	115.3	115.6
S/N	“0” data	40kHzLPF, A-weighted	115.5	115.6

2. DAC

fs=48kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	20kHzLPF	99.8	100.2
S/(N+D)	1kHz, -60dB	20kHzLPF	52.7	52.7
DR	1kHz, -60dB	22kHzLPF, A-weighted	114.8	114.8
S/N	“0” data	22kHzLPF, A-weighted	115.0	114.9

fs=96kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kLPF	99.2	99.4
S/(N+D)	1kHz, -60dB	40kLPF	50.0	50.0
DR	1kHz, -60dB	40kHzLPF, A-weighted	114.9	114.9
S/N	“0” data	40kHzLPF, A-weighted	115.0	115.0

fs=192kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kHzLPF	99.2	99.4
S/(N+D)	1kHz, -60dB	40kHzLPF	49.7	49.8
DR	1kHz, -60dB	40kHzLPF, A-weighted	114.8	114.7
S/N	“0” data	40kHzLPF, A-weighted	115.1	115.1

3. PLOT DATA

3.1 ADC (fs=48kHz)

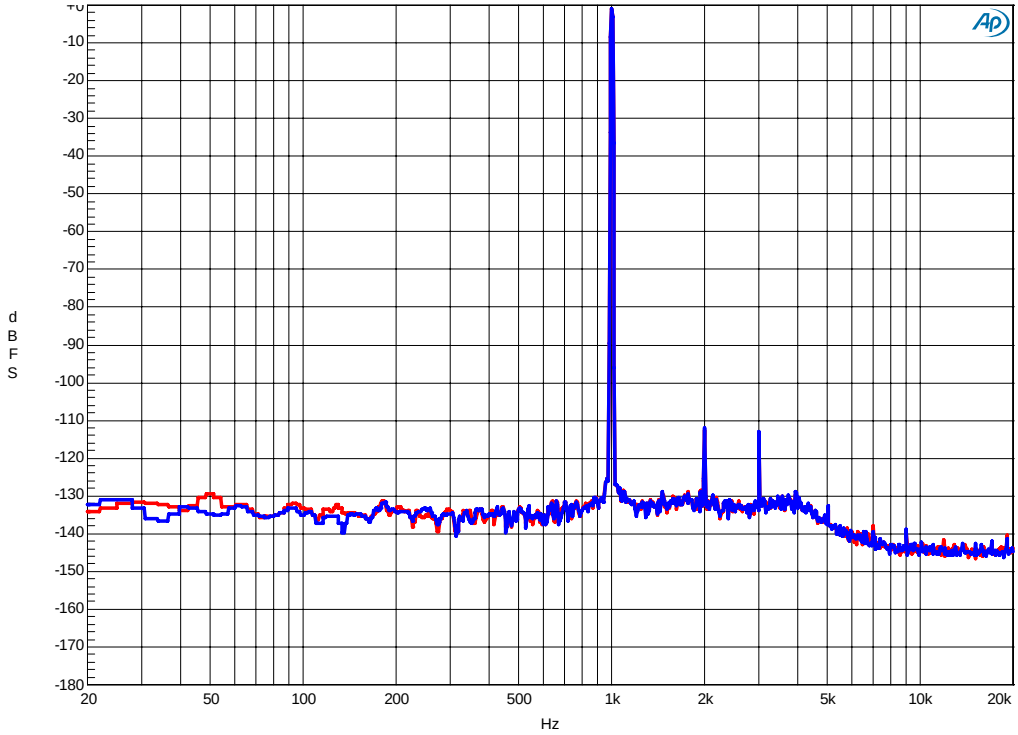


Figure 12. FFT (fin=1kHz, Input Level=-1dBFS)

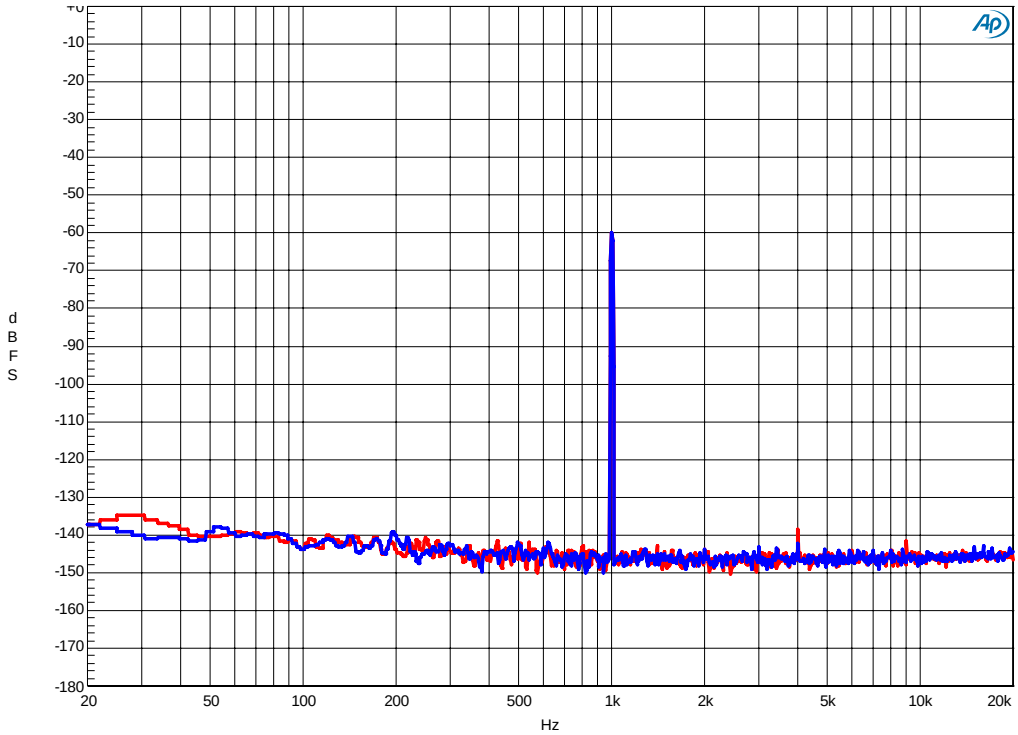


Figure 13. FFT (fin=1kHz, Input Level=-60dBFS)

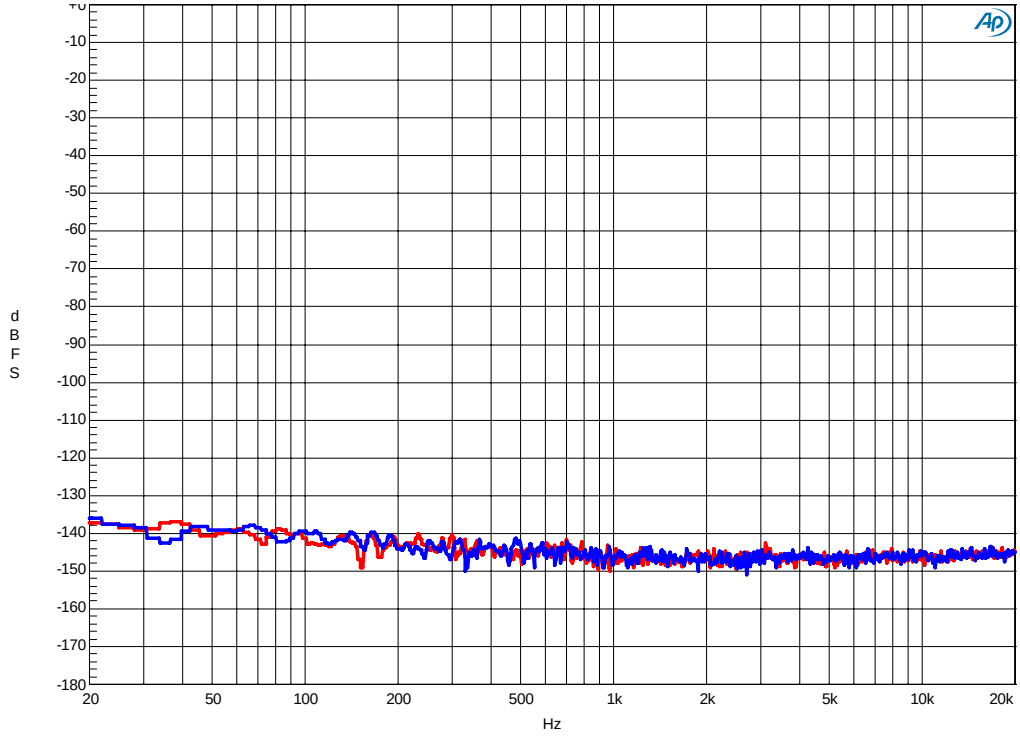


Figure 14. FFT (Noise Floor)

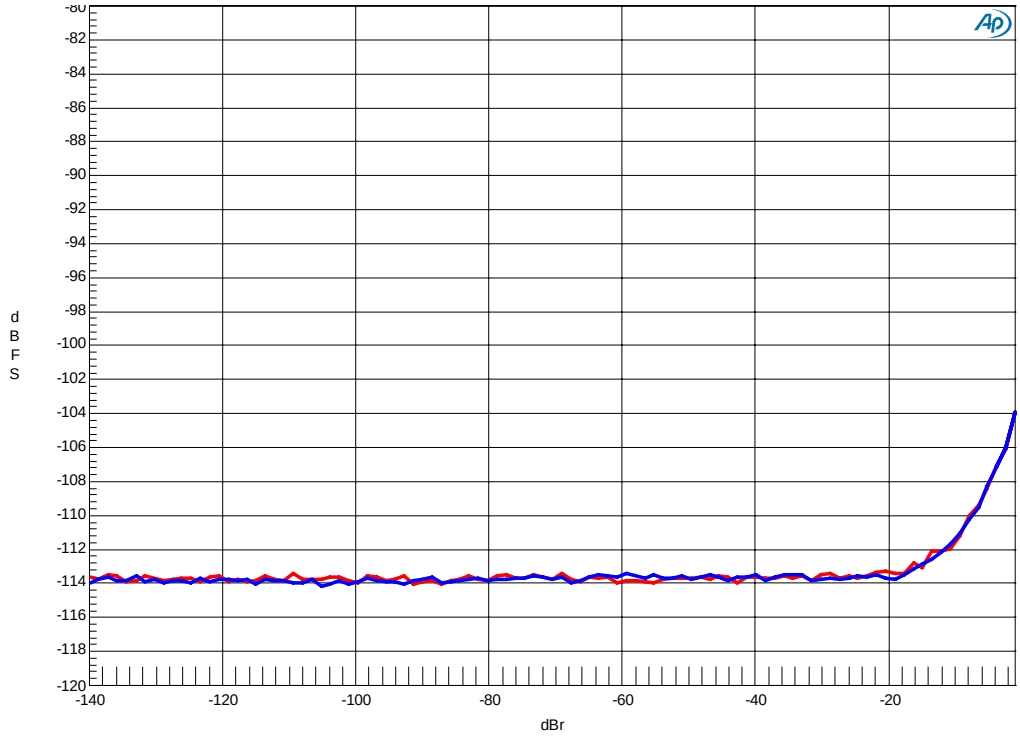


Figure 15. THD+N vs. Input level (fin=1kHz)

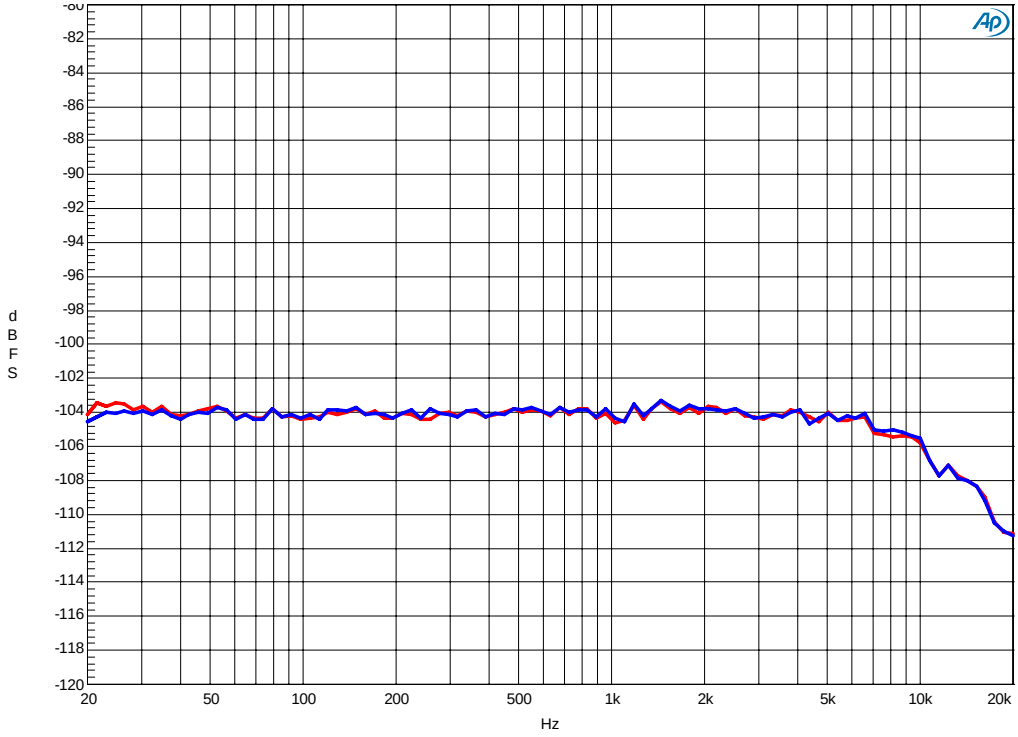


Figure 16. THD +N vs. Input Frequency (Input level=-1dBFS)

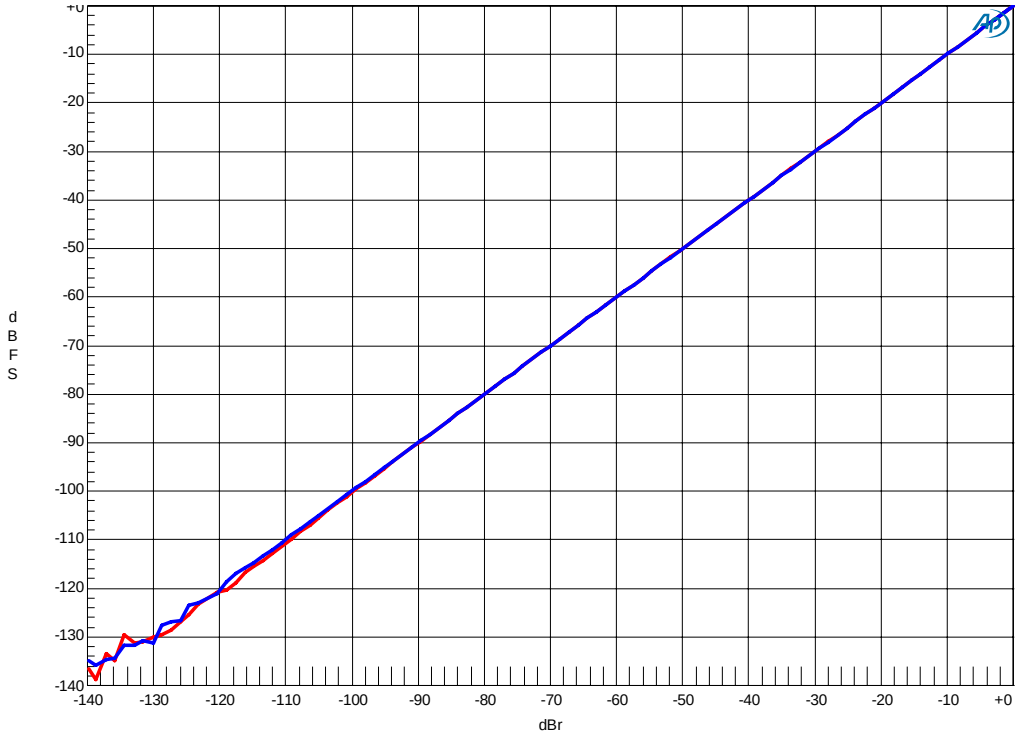


Figure 17. Linearity (fin=1kHz)

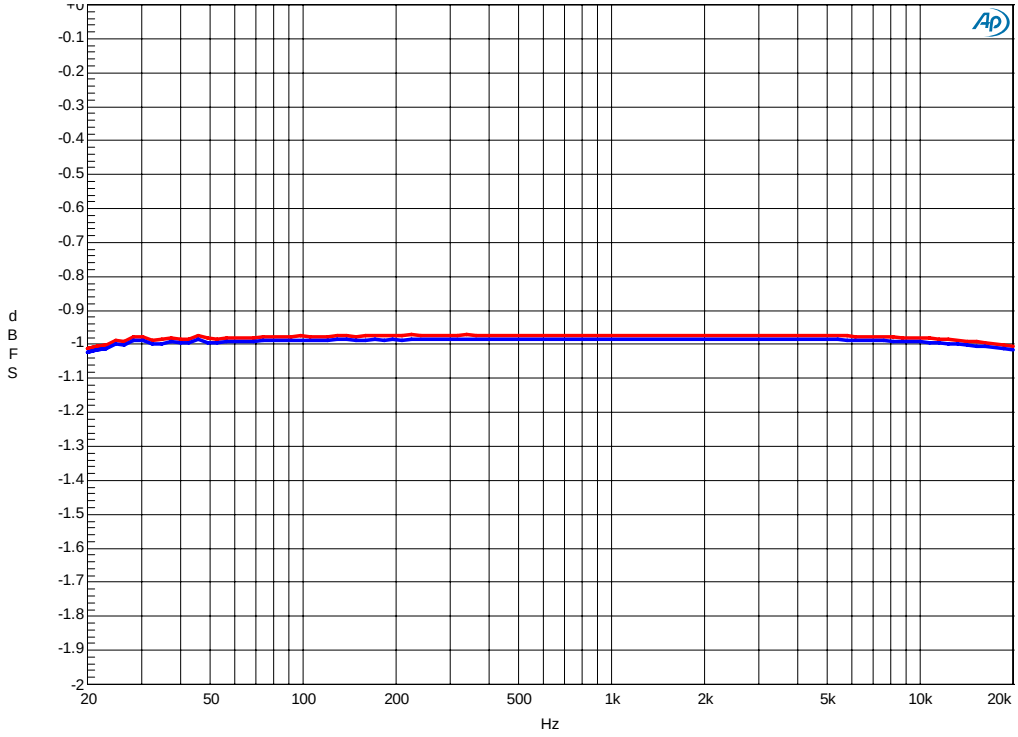


Figure 18. Frequency Response(Input level=-1dBFS)

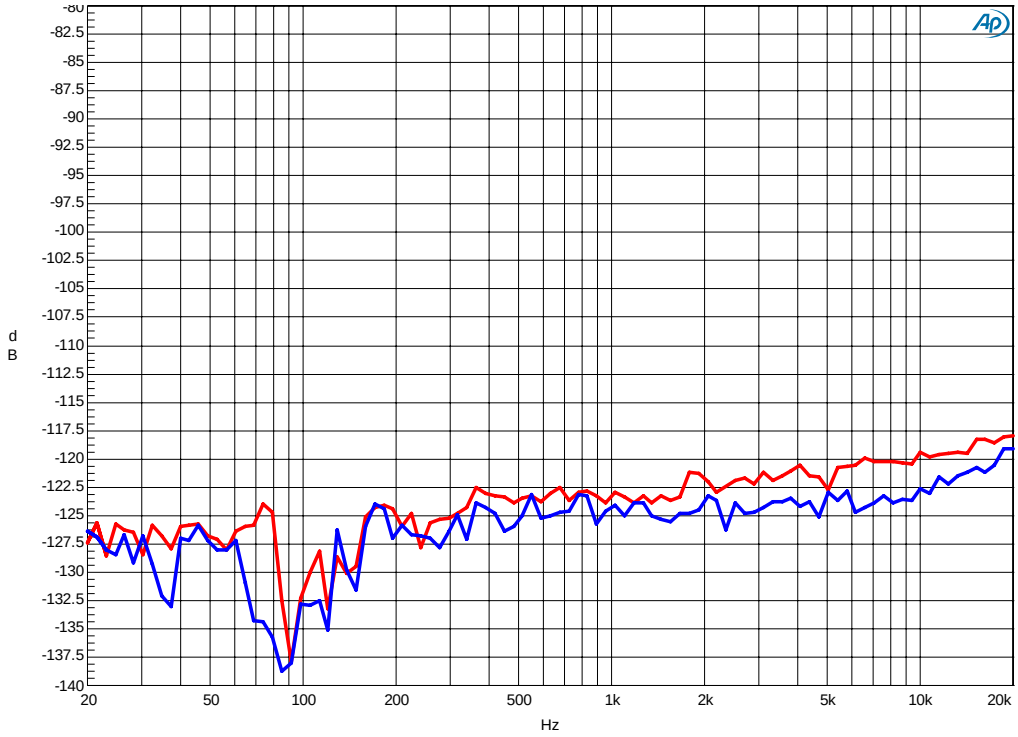


Figure 19. Crosstalk

3.2 ADC (fs=96kHz)

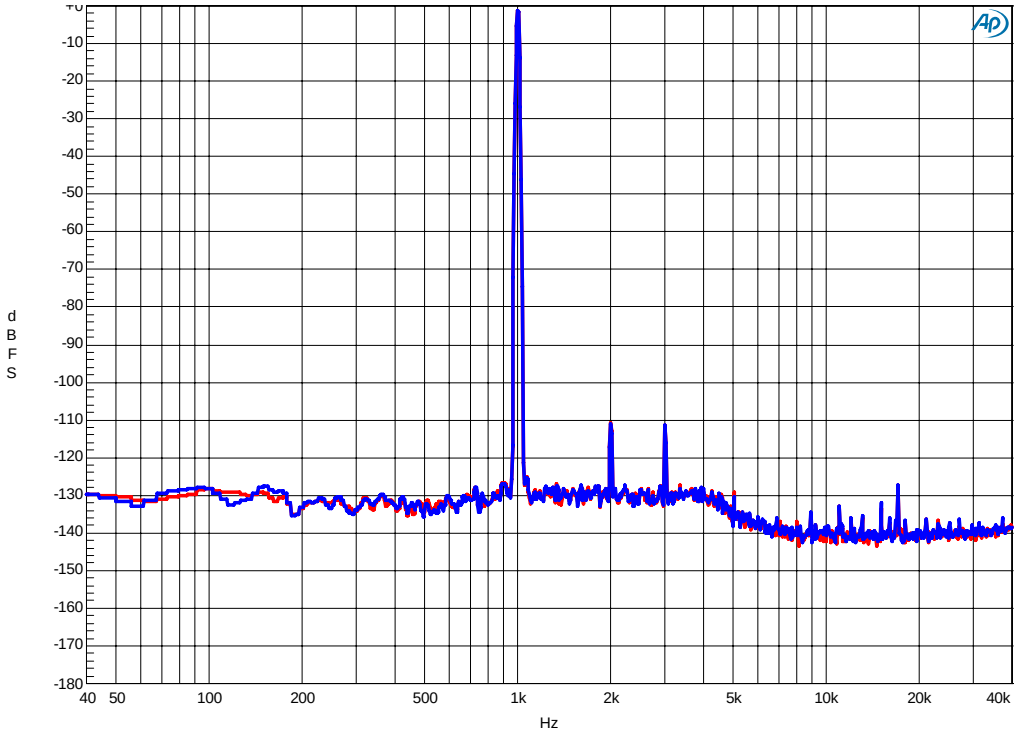


Figure 20. FFT (fin=1kHz, Input Level=-1dBFS)

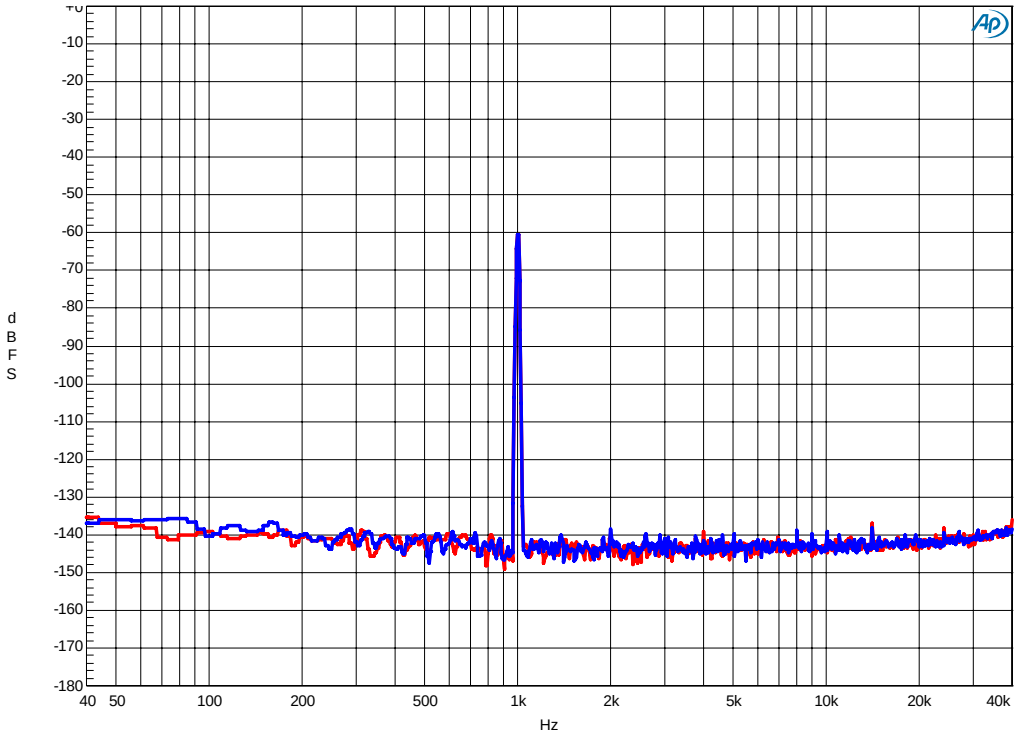


Figure 21. FFT (fin=1kHz, Input Level=-60dBFS)

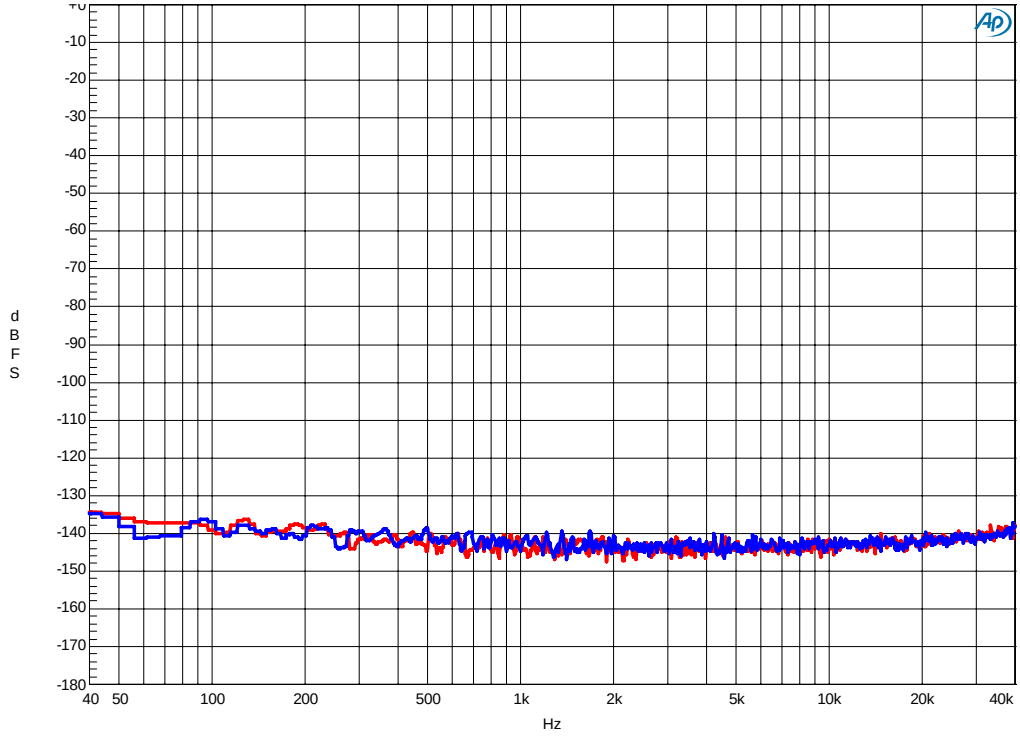


Figure 22. FFT (Noise Floor)

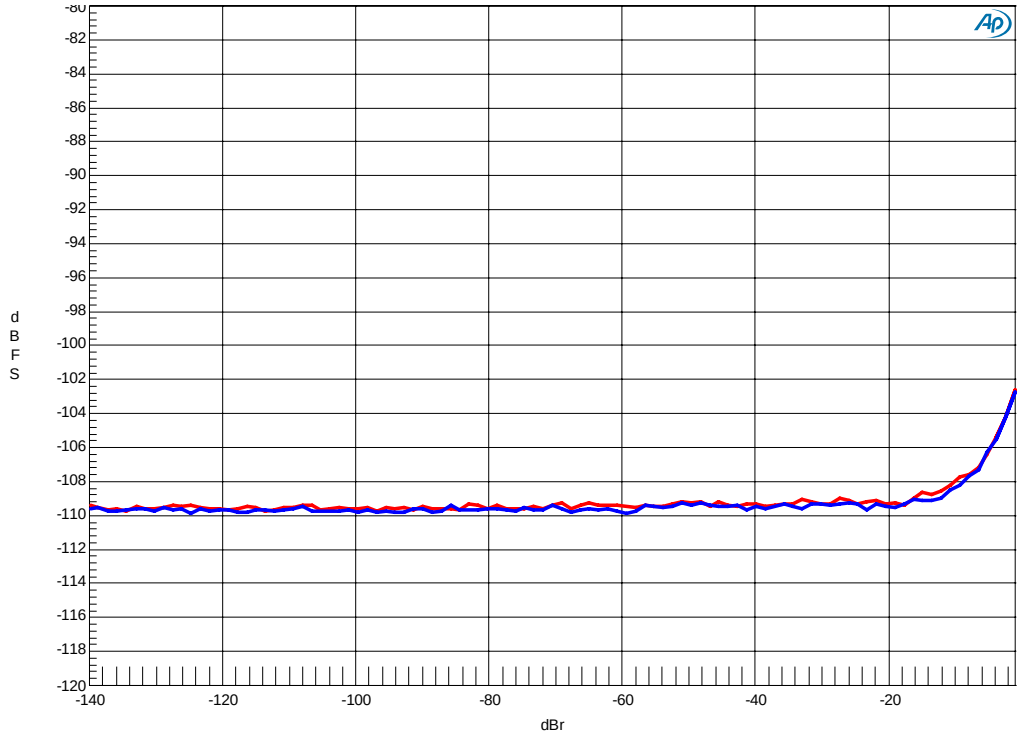


Figure 23. THD +N vs. Input level (fin=1kHz)

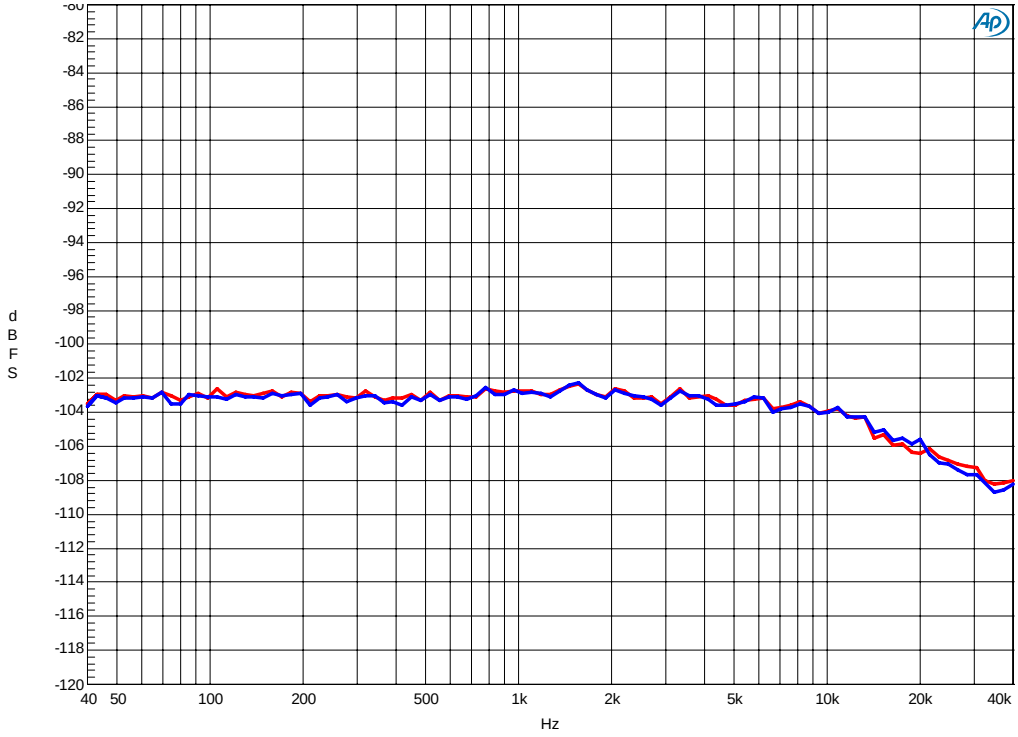


Figure 24. THD +N vs. Input Frequency (Input level=-1dBFS)

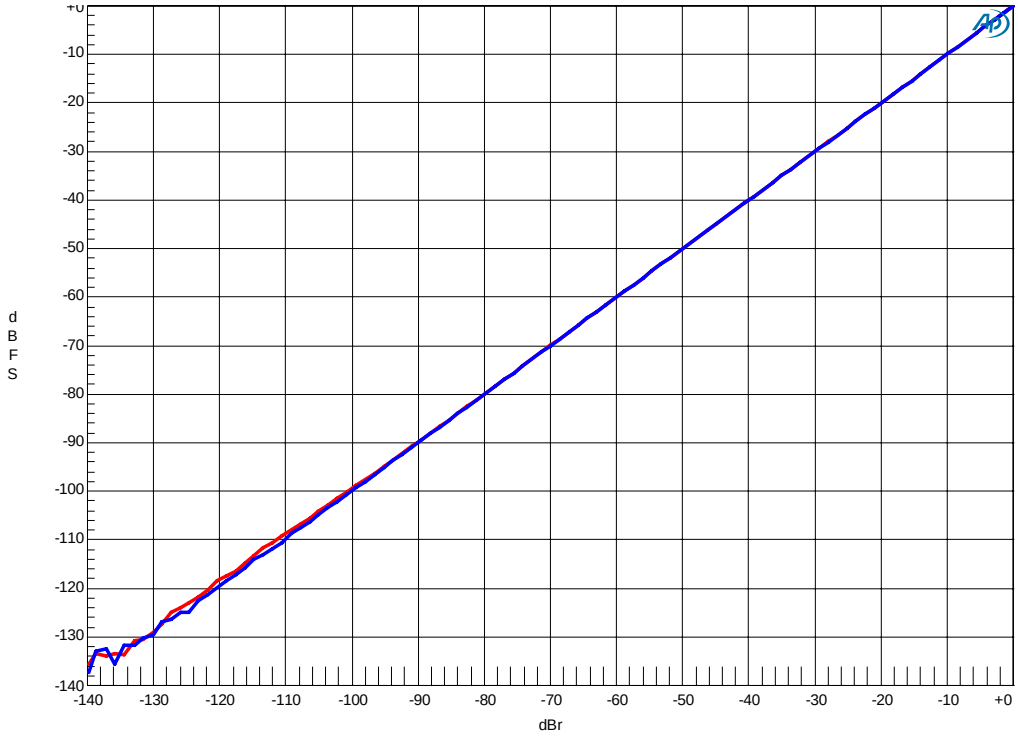


Figure 25. Linearity (fin=1kHz)

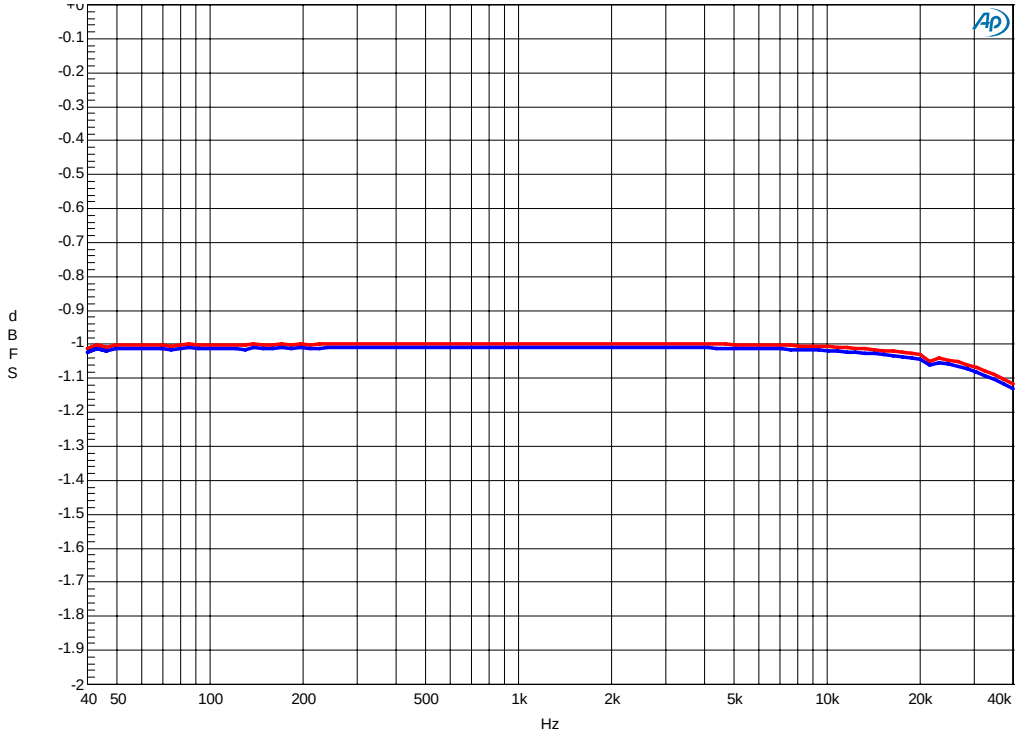


Figure 26. Frequency Response(Input level=-1dBFS)

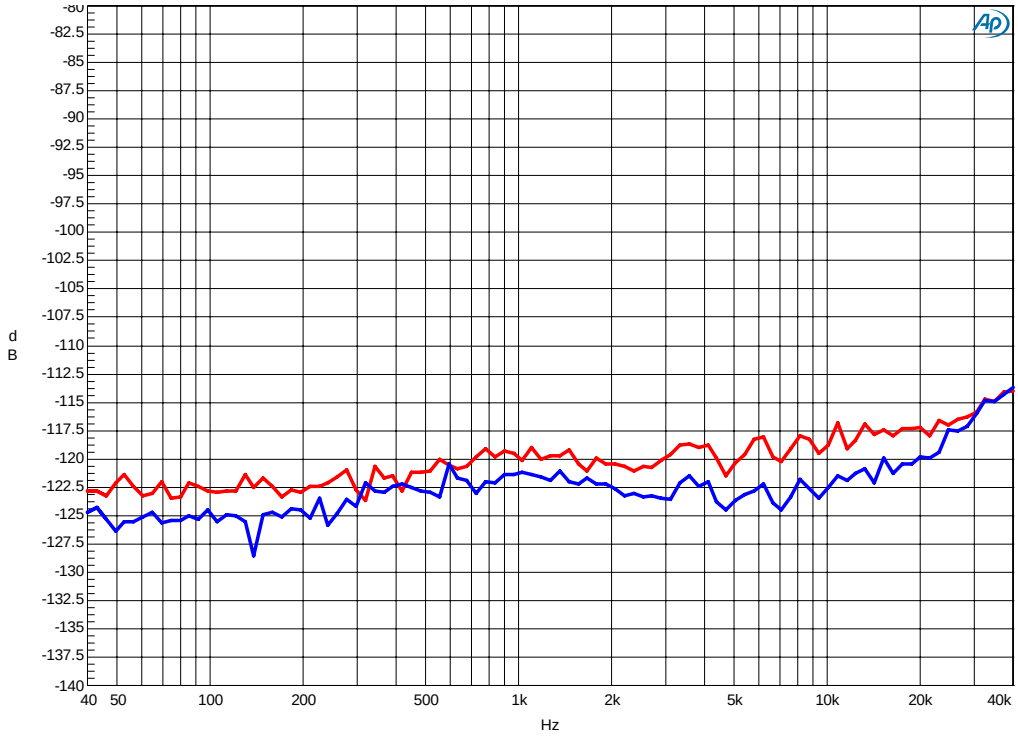


Figure 27. Crosstalk

3.3 ADC (fs=192kHz)

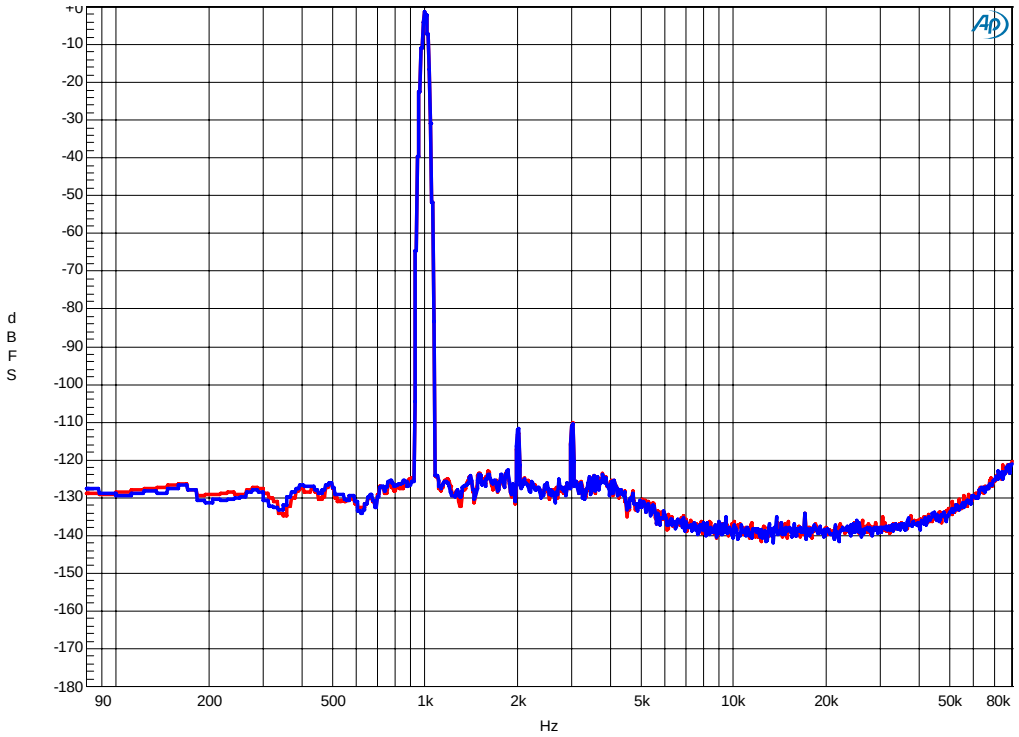


Figure 28. FFT (fin=1kHz, Input Level=-1dBFS)

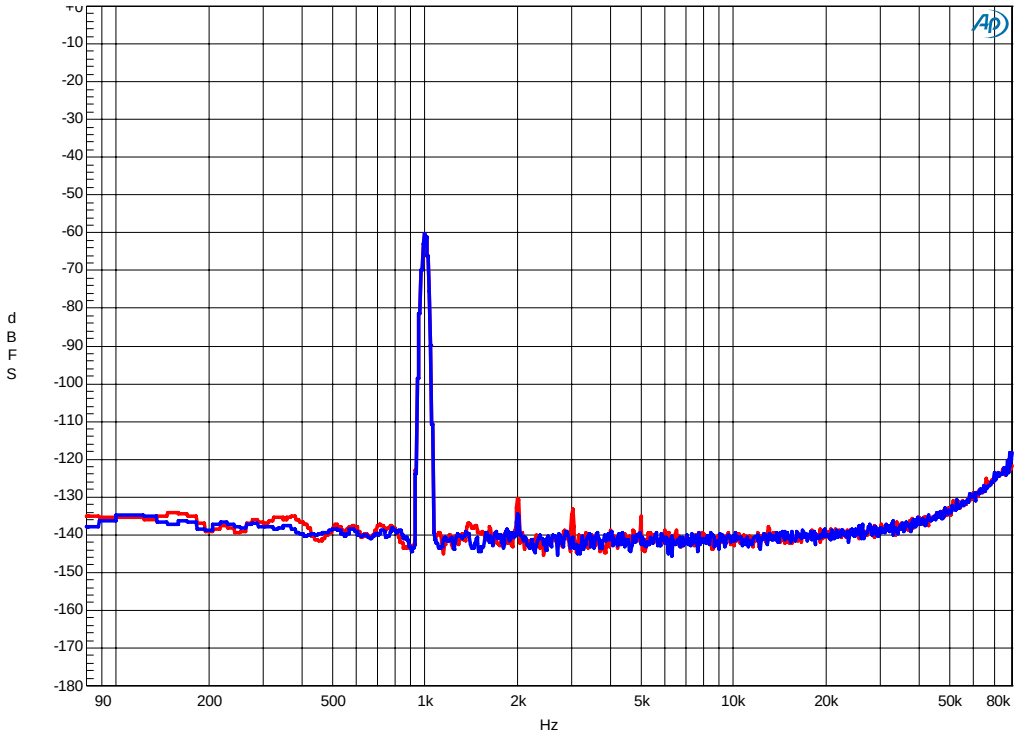


Figure 29. FFT (fin=1kHz, Input Level=-60dBFS)

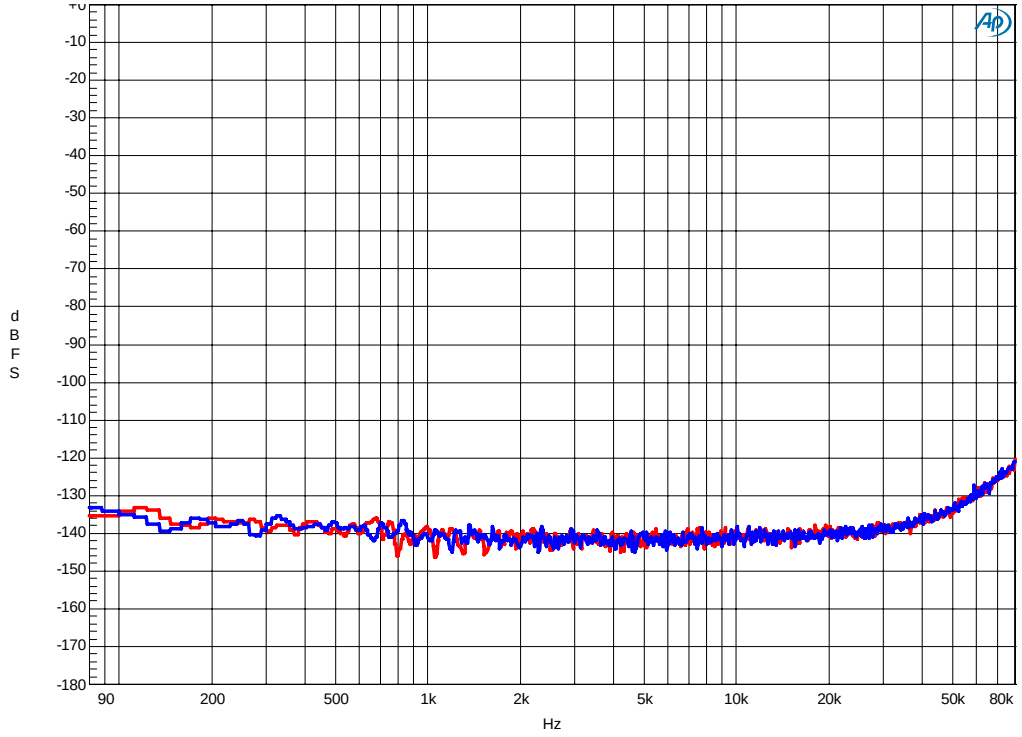


Figure 30. FFT (Noise Floor)

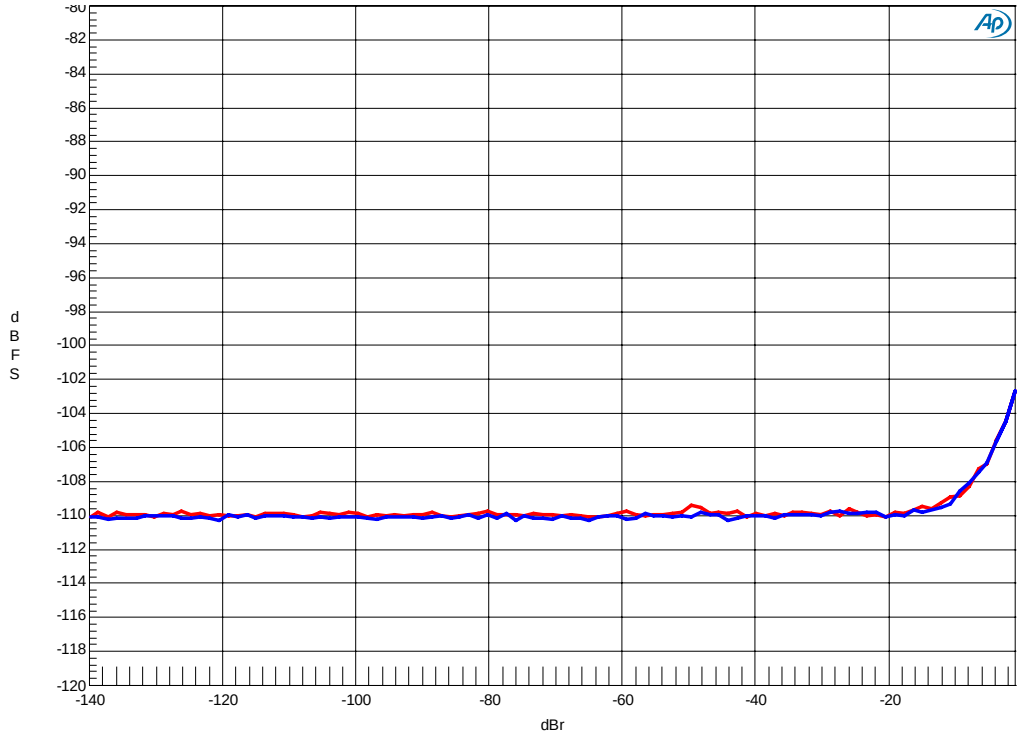


Figure 31. THD+N vs. Input level (fin=1kHz)

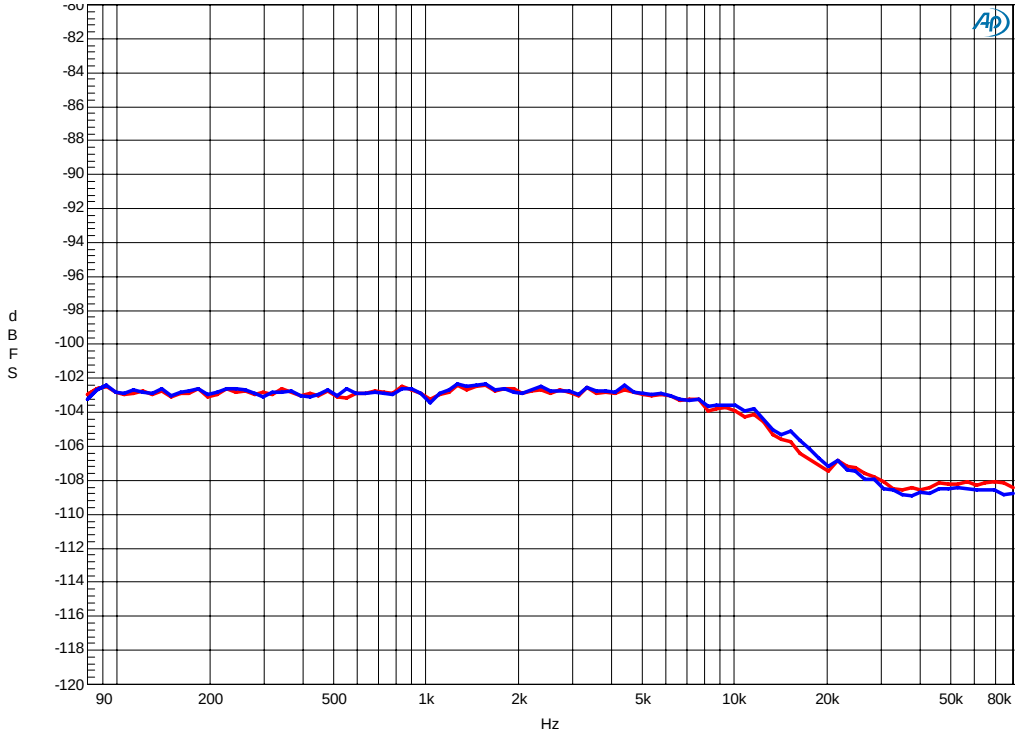


Figure 32. THD+N vs. Input Frequency (Input level=-1dBFS)

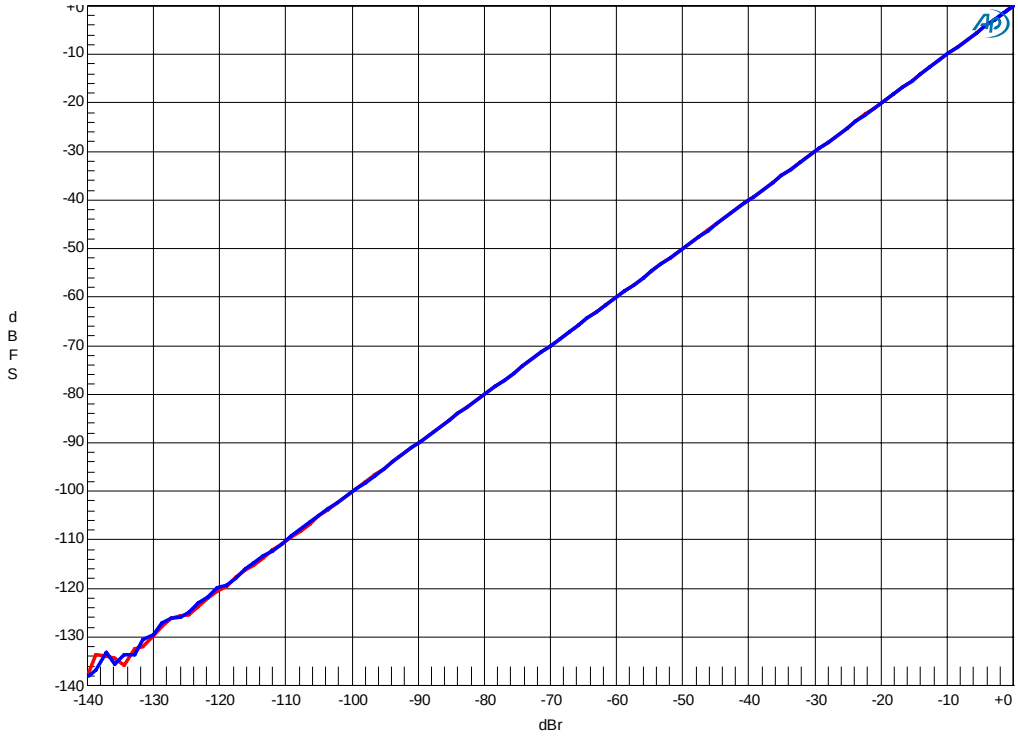


Figure 33. Linearity (fin=1kHz)

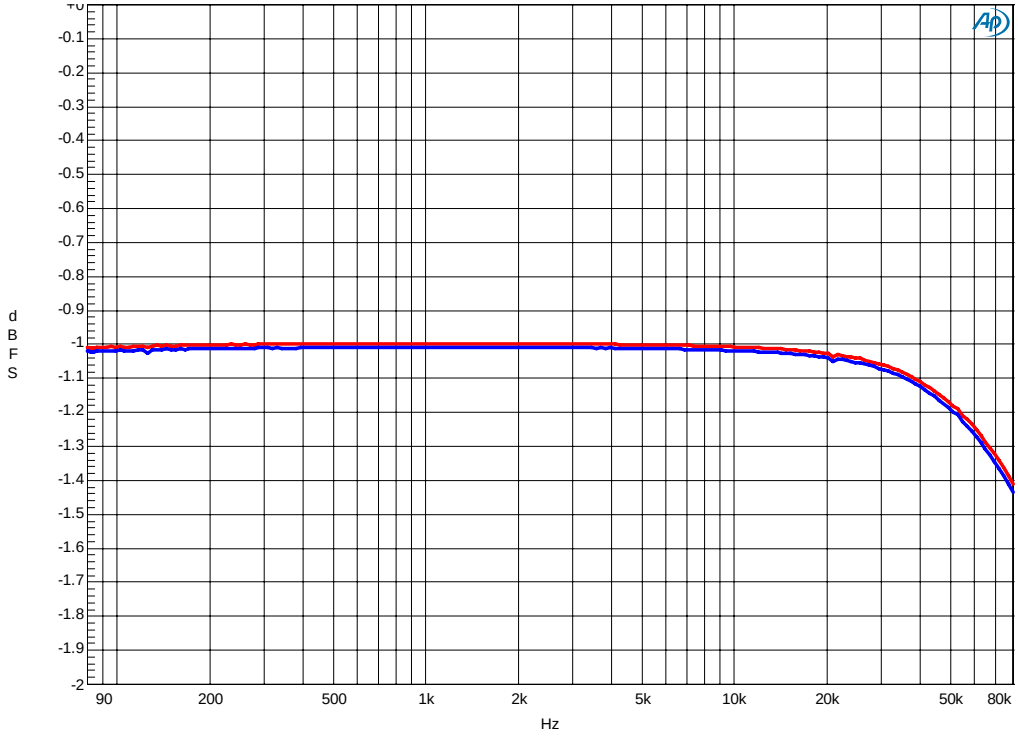


Figure 34. Frequency Response(Input level=-1dBFS)

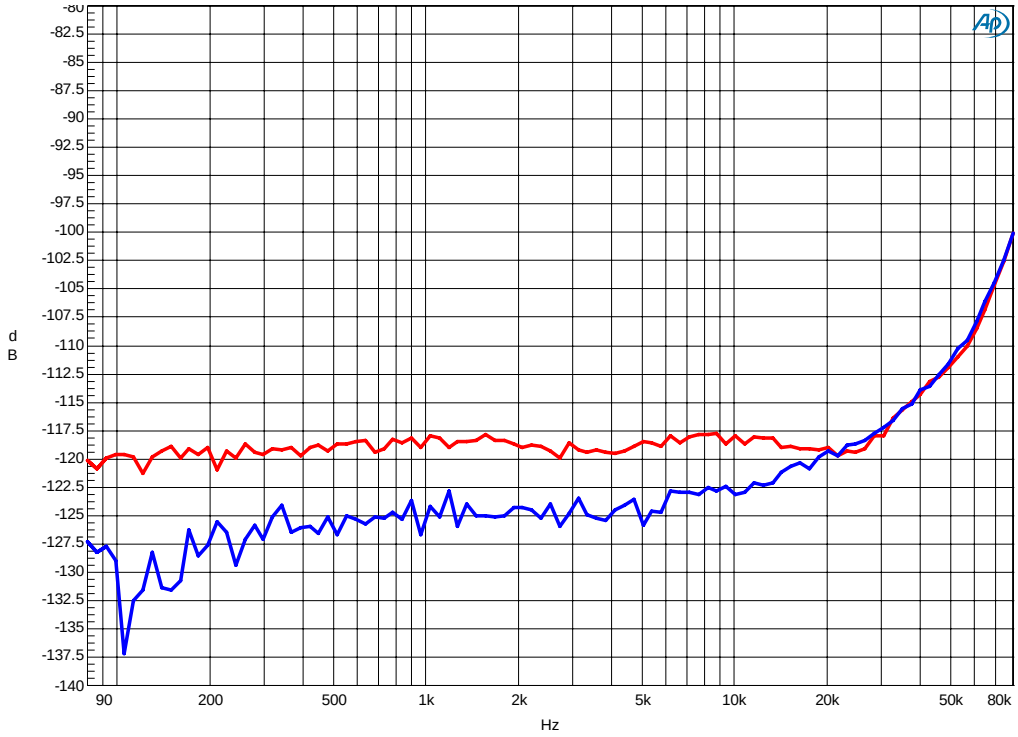


Figure 35. Crosstalk

3.4 DAC (fs=48kHz)

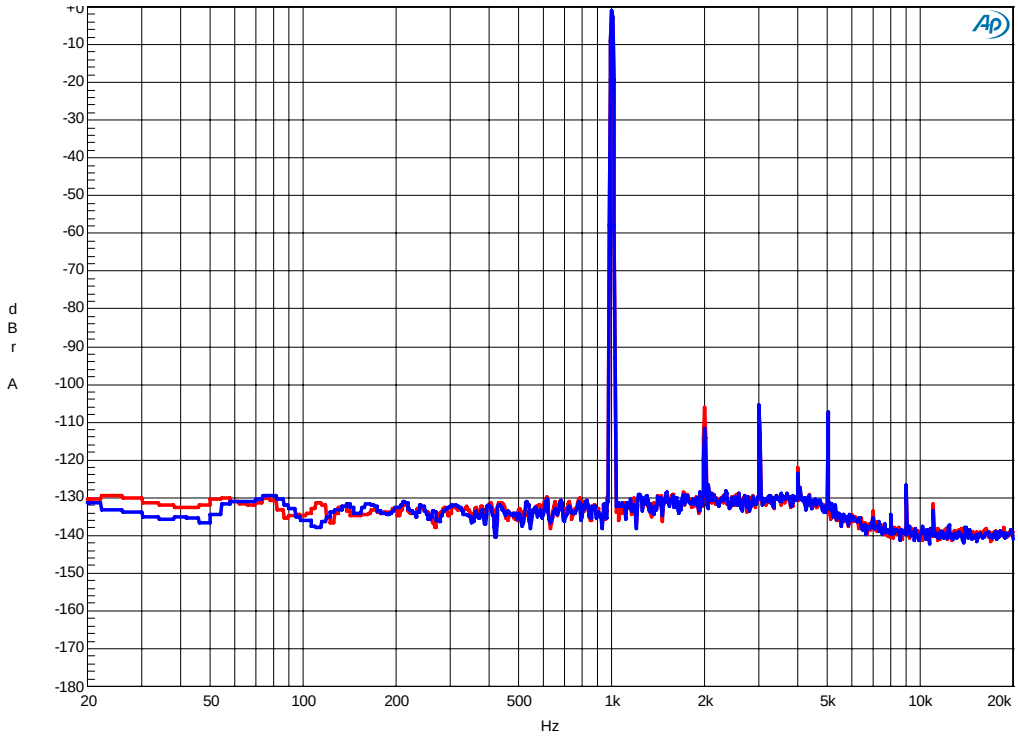


Figure 36. FFT (fin=1kHz, Input Level=-1dBFS)

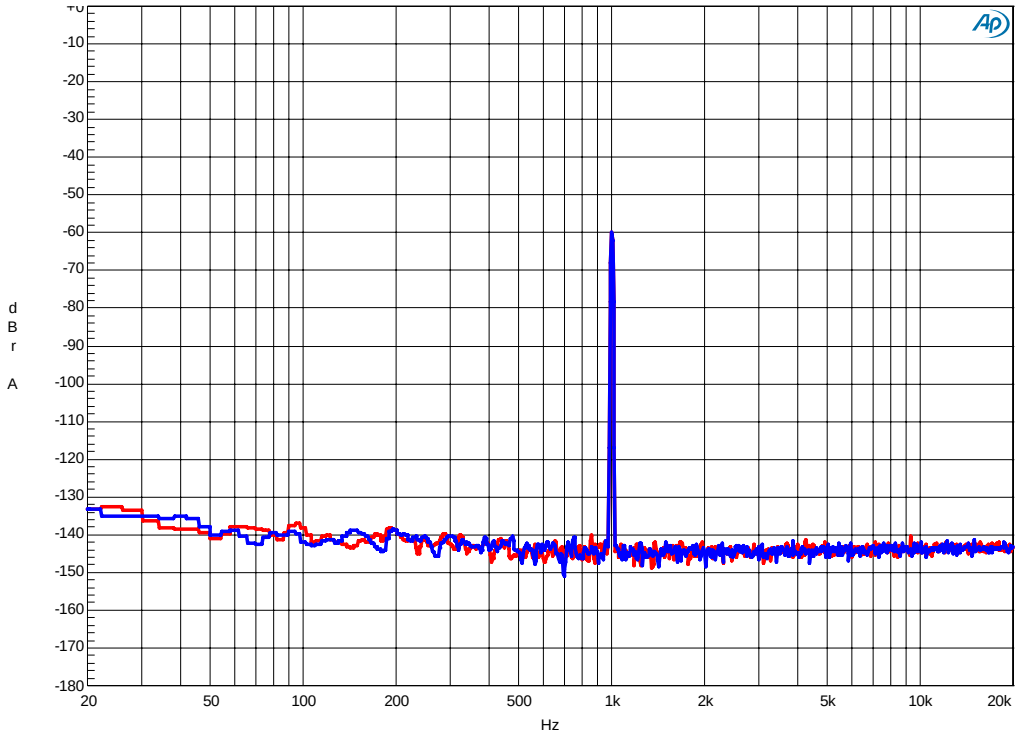


Figure 37. FFT (fin=1kHz, Input Level=-60dBFS)

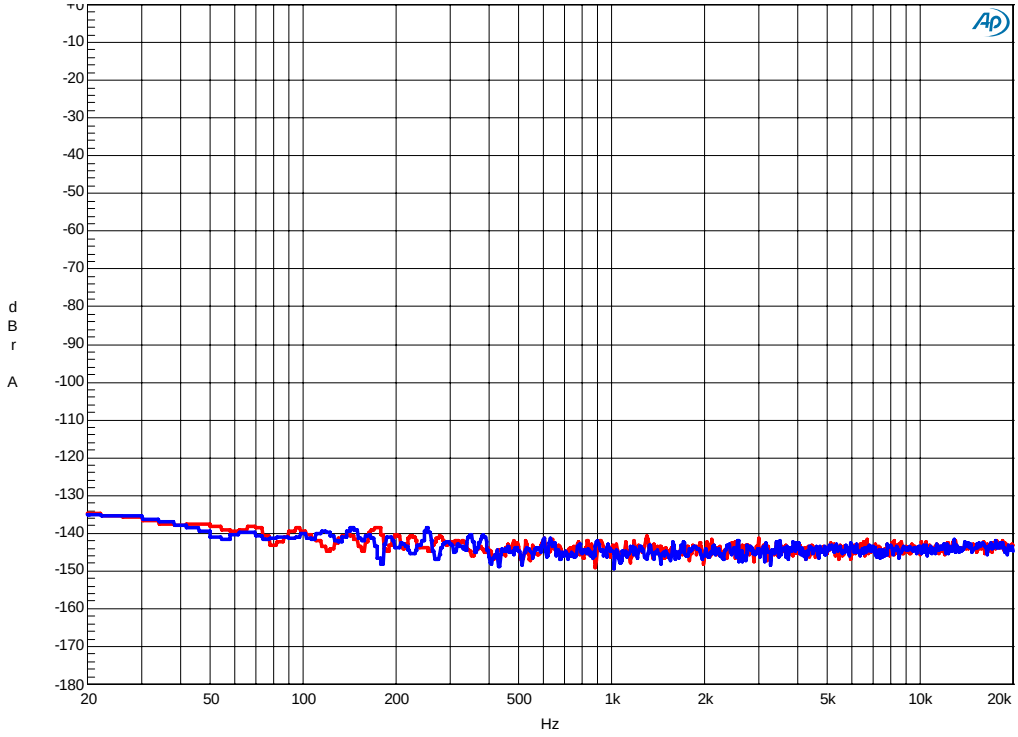


Figure 38. FFT (Noise Floor)

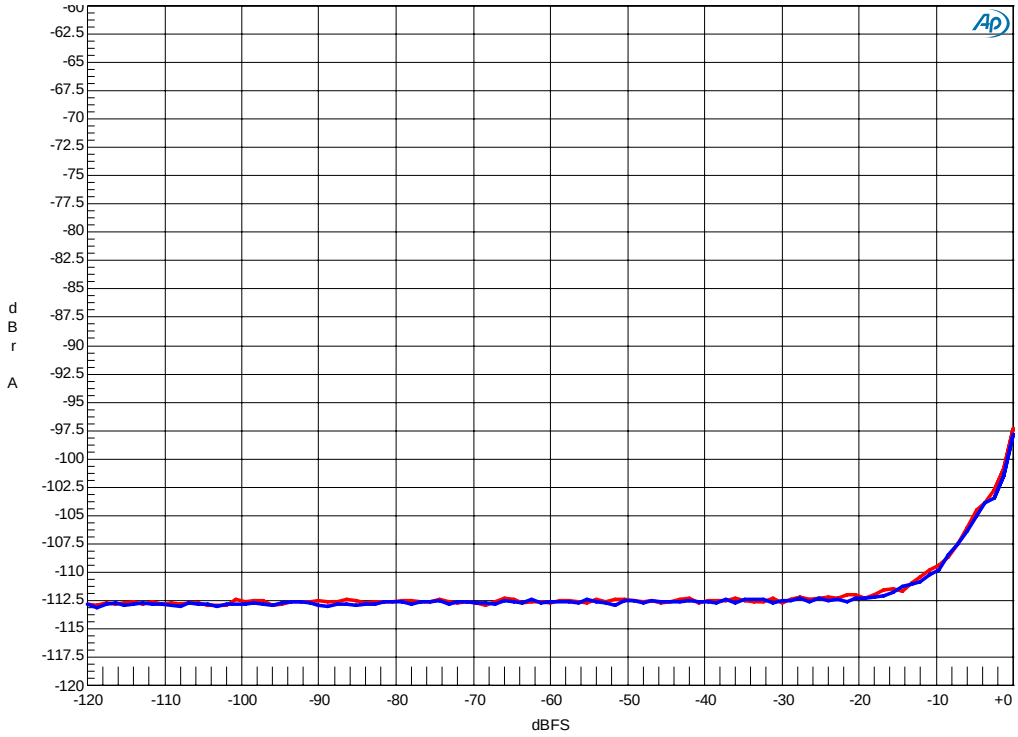


Figure 39. THD+N vs. Input level (fin=1kHz)

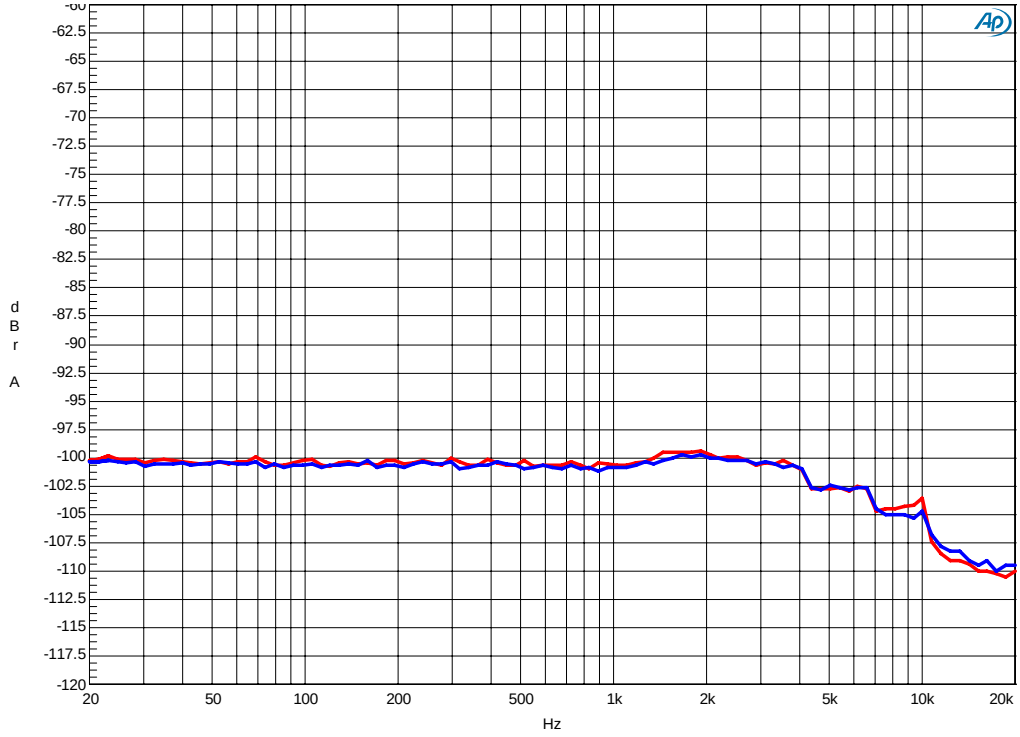


Figure 40. THD +N vs. Input Frequency (Input level=-1dBFS)

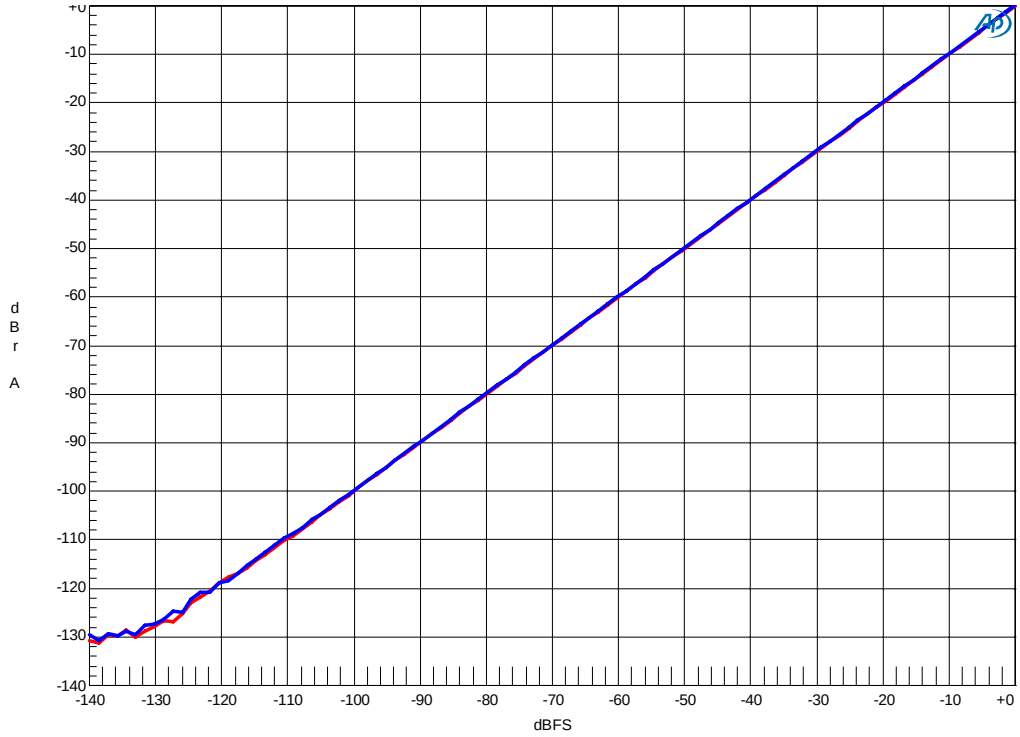


Figure 41. Linearity (fin=1kHz)

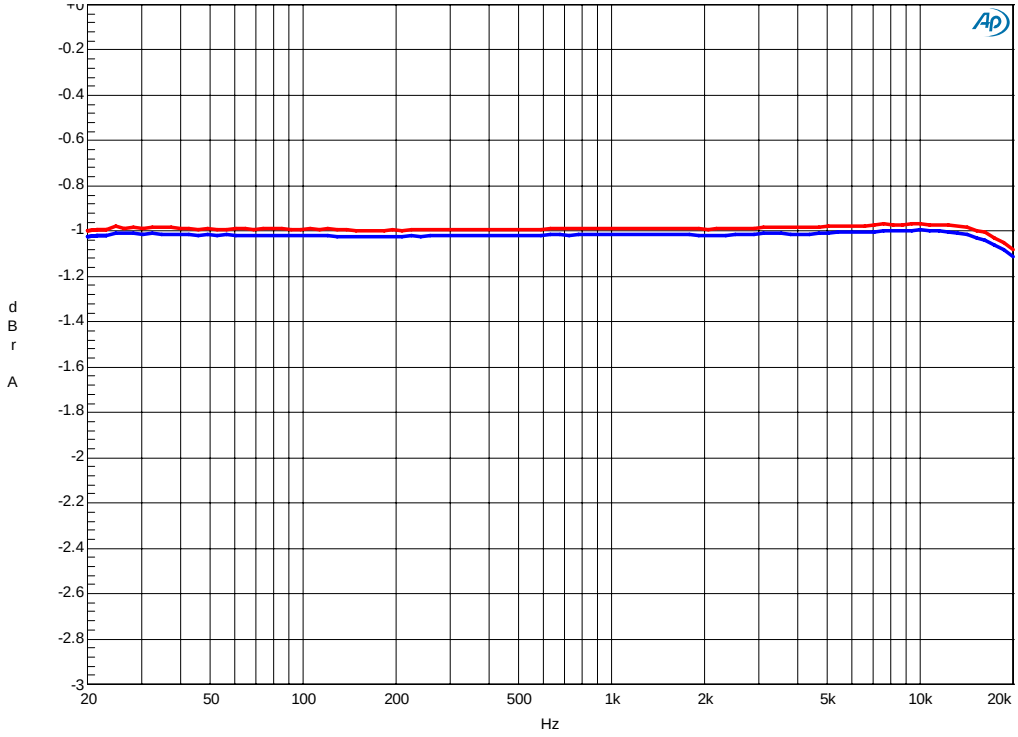


Figure 42. Frequency Response (Input level=-1dBFS)

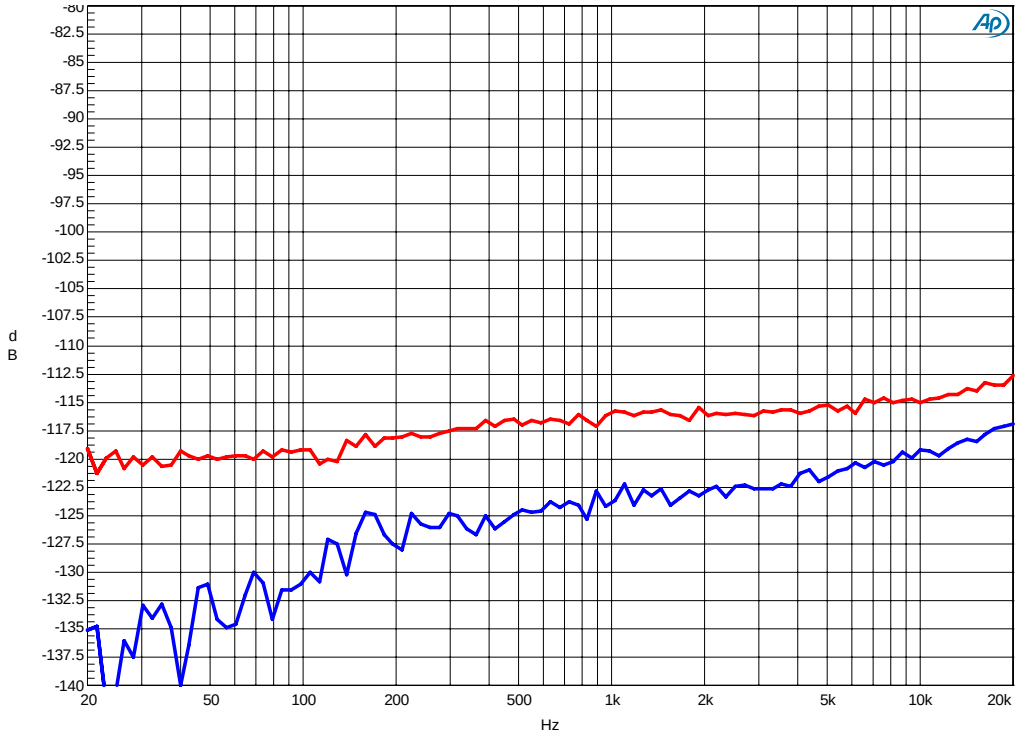


Figure 43. Crosstalk

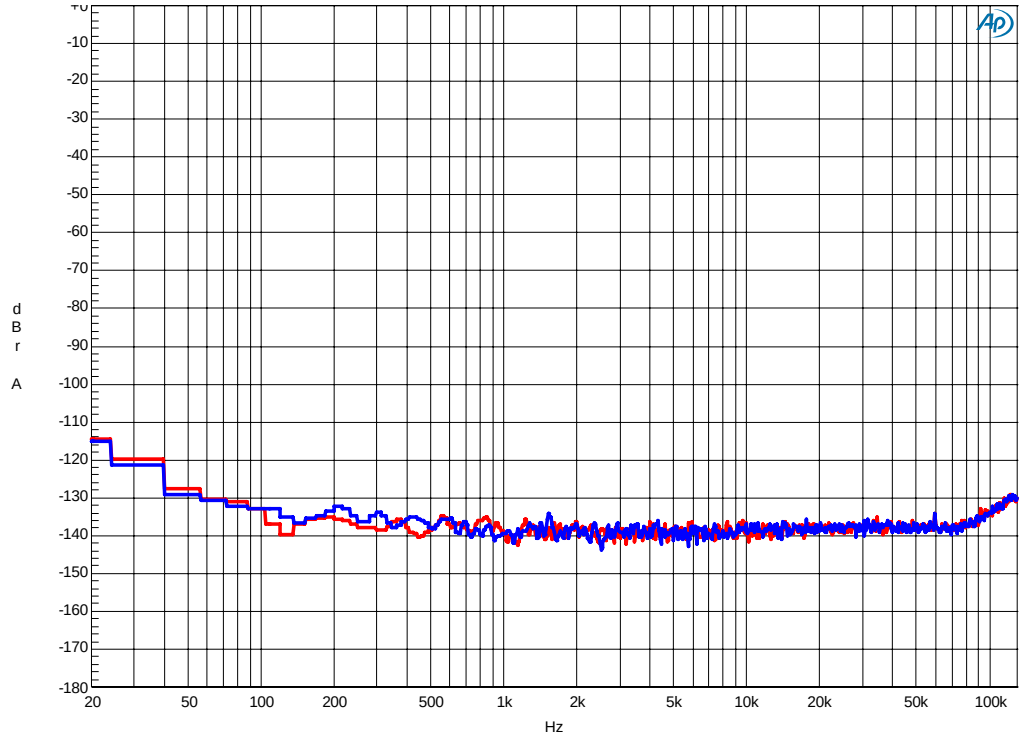


Figure 44. Out-of-band Noise

3.5 DAC (fs=96kHz)

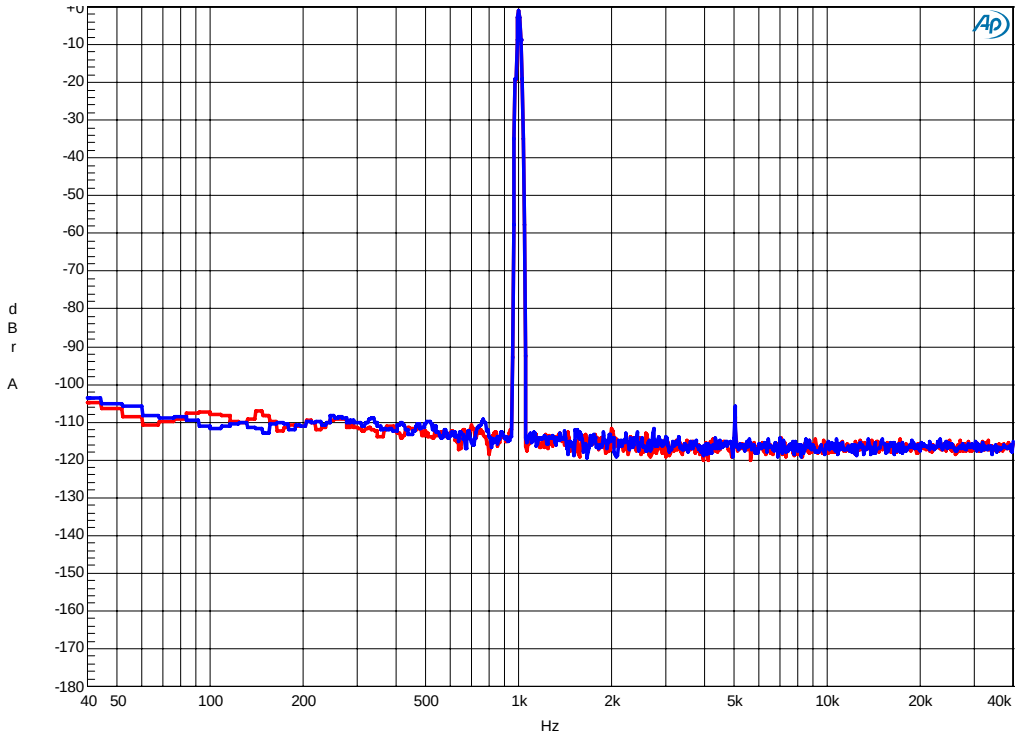


Figure 45. FFT (fin=1kHz, Input Level=-1dBFS)

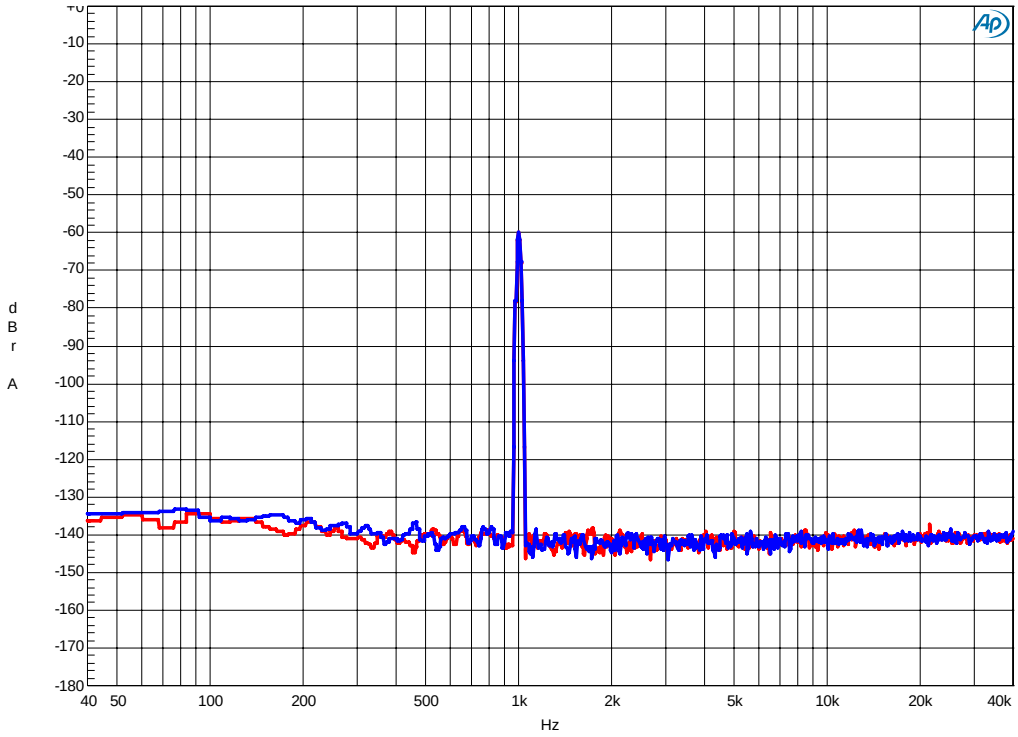


Figure 46. FFT (fin=1kHz, Input Level=-60dBFS)

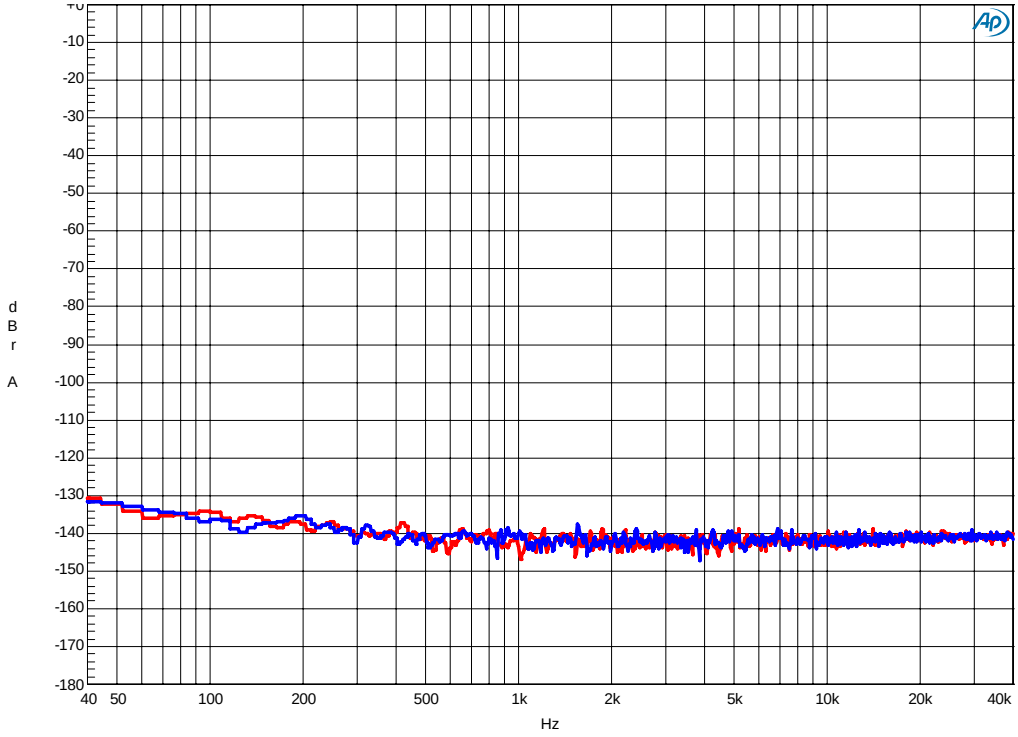


Figure 47. FFT (Noise Floor)

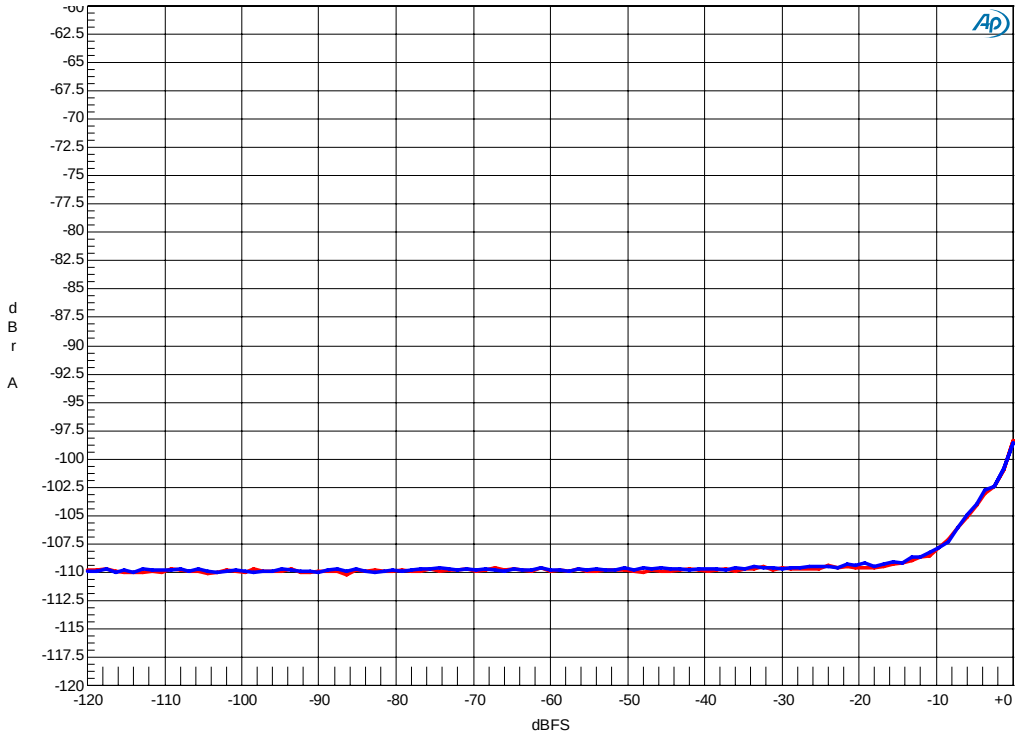


Figure 48. THD +N vs. Input level (fin=1kHz)

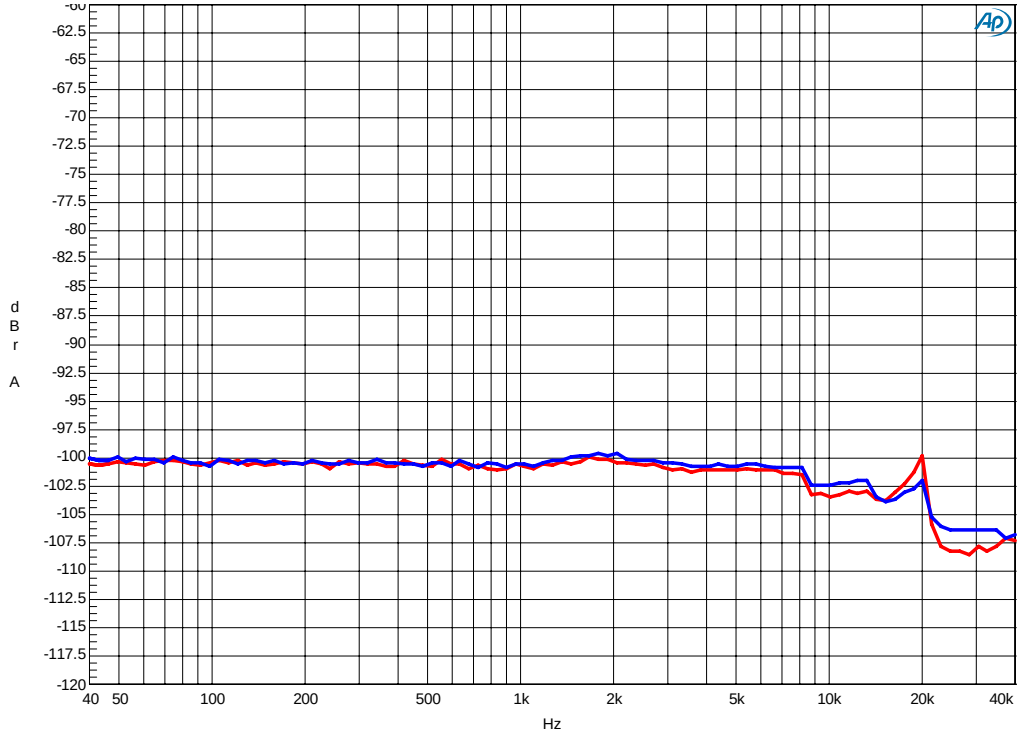


Figure 49. THD +N vs. Input Frequency (Input level=-1dBFS)

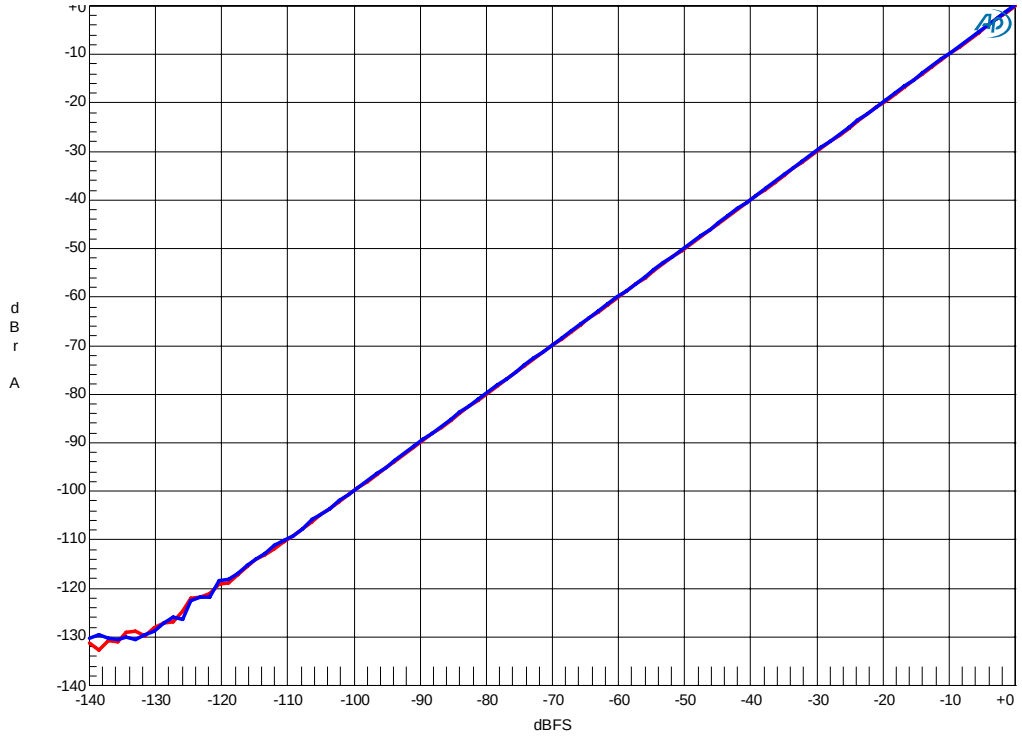


Figure 50. Linearity (fin=1kHz)

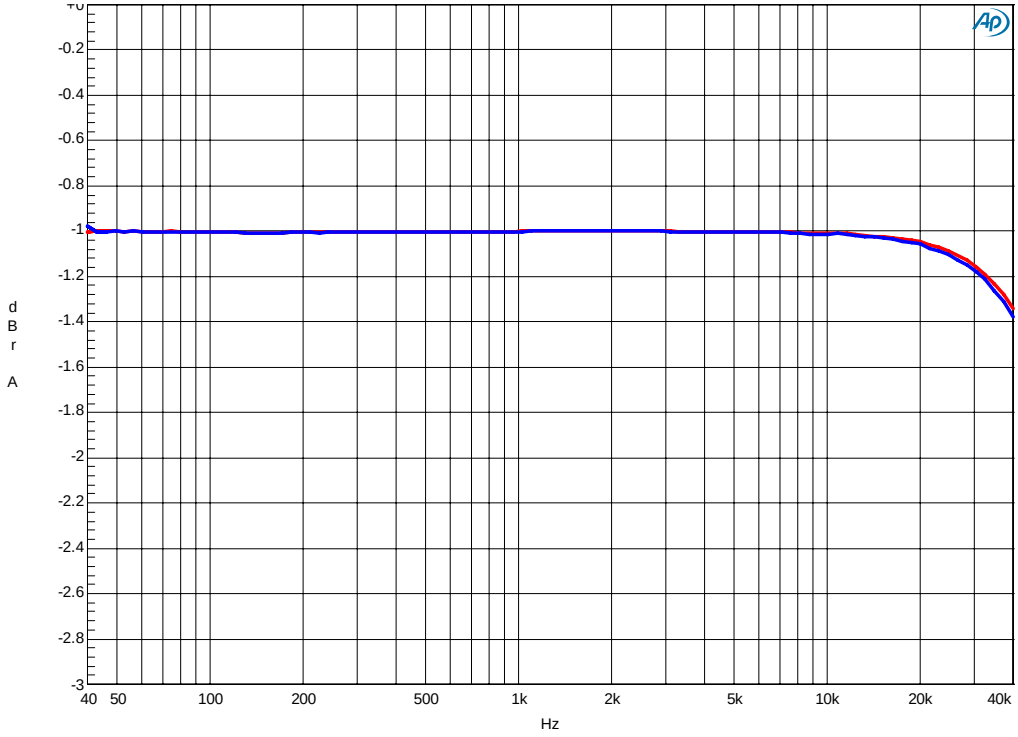


Figure 51. Frequency Response (Input level=-1dBFS)

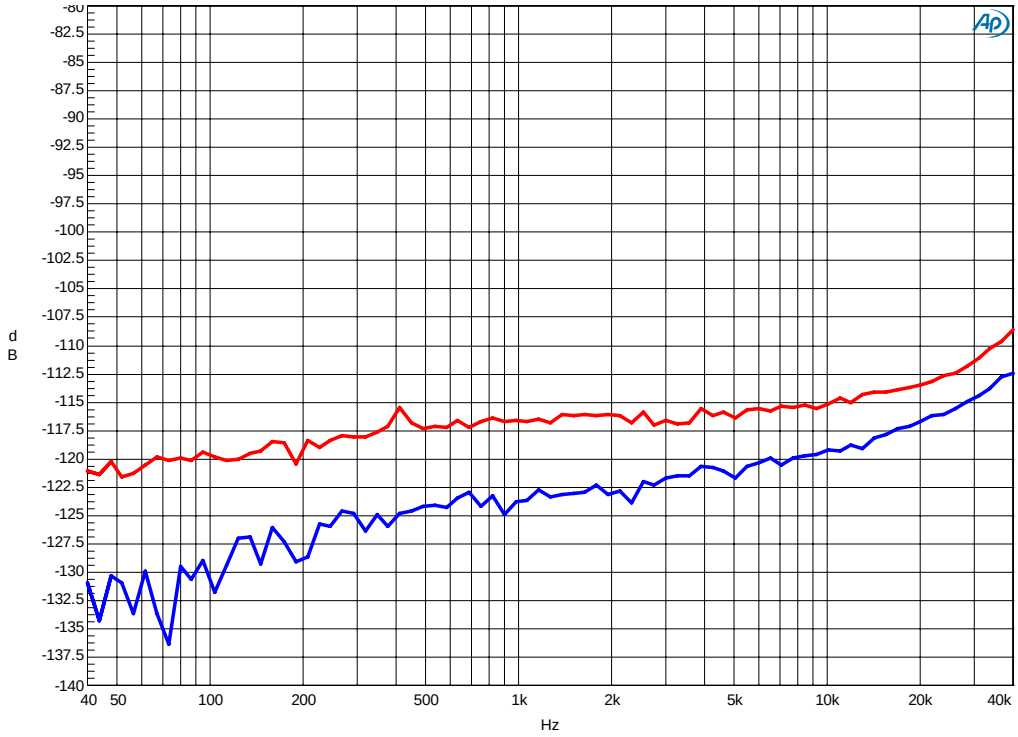


Figure 52. Crosstalk

3.6 DAC (fs=192kHz)

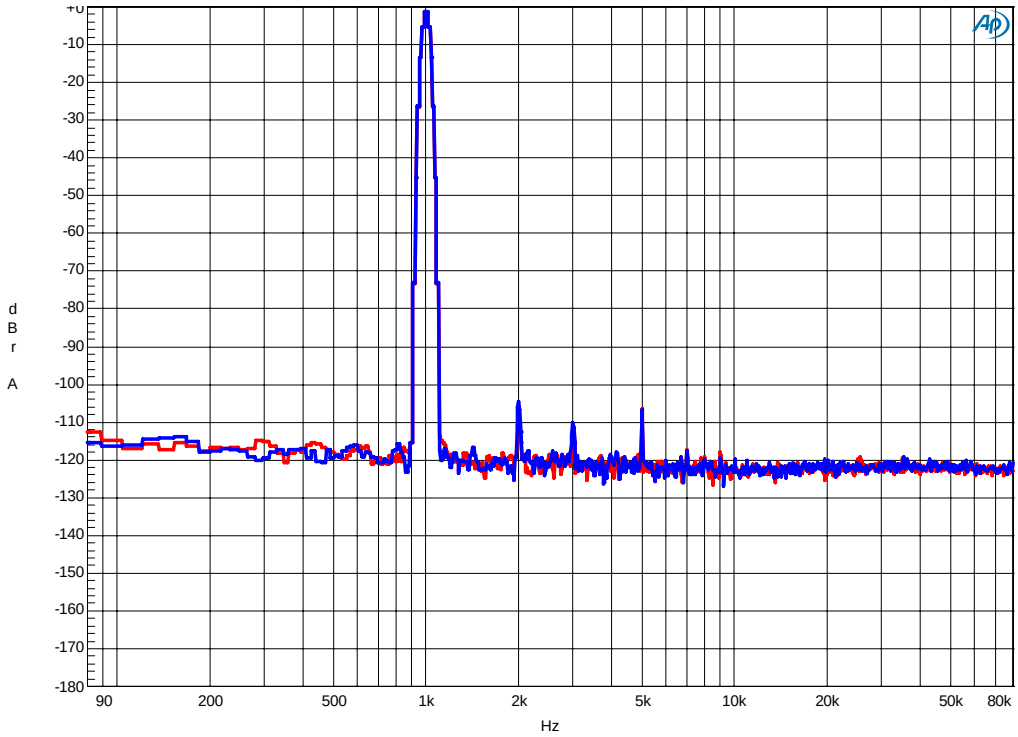


Figure 53. FFT (fin=1kHz, Input Level=-1dBFS)

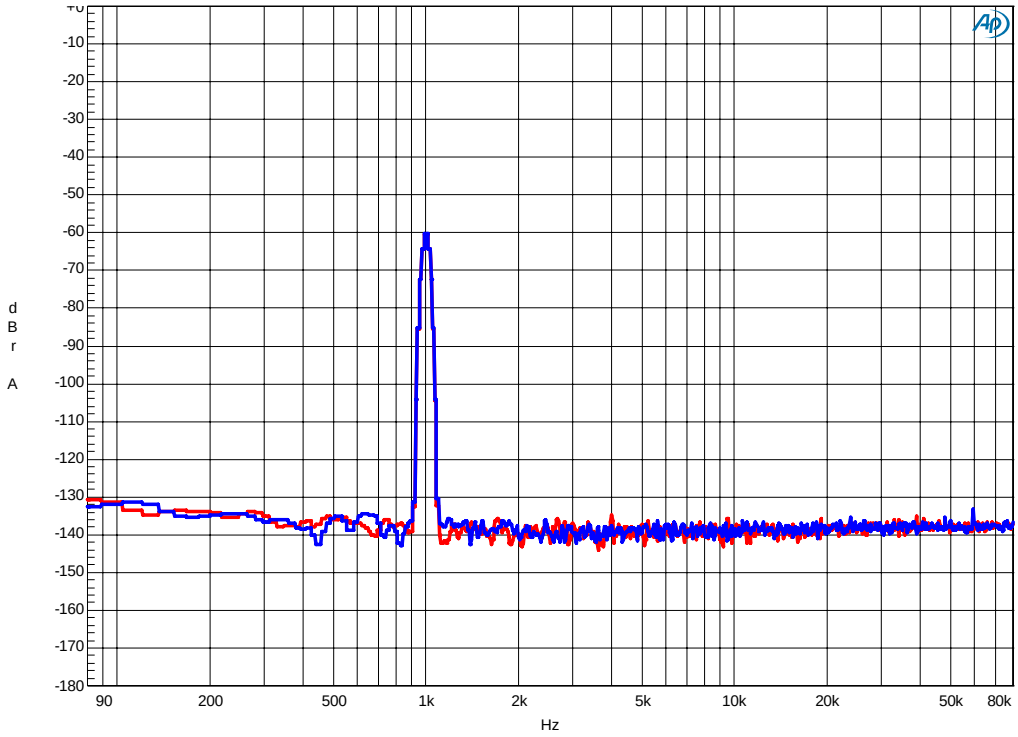


Figure 54. FFT (fin=1kHz, Input Level=-60dBFS)

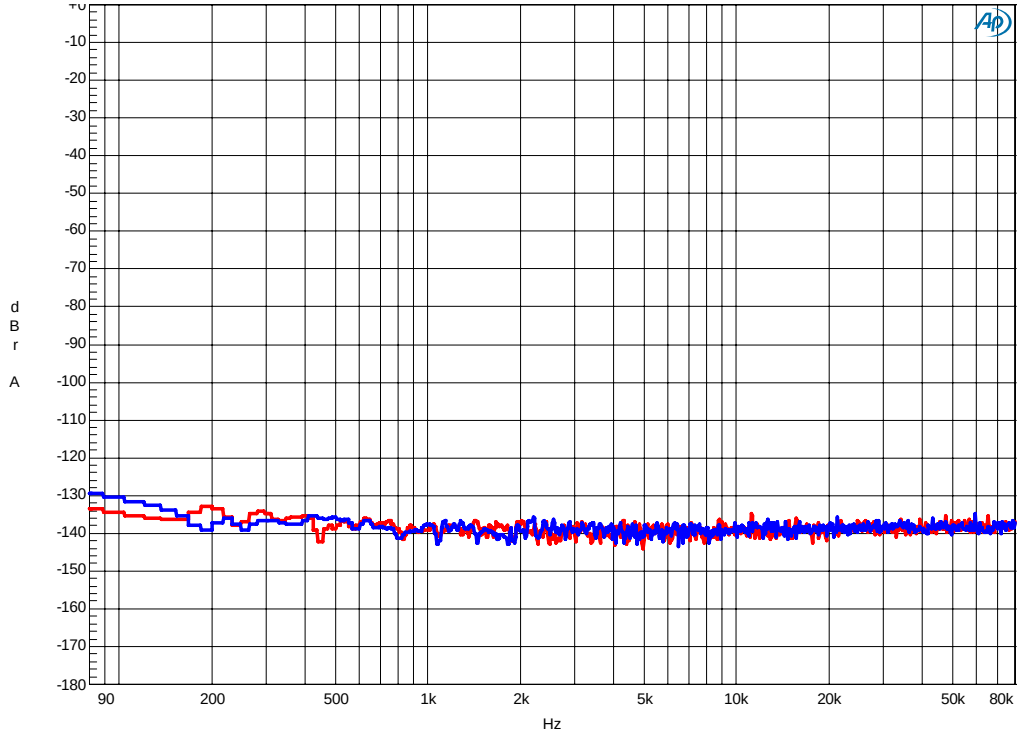


Figure 55. FFT (Noise Floor)

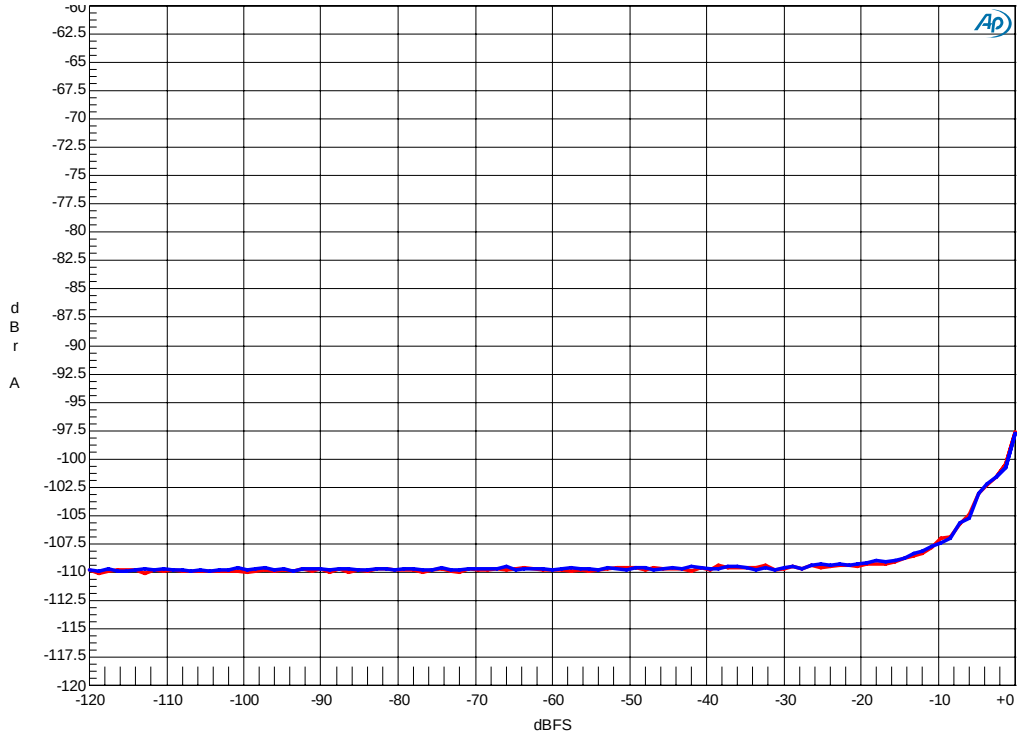


Figure 56. THD+N vs. Input level (fin=1kHz)

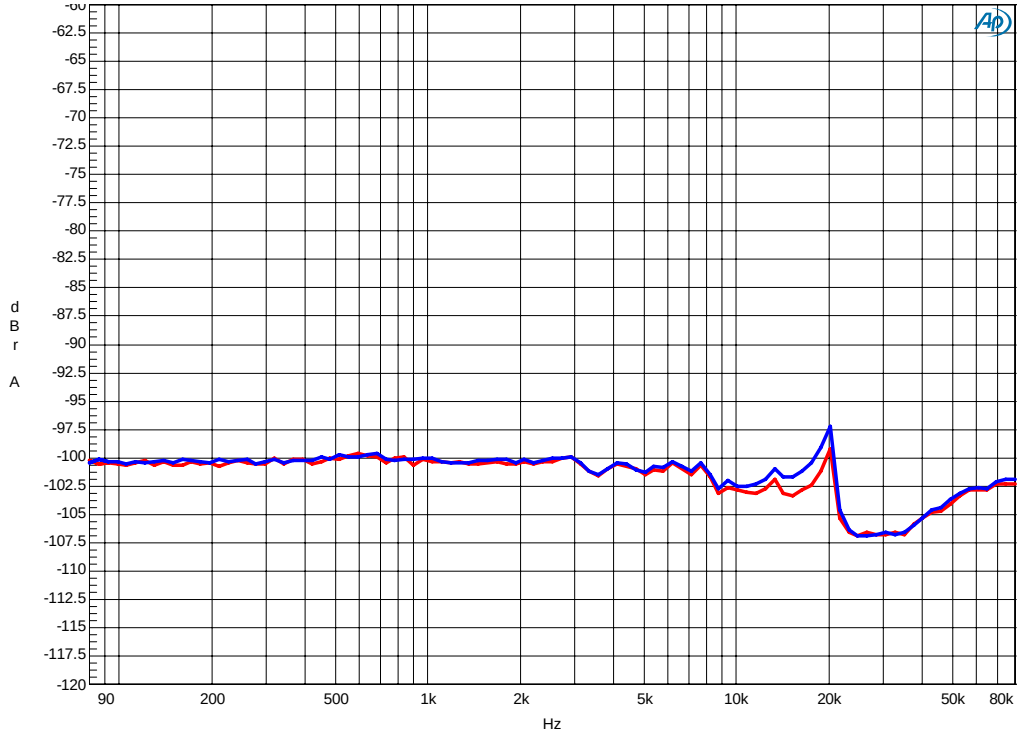


Figure 57. THD+N vs. Input Frequency (Input level=-1dBFS)

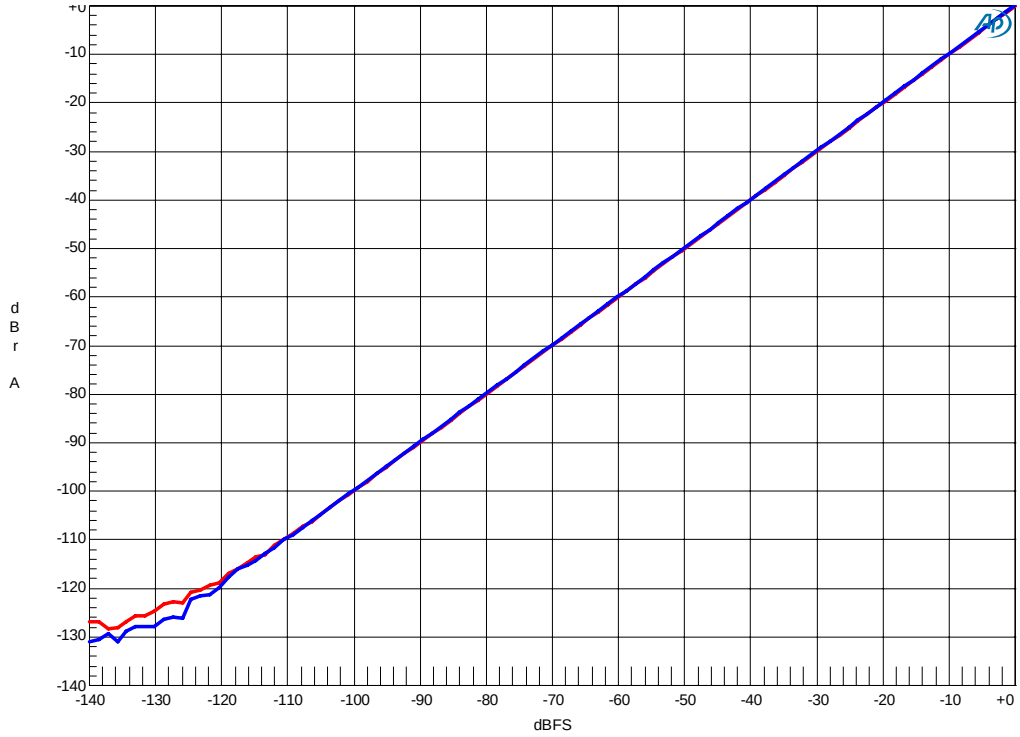


Figure 58. Linearity (fin=1kHz)

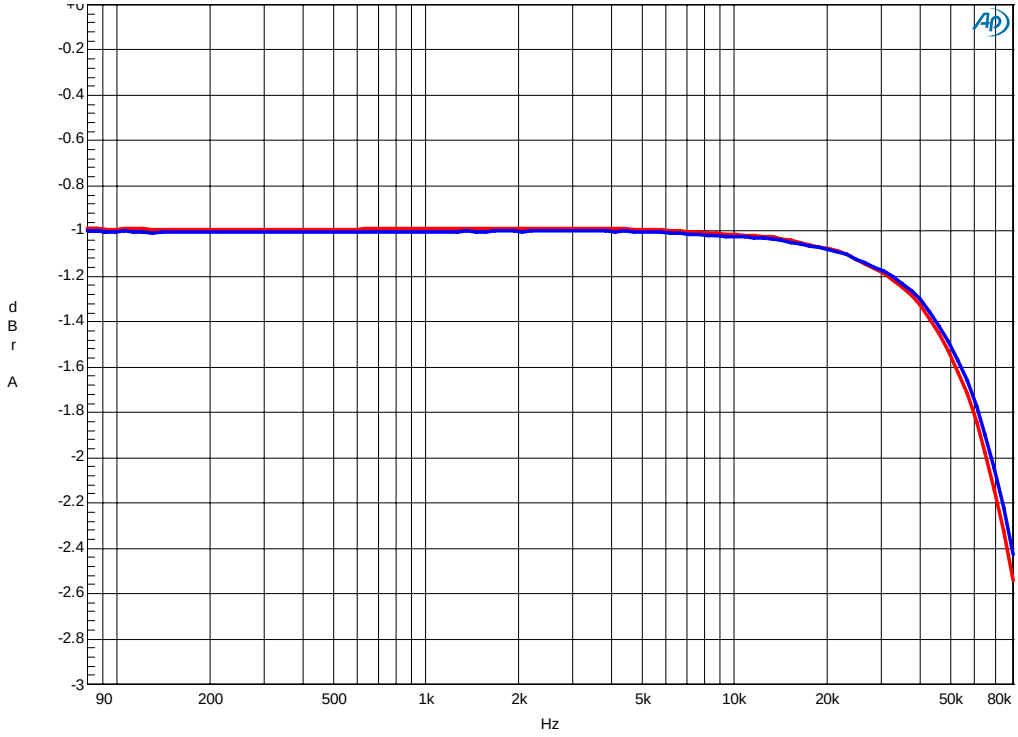


Figure 59. Frequency Response (Input level=-1dBFS)

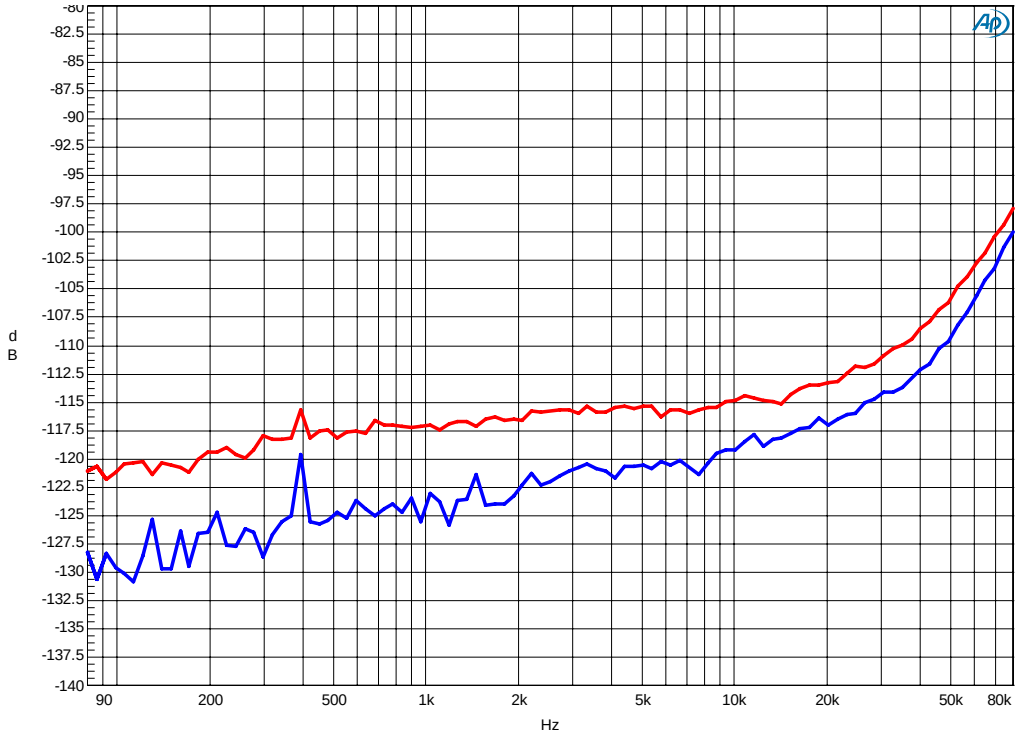
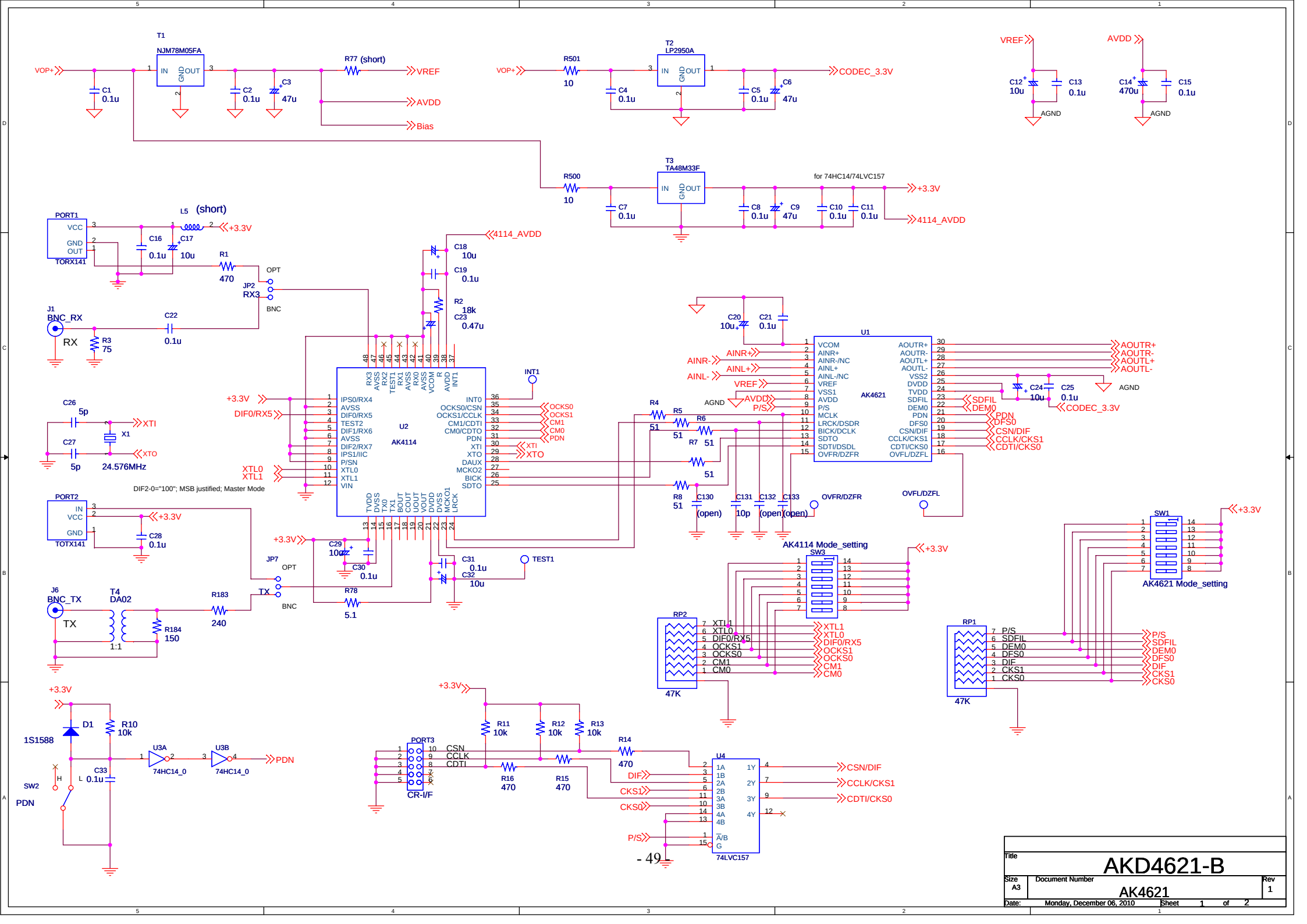


Figure 60. Crosstalk

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
2010/03/12	KM100800	0	First Edition		
2010/03/12	KM100801	1	Evaluation Board Change		Device Rev. Change AK4621: Rev.A → Rev.B
2010/12/07	KM100802	2	Modification	21~47	Device revision was changed.: Rev.B→Rev.C Update of measurement results and Plots.
			Modification	49	Circuit diagram was changed.


T1
NJM78M05FA
VOP+
C1 0.1u
C2 0.1u
C3 47u
R77 (short)
VREF
AVDD
Bias
T2
LP2950A
R501 10
C4 0.1u
C5 0.1u
C6 47u
CODEC_3.3V
VREF
AVDD
C12 10u
C13 0.1u
C14 470u
C15 0.1u
AGND
T3
TA48M33F
R500 10
C7 0.1u
C8 0.1u
C9 47u
C10 0.1u
C11 0.1u
for 74HC14/74LVC157
+3.3V
4114_AVDD
PORT1
TORX141
L5 (short)
C16 0.1u
C17 10u
R1 470
OPT
JP2
RX3
BNC
J1
BNC_RX
RX
R3 75
C22 0.1u
C18 10u
C19 0.1u
R2 18k
C23 0.47u
INT1
U2
AK4114
IPS0/RX4
AVSS
DIF0/RX5
TEST2
DIF1/RX6
AVSS
DIF2/RX7
IPS1/IIC
P/SN
XTL0
XTL1
VIN
INT0
OCKS0/CSN
OCKS1/CCLK
CM1/CDTI
CM0/CDTO
PDN
XTI
XTO
DAUX
MCKO2
BICK
SDTO
OCKS0
OCKS1
CM1
CM0
PDN
XTI
XTO
C26 5p
C27 5p
X1
24.576MHz
DIF2-0="100"; MSB justified; Master Mode
PORT2
TOTX141
C28 0.1u
C29 10u
C30 0.1u
C31 0.1u
C32 10u
TEST1
JP7
OPT
TX
BNC
R78 5.1
J6
BNC_TX
TX
T4
DA02
1:1
R183 240
R184 150
U1
AK4621
VCOM
AINR+
AINR-/NC
AINL+
AINL-/NC
VREF
VSS1
AVDD
P/S
MCLK
LRCK/DSDR
BICK/DCLK
SDTO
SDTI/DSDL
OVFR/DZFR
AOUTR+
AOUTR-
AOUTL+
AOUTL-
VSS2
DVDD
TVDD
SDFIL
DEM0
PDN
DFS0
CSN/DIF
CCLK/CKS1
CDTI/CKS0
OVFL/DZFL
C20 10u
C21 0.1u
C24 10u
C25 0.1u
AINR+
AINL+
AINR-
AINL-
VREF
AVDD
P/S
AGND
R4 51
R5 51
R6 51
R7 51
R8 51
C130 (open)
C131 10p
C132 (open)
C133 (open)
OVFR/DZFR
OVFL/DZFL
AK4114 Mode_setting
SW3
RP2
47K
XTL1
XTL0
DIF0/RX5
OCKS1
OCKS0
CM1
CM0
SW1
AK4621 Mode_setting
RP1
47K
P/S
SDFIL
DEM0
DFS0
DIF
CKS1
CKS0
D1
1S1588
R10 10k
U3A
U3B
74HC14_0
74HC14_0
PDN
SW2
C33 0.1u
PORT3
CR-I/F
CSN
CCLK
CDTI
R11 10k
R12 10k
R13 10k
R14 470
R16 470
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DIF
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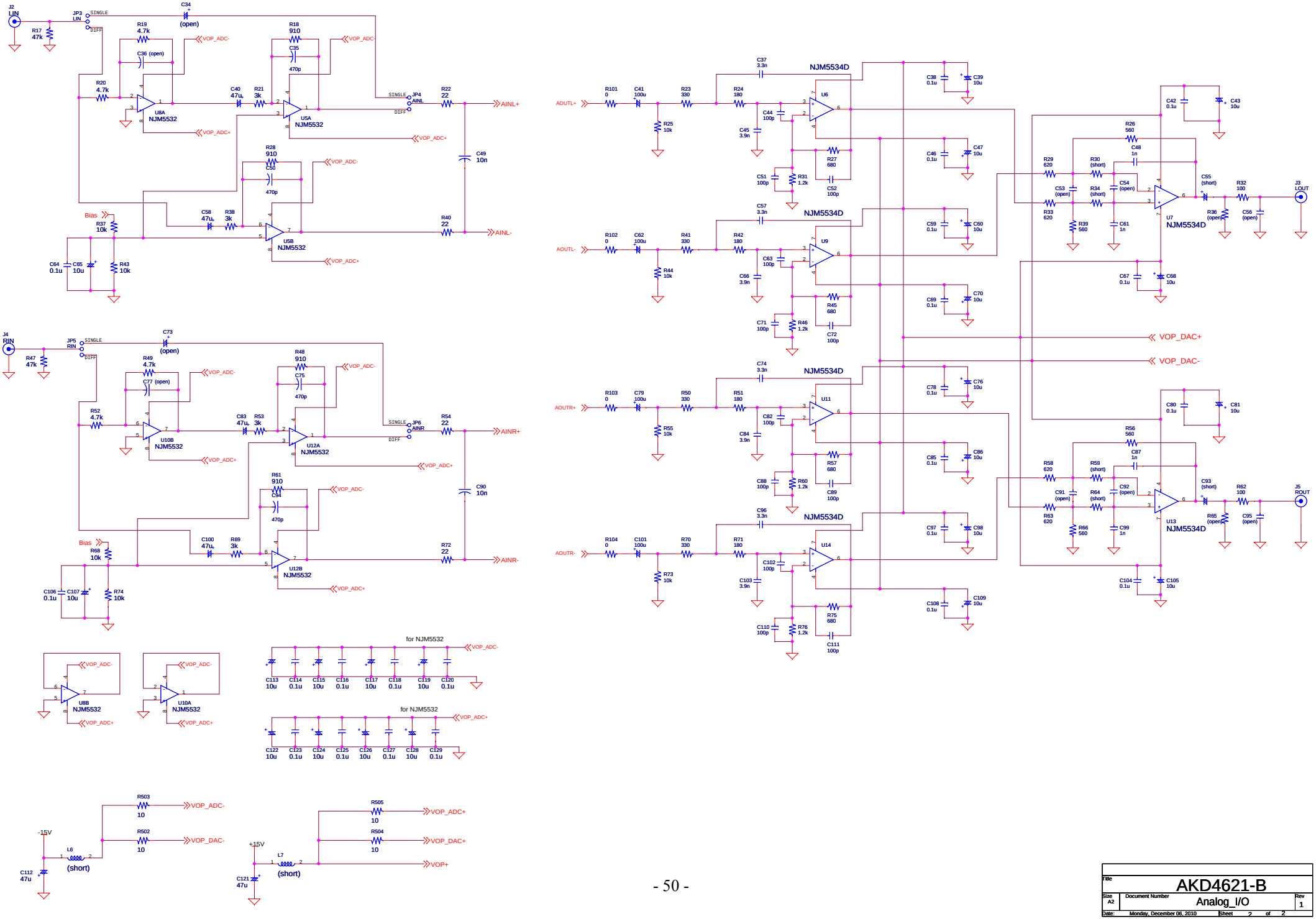

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