AKD4637-B
Evaluation board Rev.2 for AK4637

GENERAL DESCRIPTION

The AKD4637-B is an evaluation board for the AK4637 24bit CODEC with built-in PLL and MIC/SPK Amplifier. The AKD4637-B has the interface with AKM’s A/D evaluation boards. Therefore, it’s easy to evaluate the AK4637. The AKD4637-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

Ordering Guide
AKD4637-B --- Evaluation board for AK4637
(Control software is included in this package.)

FUNCTION

- Compatible with 2 types of interface
  - Direct interface with AKM’s A/D converter evaluation boards
  - DIT/DIR with optical input/output
- USB port for board control

Figure 1. AKD4637-B Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.
Operation Sequence

(1) Set up the power supply lines.

(1-1) In case of using the power supply connectors. <Default>

<table>
<thead>
<tr>
<th>JP13 AVDDSEL</th>
<th>JP11 USB5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>5V</td>
</tr>
</tbody>
</table>

(1-2) In case of supplying the power from regulator.

<table>
<thead>
<tr>
<th>JP13 AVDDSEL</th>
<th>JP11 USB5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>5V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name of Jack</th>
<th>Color</th>
<th>Default Setting</th>
<th>Using</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG1</td>
<td>red</td>
<td>5V</td>
<td>for regulator input</td>
</tr>
<tr>
<td>GND1</td>
<td>black</td>
<td>0V</td>
<td>ground</td>
</tr>
</tbody>
</table>

Table 1. Set up of power supply lines

(2) Set up the evaluation mode, jumper pins and DIP switch. (See the followings.)

(3) Power on.
   The control software must be opened after the power supplies are applied.
■ Evaluation mode

In case of using the AK4118A when evaluating the AK4637, audio interface format of both devices must be matched. Refer to the datasheet for audio interface format of the AK4637, and Table 2 for audio interface format of the AK4118A.

The AK4118A operates at fs of 32kHz or more. If the fs is slower than 32kHz, please use other mode. In addition, MCLK of AK4118A supports 256fs and 512fs. When evaluating in a condition except above, please use other mode.

Refer to the datasheet for register setting of the AK4637.

**Applicable Evaluation Mode**

1. A/D Evaluation using the AK4118A (DIT).
   1.1 Setting in External Slave Mode

2. D/A Evaluation using the AK4118A (DIR). <Default>
   2.1 Setting in External Slave Mode

3. Evaluation of A/D or D/A using the external clock.
   3.1 Setting in PLL Master Mode
   3.2 Setting in PLL Slave Mode
   3.3 Setting in External Slave Mode

4. Evaluation of Loop-back.
   4.1 Setting in PLL Master Mode
   4.2 Setting in PLL Slave Mode
   4.3 Setting in External Slave Mode
(1) A/D Evaluation using the AK4118A (DIT)

(1-1) Setting in External Slave Mode

X1 (X’tal: 12.288MHz) and PORT2 (DIT) are used. Do not connect anything to PORT1 (DIR). Registers of the AK4637 should be set to “EXT Slave Mode”. MCKI, BICK and FCK are supplied from the AK4118A, and SDTO of the AK4637 is output to the AK4118A.

The jumper pins should be set as follows.

- **JP5**: MCKI
  - EXT
  - DIR

- **JP6**: BICK
  - EXT
  - DIR

- **JP7**: FCK
  - EXT
  - DIR

- **JP8**: SDTO
  - EXT
  - DIR

(2) Evaluation of D/A using DIR of AK4118A. <Default>

(2-1) Setting in External Slave Mode

PORT1 (DIR) is used. Do not connect anything to PORT2 (DIT). Registers of the AK4637 should be set to “EXT Slave Mode”.

The jumper pins should be set as follows.

- **JP5**: MCKI
  - EXT
  - DIR

- **JP6**: BICK
  - EXT
  - DIR

- **JP7**: FCK
  - EXT
  - DIR

- **JP9**: SDTI
  - EXT
  - DIR

- **JP10**: SDTI-SEL
  - EXT
  - DIR
(3) A/D or D/A Evaluation using the external clock.

External clocks are used. Do not connect anything to PORT1 (DIR) and PORT2 (DIT).

(3-1) Setting in PLL Master Mode

The master clock is input from the MCKI pin of JP5. An internal PLL circuit generates BICK and FCK. Registers of the AK4637 should be set to “PLL Master Mode”.

MCKI and SDTI are input into JP5 and JP9. FCK, BICK and SDTO are output from JP7, JP6 and JP8.

![Figure 2. PLL Master Mode](image)

(3-2) Setting in PLL Slave Mode

A reference clock of PLL is selected among the input clocks that are supplied to the BICK pin. The required clock to operate the AK4637 is generated by an internal PLL circuit. Registers of the AK4637 should be set to “PLL Slave Mode” (Reference Clock = BICK).

BICK, FCK and SDTI are input into JP6, JP7 and JP9. SDTO is output from JP8.

![Figure 3. PLL Slave Mode 2(PLL Reference Clock: BICK pin)](image)

The jumper pins should be set as follows.

![JP5 MCKI](image)
(3-3) Setting in External Slave Mode

Registers of the AK4637 should be set to “EXT Slave Mode”.

MCLK, BICK, FCK and SDTI are input into JP5, JP6, JP7 and JP9. SDTO is output from JP8.

![Diagram of EXT Slave Mode](image-url)
(4) Evaluation in Loop-back Mode

(4-1) Setting in PLL Master Mode

Do not connect anything to PORT1 (DIR), PORT2 (DIT).
Registers of the AK4637 should be set to “PLL Master Mode”. MCLK should be supplied to JP5.

The jumper pins should be set as follows.

<table>
<thead>
<tr>
<th>JP8</th>
<th>JP9</th>
<th>JP10</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDTO</td>
<td>SDTI</td>
<td>SDTI-SEL</td>
</tr>
<tr>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
</tr>
</tbody>
</table>

ADC  | DIR

(4-2) Setting in PLL Slave Mode

Do not connect anything to PORT1 (DIR) and PORT2 (DIT).
Registers of the AK4637 should be set to “PLL Slave Mode” (Reference Clock: BICK).
BICK and FCK should be supplied to JP6 and JP7.

The jumper pins should be set as follows.

<table>
<thead>
<tr>
<th>JP5</th>
<th>JP8</th>
<th>JP9</th>
<th>JP10</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCKI</td>
<td>SDTO</td>
<td>SDTI</td>
<td>SDTI-SEL</td>
</tr>
<tr>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
</tr>
</tbody>
</table>

EXT  | DIR  | ADC  | DIR

(4-3) Setting in External Slave Mode

Do not connect anything to PORT1 (DIR), PORT2 (DIT).
Registers of the AK4637 should be set to “EXT Slave Mode”.
Use clocks from AK4118A. In case, use X1 (12.288MHz).

The jumper pins should be set as follows.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MCKI</td>
<td>BICK</td>
<td>FCK</td>
<td>SDTO</td>
<td>SDTI</td>
<td>SDTI-SEL</td>
</tr>
<tr>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
<td>◯ ◯ ◯</td>
</tr>
</tbody>
</table>

EXT  | DIR  | EXT  | DIR  | EXT  | DIR  | ADC  | DIR
### DIP Switch Setting

[S1] (SW DIP-4): Mode setting of the AK4118A.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>ON (&quot;H&quot;)</th>
<th>OFF (&quot;L&quot;)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OCKS1</td>
<td>AK4118A Master Clock Setting : See Table 4</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIF0</td>
<td></td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIF1</td>
<td>AK4118A Audio Format Setting</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DIF2</td>
<td>See Table 3</td>
<td>H</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2. Mode Setting of the AK4118A**

<table>
<thead>
<tr>
<th>Mode</th>
<th>DIF2</th>
<th>DIF1</th>
<th>DIF0</th>
<th>DAUX</th>
<th>SDTO</th>
<th>FCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>16bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>24bit, Left justified</td>
<td>18bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>20bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>24bit, FS</td>
<td>24bit, FS</td>
<td>L/H</td>
<td>O</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>I</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>24bit, FS</td>
<td>24bit, FS</td>
<td>L/H</td>
<td>I</td>
</tr>
</tbody>
</table>

**Table 3. AK4118A Audio Interface Format Setting**

<table>
<thead>
<tr>
<th>OCKS1</th>
<th>MCKO1</th>
<th>X’tal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>256fs</td>
<td>256fs</td>
</tr>
<tr>
<td>1</td>
<td>512fs</td>
<td>512fs</td>
</tr>
</tbody>
</table>

**Table 4. AK4118A Master Clock Setting**

### Tact SW Function

[SW1] (PDN): Resets AK4637 and AK4118A. When Tact switch is pushed, PDN is “L”.

### Control Port

It is possible to control AKD4637-B via general USB port. Connect cable with the USB connection (PORT3) on the board and PC.
Analog Input/Output Circuits

(1) Input Circuits

![Diagram of Analog Input/Output Circuits]

Figure 5. AIN, IN+/IN- Input Circuits

(1-1) AIN Input Circuit (Single-ended Input) <Default>

AIN is input to J1.
When the Mic Power is not used, JP2 should be set to open.

(1-2) IN+/IN- Input Circuit (Differential input)

IN+ and IN- are input to J1.
When the Mic Power is not used, JP2 and JP3 should be set to open.

(1-3) BEEP Input Circuit

BEEP is input to TP10.
Do not connect anything to J1.

(1-4) Digital Mic Input Circuit

DMCK is output from TP11 and DMDT is input to TP12.
Do not connect anything to J1.
(2) Output Circuits

Figure 6. AOUT, SPP/SPN Output Circuit

(2-1) SPP/SPN Output Circuit <Default>

SPP and SPN are output from TP3 and TP4.

JP4
AOUT

(2-2) Monaural Line Output Circuit

AOUT is output from J2.

JP4
AOUT

* AKM assumes no responsibility for the trouble when using the above circuit examples.
Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board and PC with a USB cable.
3. The USB control is recognized as HID (Human Interface Device) on the PC.
4. Double-click the icon “akd4637.exe” to open the control program. (Note 1)
   When the screen does not display “AKDUSBIF-B” at bottom left, reconnect the PC and the USB cable, and push the [Port Reset] button.
5. Begin evaluation by following the procedure below.

Note 1. The AK4637 should be reset by the SW1 after the power supplies are applied.
## Operation Overview

Function and Register map are controlled by this control software. These controls may be selected by the upper tabs.

Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window.

1. **[Port Reset]**: Resets the connection to PC. 
   Click this button when connecting USB cable after the control software set up.

2. **[Write Default]**: Register Initialization. 
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. **[All Write]**: Executes write commands for all registers displayed.

4. **[All Read]**: Executes read commands for all registers displayed.

5. **[Save]**: “Save Address of Register” dialog box pops up.

6. **[Load]**: Executes data write from a saved file.

7. **[All Reg Write]**: “All Reg Write” dialog box pops up.

8. **[Sequence]**: “Sequence” dialog box pops up.

9. **[Sequence (File)]**: “Sequence (File)” dialog box pops up.

10. **[Read]**: Reads current register settings and displays to the register area (on the right of the main window). 
    (Add: Address, R: AK4637 Read value, W: Last Write value (= Register Map))
    This is different from [All Read] button as it does not reflect to the register map. It only displays register values in hexadecimal numbers.
Tab Functions

(1) [Function] Tab: Function Control

Sequence operation and a setup of a register are executed with the function button arranged at the upper part, and each button in a block diagram.

Function block: Executes a sequential process shown on each button. (Refer to 1)-(1)-(1))
Path and Each Setting block: Executes a setup of the path or functions. (Refer to 1)-(1)-(2))

~ Explanation of the color of a pass line ~

Thick lines (blue, red, yellow, and sour orange) show that the paths are connected.

- thick line (blue): The path is connected and the power of block on this path is “OFF”.
- thick line (red): The path is connected and the power of block on this path is “ON”.
- thick line (yellow): The clock line is connected.
- thick line (sour orange): The clock line is connected and used.
(1-1) Function block

A function button executes the sequence process shown on the each button and updates several registers. These functions are mainly for path settings.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
<th>Input</th>
<th>Output</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog MIC (Recording_MIC+18dB(ALC ON))</td>
<td>MIC Input Recording</td>
<td>AMIC</td>
<td>SDTO</td>
<td>AMIC→ADC→Digi.Fil→SDTO</td>
</tr>
<tr>
<td>Digital MIC (Recording_DigitalMIC(ALC ON))</td>
<td>Digital MIC Input Recording</td>
<td>DMDAT/DMCLK</td>
<td>SDTO</td>
<td>DMDAT/DMCLK→Deci.Fil→Digi.Fil→SDTO</td>
</tr>
<tr>
<td>Speaker (Playback_Speaker+8.4dB(ALC ON))</td>
<td>Speaker Output</td>
<td>SDTI</td>
<td>SPP/SPN</td>
<td>SDTI→Digi.Fil→DAC→SPP/SPN</td>
</tr>
<tr>
<td>Line (Playback_Lineout)</td>
<td>Line Output</td>
<td>SDTI</td>
<td>AOUT</td>
<td>SDTI→DAC→AOUT</td>
</tr>
<tr>
<td>AMIC-Line (Loopback_MIC+18dB_LineOut(ALC ON))</td>
<td>Loopback (MIC Input, Line Output)</td>
<td>AMIC, AOUT</td>
<td></td>
<td>AMIC→ADC→Digi.Fil→DAC→AOUT</td>
</tr>
</tbody>
</table>

Table 5. Sequence Process Setting

※The Setting of Clock mode and I/F mode are not changed. The default values are follows.

I/F mode: 24bit MSB justified
(1-1-1) [Analog MIC (Recording_MIC+18dB(ALC ON))] Sequential process

When [Analog MIC] button in the main window is clicked, the sequence for MIC input Settings is executed.  
(Note 2)

Note 2. The function button makes some block power up, but [Power Down/Up] button is not changed.
(1-1-2) [Digital MIC (Recording_DigitalMIC(ALC ON))] Sequential process

When [Digital MIC] button in the main window is clicked, the sequence for Digital MIC input Settings is executed.

(Note 2)

Figure 11. [Digital MIC] Setting (After)
(1-1-3) [Speaker (Playback_Speaker+8.4dB(ALC ON))] Sequential process

When [Speaker] button in the main window is clicked, the sequence for Speaker output Settings is executed. (Note 2)

Figure 12. [Speaker] Setting (After)
(1-1-4) [Lineout (Playback_Lineout)] Sequential process

When [Lineout] button in the main window is clicked, the sequence for Line output Settings is executed. (Note 2)

Figure 13. [Line out] Setting (After)
(1-1-5) [AMIC-Line (Loopback_MIC+18dB_LineOut(ALC ON))] Sequential process

When [AMIC-Line] button in the main window is clicked, the sequence of Loopback settings is executed. (Note 2)

Figure 14. [AMIC-Line] Setting (After)
(1-2) Path and Various Setting Block

The enabled paths are shown. The FS and CM bits, etc… can be set up. [Input_ADC Setting], [Digital Filter Setting], [ALC Setting], [DAC_Output Setting], [BEEP Setting] -- each setting dialog can be opened.

- [Input_ADC Setting] button: Opens “Input_ADC” dialog box.
- [Digital Filter Setting] button: Opens “Filter Setting” dialog box.
- [ALC Setting] Button: Opens “ALC Setting” dialog box.
- [DAC_Output Setting] button: Opens “DAC_Output Setting” dialog box. This dialog also has a setup of Speaker amplifier and lineout amplifier.
- [BEEP Setting] button: Opens “BEEP Setting” dialog box.
- BEEP Power [OFF/ON] button: The path of a BEEP output is controlled and performs a BEEPS output “OFF/ON.” (Note 3)
- BEEPS bit switch: [ON]: BEEPS is set “1” and BEEPS bit Switch is connected.
- DACS/L bit switch: This switch is interlocked with BEEPS bit. This switch is interlocked with DACS bit and DACL bit. (Note 4)
- [Power Down/Up] button: Using the present path setting, the path for recording is set and ON/OFF of PMx bit is changed. (Note 3)

Note 3. There are some register bits which are set up automatically at Power Up/Down. (Refer to the next page.)

Note 4. The DACS (or DACL) switch on a GUI screen is updated by selection situation of a speaker/lineout. When "LOSEL=0 and DACS=1" or "LOSEL=1 and DACL=1", the switch "is connected". Other case, the switch "is disconnected".
### BEEP Power: [OFF/ON] Button

<table>
<thead>
<tr>
<th>Register bit</th>
<th>Setup value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ON</strong></td>
<td></td>
</tr>
<tr>
<td>PMVCM</td>
<td>“1” (Note 5)</td>
</tr>
<tr>
<td>BEEPS, PMBP</td>
<td>“1”</td>
</tr>
<tr>
<td>PMSL, SLPSN</td>
<td>“1” (Note 6)</td>
</tr>
<tr>
<td><strong>OFF</strong></td>
<td></td>
</tr>
<tr>
<td>PMSL, SLPSN</td>
<td>“0” (Note 6)</td>
</tr>
<tr>
<td>PMBP</td>
<td>“0”</td>
</tr>
</tbody>
</table>

### Recording: [Power Down/Up] Button

<table>
<thead>
<tr>
<th>Register bit</th>
<th>Setup value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Up</strong></td>
<td></td>
</tr>
<tr>
<td>PMVCM</td>
<td>“1” (Note 5)</td>
</tr>
<tr>
<td>PMPFIL</td>
<td>When PFSDO bit = 1, PMPFIL bit = 1</td>
</tr>
</tbody>
</table>
| PMADC (or PMDM) | -When DMIC bit = 0, PMADC bit = 1  
|               | -When DMIC bit = 1, PMDM bit = 1  |
| **Power Down** |             |
| PMADC, PMDM  | “0”         |
| PMPFIL       | “0” (Note 7) |

### Playback: [Power Down/Up] Button

<table>
<thead>
<tr>
<th>Register bit</th>
<th>Setup value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Up</strong></td>
<td></td>
</tr>
<tr>
<td>PMVCM</td>
<td>“1” (Note 5)</td>
</tr>
</tbody>
</table>
| DACS (or DACL) | -When LOSEL bit = 0, DACS bit = 1  
|               | -When LOSEL bit = 1, DACL bit = 1  |
| PMPFIL       | When PFDAC1-0 bits = 1 or 2, PMPFIL bit = 1 |
| PMDAC        | “1”         |
| PMSL, SLPSN  | “1” (Note 8) |
| **Power Down** |             |
| PMSL, SLPSN  | “0” (Note 8) |
| PMDAC        | “0”         |
| PMPFIL       | “0” (Note 7) |

**Note 5.** Once PMVCM bit is set to “1”, PMVCM is not set to “0” in this Function Tab.

**Note 6.** These bits keep “1” when Playback is “Power Up”.

**Note 7.** PMPFIL keep “1” when this is used by Playback or Recording.

**Note 8.** These bits keep “1” when BEEP Power is “ON”.
(2) [REG] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch. The register is updated by mouse operation. Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red). Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray).

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

![Figure 16. [REG] Window](image)
(2-1) [Write]: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When the checkbox next to the bit name is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”.

Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

![Figure 17. [Register Set] Window](image)

(2-2) [Read]: Data Read

Click the [Read] button located on the right of the each corresponding address to execute a register read. The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.

Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red). Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray).
Dialog Box

(1) [Save]: [Save Address of Register] Dialog Box

Click the [Save] button in the main window for save address setting dialog box.

![Save Address of Register Dialog Box]

- **[All Address] check box**: When the [All Address] checkbox is checked, all register settings will be saved.
- **[Start Address] edit box**: When the [All Address] check box is not checked, set starts register address to save.
- **[End Address] edit box**: When the [All Address] check box is not checked, set end register address to save.
- **[OK] button**: Selects a file to save and saves register settings.
- **[Cancel] button**: Cancel and finish this process.
(2) [All Reg Write]: [All Register Write] Dialog Box

Click the [All Reg Write] button in the main window to open register setting file window show below. Register setting files saved by the [Save] button may be applied.

![Figure 19. [All Reg Write] Window](image)

- **[Open (left)] button**: Selects a register setting file (*.akr).
- **[Write] button**: Executes register write with selected file setting.
- **[Help] button**: Opens a help window.
- **[Save] button**: Saves a register setting file assignment. File name is “*.mar”.
- **[Open (right)] button**: Opens a saved register setting file assignment “*.mar”.
- **[Close] button**: Closes the dialog box and finish the process.
- **[All Write] flame**: Executes all register write. Selected files are executed in descending order.
- **[Start] button**: Start the register writing.
- **[Stop] button**: Stop the register writing.
- **[Interval time] edit box**: Set interval time to start next register setting file. (5msec ~ 10,000msec)
- **[Current No] edit box**: The file number which is being processed is displayed. (File number is assigned 1-10 from top to bottom.)

~ Operating Suggestions ~

1. Files saved by the [Save] button and opened by the [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. Then register settings are changed by the [Save] button in the main window, re-read the file to reflect new register settings.
(3) [Sequence]: [Sequence] Dialog Box

Click the [Sequence] button in the main window to open register sequence setting dialog box. Register sequence can be set in this dialog box.

Figure 20. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

   Use [Select] pull-down box to choose commands. Corresponding boxes will be valid.

   < Select items >
   - No use : Not using this address
   - Register : Register write
   - Reg_Mask : Register write (Masked)
   - Interval : Takes an interval
   - Stop : Pauses the sequence
   - End : Ends the sequence
2. Input sequence

[Address] : Data address
[Data] : Write data
[Mask] : Mask

This value “ANDed” with the write data becomes the input data. The bits which corresponding Mask bit = “0” are not changed. At this time, data read is not executed, and the storage data of this software is used.

“Write Default” must be executed after power up the AK4958 or when the AK4958 is reset by the PDN pin since the storage data and register values are different.

This is the actual write data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[Interval] : Interval time

Valid boxes for each process command are shown below.
* No use : None
* Register : [ Address ], [ Data ], [ Interval ]
* Reg_Mask : [ Address ], [ Data ], [ Mask ], [ Interval ]
* Interval : [ Interval ]
* Stop : None
* End : None

~ Control Buttons ~

Functions of Control Button are shown below.

[DEL] button : Checked step is deleted.
[INS] button : The last deleted step is inserted to checked step.
[Start Step] select: Select start step.
　No.1 Step : Start from No.1 step.
　Checked Step : Start from checked step.
[Start] button : Executes the sequence.
[Stop] button : Stops the sequence.
[Help] button : Opens a help window.
[Save] button : Saves sequence settings as a file. The file name is “*.aks”.
[Open] button : Opens a sequence setting file “*.aks”.
[Close] button : Closes the dialog box and finishes the process.

~ Stop of the Sequence ~

When “Stop” is selected in the sequence, the process is paused at this step and restart step number is checked. It starts again from the checked step by clicking the [Start] button. When the process at the end of sequence is finished, “Step No.1” of [start step] is selected automatically.
(4) [Sequence (File)]: [Sequence by *.aks file] Dialog Box

Click the [Sequence (File)] button to open sequence setting file dialog box shown below. Files saved in the “Sequence setting dialog” can be applied in this dialog.

![Sequence by *.aks file](image)

Figure 21. [Sequence (File)] Window

- **[Open (left)] button**: Opens a sequence setting file (*.aks).
- **[Start] button**: Executes the sequence by the setting of selected file.
- **[Start All] button**: Executes all sequence settings. Selected files are executed in descending order.
- **[Stop] button**: Stops the sequence process.
- **[Help] button**: Opens a help window.
- **[Save] button**: Saves a sequence setting file assignment. The file name is “*.mas”.
- **[Open (right)] button**: Opens a saved sequence setting file assignment “*.mas”.
- **[Close] button**: Closes the dialog box and finishes the process.

~ Operating Suggestions ~

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” is selected in the sequence, the process will be paused and a pop-up message will appear. Click “OK” to continue the process.

![Sequence Pause](image)

Figure 22. [Sequence Pause] Window
(5) [Input_ADC Setting]: [Input_ADC Setting] Dialog Box

Click the [Input_ADC Setting] button in the main window to open MIC and ADC setting dialog. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![Input_ADC Setting Dialog Box](image)

Figure 23. [Audio I/F] Window

~ Gain Control by Slider ~

The volume can also be changed by slider. When a value is input in the edit box, the slider is moved to the value that selected by the edit box. Use the mouse or arrow keys on the keyboard for fine tuning.

![Slider Operation](image)

Figure 24. Slider operation
(6) [Digital Filter Setting]: [Filter Setting] Dialog Box

Click the [Digital Filter] button in the main window to open digital filter setting dialog. Coefficient and frequency of digital filter are calculated on this dialog. (Refer to the datasheet for register definitions.)

![Digital Filter Setting: Filter Setting Dialog Box](image)

**Figure 25. [Filter Setting] Window**

- **[Register Setting] button**: Opens the register setting dialog. Register writes of a filter factor are also executed.
- **[F Response] button**: Opens the frequency response plot dialog [Filter Plot]. Register writes of a filter factor are also executed.
- **[Write] button**: Calculation of all the filters and coefficient writing are executed.
- **[Example Setting] button**: The example parameters are set in dialog and the filter coefficients are written.
- **EQ Sequence for Noise [ON/OFF] button**: ON: EQCx bit, EQxT bits and EQxG bits are set for noise processing. OFF: The bits will return to the state of before the button is set to ON.
- **[Notch ON/OFF] button**: ON: The gain is fixed to “-1.0” in order to use as Notch filter. OFF: Gain is set to “1.0” when this is changed to “OFF”.
- **[Close] button**: Closes the dialog box and finishes the process.
(6-1) Parameter Setting

“HPF1 Enable”, “HPF2 Enable”, “LPF Enable”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5”
Please set ON/OFF of Filter with a check button.
When checked it, Filter becomes ON. When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed.

Please set a parameter of each Filter (Note 9)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Detail</th>
<th>Setting Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>Sampling Frequency (fs)</td>
<td>8, 11.025, 12, 16, 22.05, 24, 32, 44.1 or 48kHz</td>
</tr>
<tr>
<td><strong>HPF</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HPF1 Cut Off Frequency</td>
<td>High Pass Filter 1 cut off frequency</td>
<td>3.7×fs/48 ~ 236.8×fs/48 (kHz)</td>
</tr>
<tr>
<td>HPF2 Cut Off Frequency</td>
<td>High Pass Filter 2 cut off frequency</td>
<td>0.0001 ≤ fc/fs &lt; 0.497</td>
</tr>
<tr>
<td><strong>LPF</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cut Off Frequency</td>
<td>Low Pass Filter cut off frequency</td>
<td>0.05 ≤ fc/fs &lt; 0.497</td>
</tr>
<tr>
<td><strong>5 Band Equalizer</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EQ1-5 Center Frequency</td>
<td>EQ1-5 Center frequency</td>
<td>0.003 &lt; fo/fs &lt; 0.497</td>
</tr>
<tr>
<td>EQ1-5 Band Width</td>
<td>EQ1-5 Band width (Note 10)</td>
<td>fo/fs &lt; 0.497</td>
</tr>
<tr>
<td>EQ1-5 Gain</td>
<td>EQ1-5 Gain (Note 11)</td>
<td>-1 ≤ Gain &lt; 3</td>
</tr>
</tbody>
</table>

Table 6. Parameter Setting of [Filter Setting]

Note 9. When the value smaller than a setting range is set, the minimum value of setting range is set.
When the value bigger than a setting range is set, the maximum value of setting range is set.
When set error value to the filter of “OFF”, an error message is not displayed.

Note 10. A gain difference is a bandwidth of 3dB from center frequency.
Note 11. When a gain is “-1”, EQ becomes a notch filter.
(6-2) **[Register Setting]: [Register Setting for Filter] Dialog Box**

Click the [Register Setting] button, a register set value is displayed.

![Figure 27. [Register Setting for Filter] Window](image)

Followings are the cases when a register set value is updated.
1. When [Register Setting] button was pushed.
2. When [F Response] button was pushed.
3. When [Write] button was pushed.
4. When [UpDate] button was pushed on a frequency characteristic indication window.
5. When Enter or the Tab key is pressed after setting each parameter.
(6-3) [F Response]: [Filter Plot] Dialog Box

The frequency response of digital filter is displayed when push a [F Response] button. Then, the register setting for digital filter are also updated. Change Frequency Range, and indication of a frequency characteristic is updated when push a [UpDate] button.

![Filter Plot Dialog Box](image)

Figure 28. [F Response] Window

[Frequency Range] edit box: The width of the frequency display is specified.
[UpDate] button: It draws in the graph again.
[Log View] check button: Switch of “Linear/Log” display.
[Mouse Control of Left Button] radio button: The item (fo, Gain) which can be adjusted with a mouse can be chosen. (at using EQx) (Note 12)

fo: Center frequency can be adjusted.
Gain: Gain can be adjusted.
fo and Gain: Center frequency and Gain can be adjusted.

[Close] button: Closing the dialog box and finish the process.

Note 12. EQx of “Notch ON” is able to adjust only “fo”.

~ Adjustment of vertical range ~

2. [Vertical slider]: Movement of vertical display.
3. [Horizontal slider]: Adjustment of the horizontal display.
   (The left side reduces, and the right side expands.)
(6-4) 5-BandEQ operation on Filter Plot screen

When EQ (1~5) is turning “ON”, a green number is displayed on the Filter Plot dialog box. This number shows the setting of the center frequency and the gain of each EQ. (The horizontal coordinates of a number is the center frequency of EQ, and the vertical ordinate is a gain of EQ (-1 ～ 2.99).)

The number under the display is operated with the mouse, and it is possible to set the filter characteristic on this screen. The center frequency and the gain setting are changed by moving the mouse while left-clicking. (Note 12)

The setting of the bandwidth is changed by moving the mouse while right-clicking.

Figure 29. Filter Setting (Left-clicking operation)

Figure 30. Filter Setting (Right-clicking operation)
(6-5) About “Notch Auto Correct”

If the gain of 5-Band EQ is set to “-1”, Equalizer becomes a notch filter.
When the center frequency of two or more notch filters is adjacent, the gap is generated in the center frequency.
(Figure 31) When “Notch Auto Correct” button is checked, the center frequency of the notch filter is automatically corrected. The gain setting of the automatic correction function is effective and only EQ of “-1” is effective.
(Figure 32)
This automatic compensation is effective to EQ which set the gain as “-1”. (Note 12, Note 13, Note 14)

Note 13. There is a possibility that the automatic compensation is not correctly done when the width of the center frequency is smaller than that of the bandwidth setting.
Note 14. Gain is fixed to “-1.0” by [Notch OFF/ON] button “ON”.

Gain is fixed to “-1.0” by [Notch OFF/ON] button “ON.”

Figure 31. 5Band Equalizer Operation (Not Check of “Notch Auto Correct”)

Figure 32. 5Band Equalizer Operation (Checked of “Notch Auto Correct”)
(6-6) Common Gain Sequence for Noise

If “EQ Sequence for Noise (ON/OFF)” button is pushed, setup bits about EQ2-5 shown below are changed. When the button pushed to OFF, each setup is returned to the state of before pushing a button. Please use the button when it expected that a noise continues.

Figure 33. Equalizer Gain Setting

Button ON : EQCx bit: OFF, EQxG5-0 bits: 0x3F (-0.03dB), EQxT1-0 bits: 00 (256/fs)
Figure 34. Equalizer Gain Setting (Setting for Noise button is “ON”)

Button OFF : the state of before pushing a button.
Figure 35. Equalizer Gain Setting (Setting for Noise button is “OFF”)
(7) [ALC Setting]: [ALC Setting] Dialog Box

Click the [ALC Setting] button in the main window to open ALC setting dialog. ALC parameters are controlled in this dialog. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![Figure 36. [ALC Setting] Window](image)

~ Volume Read ~

When the [Start] button on the bottom right of the dialog is clicked, reading “VOL” register is executed periodically. This interval time is set by the edit box beside the button. This reading continues until the stop button is pushed.

![Figure 37. Volume Progress Control](image)
(8) [DAC_Output Setting]: [DAC_Output Setting] Dialog Box

Click the [DAC Setting] button in the main window to open DAC setting dialog. Output mode, DAC and output gain setting are available. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

Figure 38. [DAC_Output Setting] Window
(9) [BEEP Setting] Dialog Box

Click the [BEEP Setting] button in the main window to open BEEP setting dialog. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![BEEP Setting Dialog Box](image)

Figure 39. [BEEP Setting] Window
### 測定結果

#### 测定条件
- Measurement unit: Audio Precision, System two Cascade
- MCKI: 256fs (12.288MHz)
- BICK: 64fs
- fs: 48kHz
- Bit: 24bit
- Measurement Mode: EXT Slave Mode
- Power Supply: AVDD = TVDD = 3.3V, DVDD = 1.8V
- Input Frequency: 1kHz
- Measurement Frequency: 20 ~ 20kHz
- Temperature: Room

#### 測定結果

1. **ADC**

<table>
<thead>
<tr>
<th>ADC: AIN → ADC → SDTO, IVOL=0dB, ALC=OFF</th>
<th>Result (dB)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGAIN = +18dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>82.5</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>88.1</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>88.1</td>
<td>dB</td>
</tr>
<tr>
<td>MGAIN = 0dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>84.3</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>94.9</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>95.0</td>
<td>dB</td>
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</table>

2. **DAC**

<table>
<thead>
<tr>
<th>Speaker-Amp: DAC → SPP/SPN, IVOL=DVOL=0dB, SPKG=+8.45dB, RL=8Ω</th>
<th>Result (dB)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGAIN = +18dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>80.0</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>85.7</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>85.7</td>
<td>dB</td>
</tr>
<tr>
<td>MGAIN = 0dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>83.0</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>93.2</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>93.1</td>
<td>dB</td>
</tr>
</tbody>
</table>

Stereo Line Output: DAC → AOUT, IVOL=DVOL=0dB, RL=22kΩ

LVCM1-0 bits = “01”, fs=48kHz, BW=20kHz

<table>
<thead>
<tr>
<th>S/(N+D) (0dBFS)</th>
<th>81.6</th>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/N (A-weighted)</td>
<td>94.3</td>
<td>dB</td>
</tr>
<tr>
<td>S/(N+D) (-3dBFS)</td>
<td>86.0</td>
<td>dB</td>
</tr>
</tbody>
</table>
[Plot]

1. ADC (AIn → ADC) (Single-ended Input)
   [MGAIN=+18dB]

Figure 40. FFT (Input level = -1dBFS)

Figure 41. FFT (Input level = -60dBFS)
AK4637 ADC FFT (No signal)

Figure 42. FFT (No signal)

AK4637 ADC THD+N vs Input Level (fin=1kHz)

Figure 43. THD+N vs Input Level
AK4637 ADC THD+N vs Input Frequency (-1dBFS)

Figure 44. THD+N vs Input Frequency

AK4637 ADC Linearity (fin=1kHz)

Figure 45. Linearity
Figure 46. Frequency Response
Figure 47. FFT (Input level = -1dBFS)

Figure 48. FFT (Input level = -60dBFS)
AK4637 ADC FFT (No signal)

Figure 49. FFT (No signal)

AK4637 ADC THD+N vs Input Level (fin=1kHz)

Figure 50. THD+N vs Input Level
AK4637 ADC THD+N vs Input Frequency (-1dBFS)

Figure 51. THD+N vs Input Frequency

AK4637 ADC Linearity (fin=1kHz)

Figure 52. Linearity
AK4637 ADC Frequency Response (-1dBFS)

Figure 53. Frequency Response
2. ADC (IN+/IN- → ADC) (Differential Input)
[MGAIN=±18dB]

Figure 54. FFT (Input level = -1dBFS)

Figure 55. FFT (Input level = -60dBFS)
AK4637 ADC FFT (No signal)

Figure 56. FFT (No signal)

AK4637 ADC THD+N vs Input Level (fin=1kHz)

Figure 57. THD+N vs Input level
AK4637 ADC THD+N vs Input Frequency (-1dBFS)

Figure 58. THD+N vs Input Frequency (C8 and C9: Ceramic Capacitor)

AK4637 ADC Linearity (fin=1kHz)

Figure 59. Linearity
Figure 60. Frequency Response
AK4637 ADC FFT (-1dBFS)

Figure 61. FFT (Input level = -1dBFS)

AK4637 ADC FFT (-60dBFS)

Figure 62. FFT (Input level = -60dBFS)
AK4637 ADC FFT (No signal)

Figure 63. FFT (No signal)

AK4637 ADC THD+N vs Input Level (fin=1kHz)

Figure 64. THD+N vs Input Level
Figure 65. THD+N vs Input Frequency

Figure 66. Linearity
AK4637 ADC Frequency Response (-1dBFS)

Figure 67. Frequency Response
3. DAC (DAC → Speaker (SPP/SPN))

AK4637 DAC=>SPK FFT (-0.5dBFS; SPKG=01)

Figure 68. FFT (Input level = -0.5dBFS)

AK4637 DAC=>SPK FFT (-60dBFS; SPKG=01)

Figure 69. FFT (Input level = -60dBFS)
AK4637 DAC=>SPK FFT (No signal; SPKG=01)

Figure 70. FFT (No signal)

AK4637 DAC=>SPK Out of band noise (SPKG=01)

Figure 71. FFT (Out-of-band Noise)
AK4637 DAC=>SPK THD+N vs Frequency (-0.5dBFS; SPKG=01)

Figure 72. THD+N vs Input Frequency

AK4637 DAC=>SPK Linearity (fin=1kHz; SPKG=01)

Figure 73. Linearity
AK4637 DAC=>SPK Frequency Response (-0.5dBFS; SPKG=01)

Figure 74. Frequency Response

AK4637 DAC=>SPK THD+N vs Output Power (fin=1kHz; SPKG=00)

Figure 75. THD+N vs Output Power (SPKG=00)
AK4637 DAC=>SPK THD+N vs Output Power (fin=1kHz; SPKG=01)

Figure 76. THD+N vs Output Power (SPKG=01)

AK4637 DAC=>SPK THD+N vs Output Power (fin=1kHz; SPKG=10)

Figure 77. THD+N vs Output Power (SPKG=10)
AK4637 DAC=>SPK THD+N vs Output Power (fin=1kHz; SPKG=11)

Figure 78. THD+N vs Output Power (SPKG=11)
4. DAC (DAC → Line-out (AOUT))

AK4637 DAC=>Line-out FFT (0dBFS; LVCM=01)

Figure 79. FFT (Input level = 0dBFS)

AK4637 DAC=>Line-out FFT (-3dBFS; LVCM=01)

Figure 80. FFT (Input level = -3dBFS)
Figure 81. FFT (Input level = -60dBFS)

Figure 82. FFT (No signal)
AK4637 DAC=>Line-out Out of band noise (LVCM=01)

Figure 83. FFT (Out-of-band Noise)

AK4637 DAC=>Line-out Input Level (fin=1kHz; LVCM=01)

Figure 84. THD+N vs Input Level
AK4637 DAC=>Line-out THD+N vs Frequency (-3dBFS; LVCM=01)

Figure 85. THD+N vs Input Frequency

AK4637 DAC=>Line-out Linearity (fin=1kHz; LVCM=01)

Figure 86. Linearity
AK4637 DAC=>Line-out Frequency Response (-3dBFS; LVCM=01)

Figure 87. Frequency Response
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Date (YY/MM/DD)</th>
<th>Manual Revision</th>
<th>Board Revision</th>
<th>Reason</th>
<th>Page</th>
<th>Contents</th>
</tr>
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<tbody>
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<td>KM120600</td>
<td>0</td>
<td>First edition</td>
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<td>15/06/18</td>
<td>KM120601</td>
<td>1</td>
<td>Board change</td>
<td>1</td>
<td>AK4637: Rev.A → Rev.B</td>
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<tr>
<td></td>
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<td>Error correction</td>
<td>2</td>
<td>Correction of Figure and Name of Jumper pin JP3→JP13</td>
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|                 |                 |                |                     | 9 | Correction of Name of Jumper pin and Test pins  
|                 |                 |                |                     |     | (1-1) JP4→JP2  
|                 |                 |                |                     |     | (1-3) JP10→TP10  
|                 |                 |                |                     |     | (1-4) JP11→TP11, JP12→TP12  
|                 |                 |                | Description addition | 40-67 | Measurement data were added. |
| 16/06/02        | KM120602        | 2              | Board change | 70,71 | Part number was changed.(T2,T3) |
| 18/10/17        | KM120603        | 2              | Board change | 70 | Part number was deleted.(D1) |
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