GENERAL DESCRIPTION
The AKD4953A-B is an evaluation board for the AK4953A 24bit CODEC with built-in PLL and MIC/HP/SPK Amplifier. The AKD4953A-B has the interface with AKM’s A/D evaluation boards. Therefore, it’s easy to evaluate the AK4953A. The AKD4953A-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

Ordering Guide
AKD4953A-B --- Evaluation board for AK4953A
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION
- Compatible with 2 types of interface
  - Direct interface with AKM’s A/D converter evaluation boards
  - DIT/DIR with optical input/output
- 10pin header for serial control interface

Figure 1. AKD4953A-B Block Diagram
*Circuit diagram and PCB layout are attached at the end of this manual.
Figure 2. AKD4649-B Outline Chart

■ Comment

(1) J1, J2, J3 (Mini Jacks)
Analog signal input.

(2) J4, J5 (Mini Jacks)
Analog signal output.

(3) +5V, GND (Power Supply Terminal)
Connect power supply with these terminals.

(4) PORT1, PORT2 (Optical Connectors)
PORT1 (DIT) : Output optical signal from AK4118A.
PORT2 (DIR) : Input optical signal to AK4118A.

(5) PORT3 (10pin Header)
DSP port. MCLK, BICK, LRCK, SDTO and SDTI can be input/output from PORT3.

(6) PORT4 (10pin Header)
Control port. Connect the bundled cable into this port.
■ Operation sequence

1) Set up the power supply lines.

<table>
<thead>
<tr>
<th>Name</th>
<th>Color</th>
<th>Voltage</th>
<th>Comments</th>
<th>Attention</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5.0V</td>
<td>Red</td>
<td>+5.0V</td>
<td>Regulator</td>
<td>Power line is needed for this jack.</td>
</tr>
<tr>
<td>GND</td>
<td>Black</td>
<td>0V</td>
<td>Ground</td>
<td>Power line is needed for this jack.</td>
</tr>
</tbody>
</table>

Table 1. Set up of power supply lines

2) Set up the evaluation mode, jumper pins. (See the followings.)

3) Power on.

   The AK4953A and AK4118A should be reset once bringing SW1 “L” upon power-up.

■ Evaluation mode

(1) Slave mode

(1-1) Evaluation of Recording block (MIC, ADC) using DIT of AK4118A
(1-2) Evaluation of Playback block (HP, SPK) using DIR of AK4118A
(1-3) Evaluation of Loop-back using AK4118A <Default>
(1-4) All interface signals including master clock are fed externally.

(1-1) Evaluation of Recording block using DIT of AK4118A
PORT1 (DIT) and X1 (X’tal) are used. Nothing should be connected to PORT2 (DIR) and PORT3 (DSP).

(1-2) Evaluation of Playback block using DIR of AK4118A
PORT2 (DIR) is used. Nothing should be connected to PORT3 (DSP).

The AK4118A operates at fs of 32kHz or more. If the fs is slower than 32kHz, any other evaluation mode without using DIR should be used.

(1-3) Evaluation of Loop-back using AK4118A <Default>
X’tal oscillator (X1) is used. Nothing should be connected to PORT2 (DIR) and PORT3 (DSP).

The AK4118A operates at fs of 32kHz or more. If the fs is slower than 32kHz, any other evaluation mode without using DIR should be used.
(1-4) All interface signals including master clock are fed externally. PORT3 (DSP) is used. Nothing should be connected to PORT2 (DIR).

(2) Master mode

(2-1) Evaluation of Loop-back using MCLK of AK4118A

(2-2) Master clock is fed externally

(2-1) Evaluation of Loop-back using MCLK of AK4118A
X’tal oscillator (X1) is used. Nothing should be connected to PORT2 (DIR) and PORT3 (DSP). It is possible to evaluate the AK4953A on Internal Loopback mode. (ADCPF=PFDC bits= “1”) It is possible to evaluate at various sampling frequencies using built-in AK4953A’s PLL.

(2-2) Master clock is fed externally
PORT3 (DSP) is used and MCLK is fed from PORT3. Nothing should be connected to PORT2 (DIR). It is possible to evaluate the AK4953A on Internal Loopback mode. (ADCPF=PFDC bits= “1”) It is possible to evaluate at various sampling frequencies using built-in AK4953A’s PLL.
DIP Switch Set Up

[S1] (SW DIP-4): Mode setting of the AK4118A.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIF2</td>
<td></td>
<td></td>
<td>H</td>
</tr>
<tr>
<td>2</td>
<td>DIF1</td>
<td></td>
<td></td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>DIF0</td>
<td></td>
<td></td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>OCKS1</td>
<td></td>
<td></td>
<td>L</td>
</tr>
</tbody>
</table>

Table 2. Mode Setting of the AK4118A

<table>
<thead>
<tr>
<th>Mode</th>
<th>DIF2</th>
<th>DIF1</th>
<th>DIF0</th>
<th>DAUX</th>
<th>SDTO</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>24bit, Left justified</td>
<td>16bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>18bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>24bit, Left justified</td>
<td>20bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Right justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>24bit, I²S</td>
<td>24bit, I²S</td>
<td>L/H</td>
<td>O</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>24bit, Left justified</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>I</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>24bit, I²S</td>
<td>24bit, I²S</td>
<td>L/H</td>
<td>I</td>
</tr>
</tbody>
</table>

Table 3. AK4118A Audio Interface Format Setting

<table>
<thead>
<tr>
<th>OCKS1</th>
<th>MCKO1</th>
<th>X’tal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>256fs</td>
<td>256fs</td>
</tr>
<tr>
<td>1</td>
<td>512fs</td>
<td>512fs</td>
</tr>
</tbody>
</table>

Table 4. AK4118A Master Clock Setting
Other jumper pins set up

1. [JP1](SVDD) : Select SVDD Voltage
   1.8V : 1.8V Input.
   3.3V : 3.3V Input. <Default>
   5V : 5V Input. from “+5V” terminal.

2. [JP4](I2C) : Select I/F Mode.
   OPEN : 3-wire Serial Mode.
   SHORT : I2C Bus Mode. <Default>

   OPEN : Mic power is not connected. <Default>
   SHORT : Mic power is connected.

   3-wire : 3-wire Serial Mode.
   I2C : I2C Bus Mode. <Default>

5. JP18 (CAD0) : Select chip address in I2C Mode.
   OPEN : Chip address (CAD0) = “1”
   SHORT : Chip address (CAD0) = “0” <Default>

The function of the toggle SW

Serial Control

The AK4953A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (up/-I/F) with PC by 10 wire flat cable packed with the AKD4953A-B.

Analog Input/Output Circuits

(1) Input Circuits

Figure 3. Connect of 10 wire flat cable

Figure 4. Input Circuit
(2) Output Circuits

1. HP Output Circuit

![HP Output Circuit Diagram]

Figure 5. HP Output Circuit

2. SPEAKER Output Circuit

![SPEAKER Output Circuit Diagram]

Figure 6. SPEAKER Output Circuit
Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the “Driver Control Install Manual for AKM Device Control Software” for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Then please evaluate according to the following descriptions.

Operation Screen

1. Start up the control program following the process above.
2. After the evaluation board’s power is supplied, the AK4953A must be reset once bring SW1 (toggle Switch) “L” to “H”, and Click [RESET] button.
3. The operation screen is shown below.

Figure 7. Window of Control Soft
Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.
   (AKD4953A-B does not support READ function)

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area (on the right of the main window).
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.
    (AKD4953A-B does not support READ function)

12. [RESET]: Writes a reset command
    After the evaluation board power is supplied, the AK4953A must be reset once bring SW1 (toggle Switch) “L” to “H”, and then the [RESET] button should be clicked once to reset the register setting of the AK4953A.
Tab Functions

1. [Function]: Function control

This tab is for function control. Each operation is executed by the function buttons on the left side of the screen.

Figure 8. Window of [Function]
1-1. System Clock, Audio I/F Setting

When [System Clock Audio I/F] button is clicked, the window as shown in Figure 9 opens. This window is for System Clock and Audio I/F Setting. Refer to the datasheet for register settings of the AK4953A.

Figure 9. Window of [SystemClock AudioI/F]
1-2. ALC Setting

When [ALC Setting] button is clicked, the window as shown in Figure 10 opens. This window is for ALC setting. Refer to the datasheet for register settings of the AK4953A.

![Figure 10. Window of [ALC Setting]](image)
1-3. Volume Setting

When [Volume Setting] button is clicked, the window as shown in Figure 11 opens. This window is for Volume setting. Refer to the datasheet for register settings of the AK4953A.

![Volume Setting Window](image)

The volume can be controlled by slide bars. A register writing is made on every slide bar move.

After the volume slide is moved, it is reflected on to the register map and data writing dialog box.
Volume Control by Pull-down Menu

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that written in the dialog box. Use the mouse or arrow keys on the keyboard for small adjustments.

1-4. Beep Setting

When [Beep Setting] button is clicked, the window as shown in Figure 13 opens. This window is for Beep setting. Refer to the datasheet for register settings of the AK4953A.
1-5. Digital Filter Setting

A calculation of a coefficient of Digital Programmable Filters such as HPF and EQ filters, a register writing and a frequency response checking of HPF and EQ filter can be made. When [Digital Filter] button is clicked, the window as shown in Figure 14 opens.

Refer to the datasheet for register settings of the AK4953A.

![Digital Filter Setting Window](image-url)

Figure 14. Window of [Digital Filter Setting]
1-5-1. parameter Setting

(1) Please set a parameter of each Filter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Function</th>
<th>Setting Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>Sampling frequency (fs)</td>
<td>7350Hz ≤ fs ≤ 48000Hz</td>
</tr>
<tr>
<td>HPF</td>
<td>High pass filter cut off frequency</td>
<td>fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)</td>
</tr>
<tr>
<td>LPF</td>
<td>Low pass filter cut off frequency</td>
<td>fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs)</td>
</tr>
<tr>
<td>5 Band Equalizer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EQ1-5 Center Frequency</td>
<td>EQ1-5 Center Frequency</td>
<td>0Hz ≤ Center Frequency &lt; (0.497 * fs)</td>
</tr>
<tr>
<td>EQ1-5 Band Width</td>
<td>EQ1-5 Band Width (Note 1)</td>
<td>1Hz ≤ Band Width &lt; (0.497 * fs)</td>
</tr>
<tr>
<td>EQ1-5 Gain</td>
<td>EQ1-5 Gain (Note 2)</td>
<td>-1 ≤ Gain &lt; 3</td>
</tr>
</tbody>
</table>

Note 1. A gain difference is a bandwidth of 3dB from center frequency.
Note 2. When a gain is smaller than 0, EQ becomes a notch filter.

(2) “FIL3”, “EQ0”, “LPF”, “HPF”, “HPFAD”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5” Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed. (“1-5-4. automatic correction of the center frequency of a notch filter”)

Figure 15. Filter ON/OFF setting button
1-5-2. A calculation of a register

A register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

Figure 16. A register setting calculation result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”
1-5-3. Indication of a frequency characteristic

A frequency characteristic is displayed when push a [Frequency Response] button. Then, a register set point is also updated. Change "Frequency Range", and indication of a frequency characteristic is updated when push a [UpDate] button.

Followings are the cases when a register set value is updated.
1. When [Register Setting] button was pushed.
2. When [Frequency Response] button was pushed.
3. When [UpDate] button was pushed on a frequency characteristic indication window.
4. When set ON/OFF of a check button “Notch Filter Auto Correction”

1-5-4. Automatic correction of the center frequency of a notch filter

When set a gain of 5 band Equalizer to -1, Equalizer becomes a notch filter. When the center frequencies of plural notch filters are adjacent, produce a gap to central frequency (Figure 18). When check "a Notch Filter Auto Correction“ button, perform automatic correction of central frequency of a notch filter, display register setting after automatic correction and a frequency characteristic (Figure 19). This automatic correction is valid for a Equalizer Band which is set its gain to "-1".

(Note) When distance among center frequency is smaller than band width, there is a possibility that automatic correction is not performed properly. Please confirm a correction result by indication of a frequency characteristic.
Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width: 200Hz (3 band common)

Figure 18. When there is no center frequency revision

Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width: 200Hz (3 band common)

Figure 19. When there is a center frequency revision
2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch. Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red). Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray).

Grayout registers are Read Only registers. They can not be controlled. (AKD4953A-B does not support READ function)

The registers which is not defined in the datasheet are indicated as “---”.

![Figure 20. Window of [REG]](image-url)
**[Write]: Data Writing Dialog**

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or “0”. Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

Figure 21. Window of [Register Set]
3. [Tool]: Testing Tools

This tab screen is for evaluation testing tool. Click buttons for each testing tool.

Figure 22. Window of [Tool]
### Dialog Boxes

1. **[All Reg Write]: All Reg Write dialog box**

Click [All Reg Write] button in the main window to open register setting files. Register setting files saved by [SAVE] button can be applied.

![Figure 23. Window of [All Reg Write]](image)

**[Open (left)]:** Selecting a register setting file (*.akr).

**[Write]:** Executing register writing.

**[Write All]:** Executing all register writings.

Writings are executed in descending order.

**[Help]:** Help window is popped up.

**[Save]:** Saving the register setting file assignment. The file name is “*.mar”.

**[Open (right)]:** Opening a saved register setting file assignment “*.mar”.

**[Close]:** Closing the dialog box and finish the process.

*Operating Suggestions*

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.

2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.
2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box. Data write is available to specified address.

![Data Read/Write](image)

Address Box: Input data address in hexadecimal numbers for data writing.
Data Box: Input data in hexadecimal numbers.
Mask Box: Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write]: Writing to the address specified by “Address” box.

[Read]: Reading from the address specified by “Address” box.
The result will be shown in the Read Data Box in hexadecimal numbers.
(AKD4953A-B does not support READ function)

[Close]: Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.
3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box. Register sequence can be set in this dialog box.

![Sequence Setting](image)

**Figure 25. Window of [Sequence]**

**Sequence Setting**

Set register sequence by following process below.

1. Select a command
   - Use [Select] pull-down box to choose commands. Corresponding boxes will be valid.
   - < Select Pull-down menu >
     - No_use: Not using this address
     - Register: Register writing
     - Reg(Mask): Register writing (Masked)
     - Interval: Taking an interval
     - Stop: Pausing the sequence
     - End: Finishing the sequence
(2) Input sequence

[Address]: Data address
[Data]: Writing data
[Mask]: Mask

[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[ Interval ]: Interval time
Valid boxes for each process command are shown bellow.
· No _use: None
· Register: [Address], [Data], [Interval]
· Reg(Mask): [Address], [Data], [Mask], [Interval]
· Interval: [Interval]
· Stop: None
· End: None

Control Buttons

The function of Control Button is shown bellow.

[Start]: Executing the sequence
[Help]: Opening a help window
[Save]: Saving sequence settings as a file. The file name is “*.aks”.
[Open]: Opening a sequence setting file “*.aks”.
[Close]: Closing the dialog box and finish the process.

Stop of the sequence

When “Stop” is selected in the sequence, processing is paused and it starts again when [Start] button is clicked.
Restarting step number is shown in the “Start Step” box. When finishing the process until the end of sequence, “Start Step” will return to “1”.

The sequence can be started from any step by writing the step number to the “Start Step” box.
Write “1” to the “Start Step” box and click [Start] button, when restarting the process from the beginning.
4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box. Those files saved in the “Sequence setting dialog” can be applied in this dialog.

![Sequence by *.aks file](image)

Figure 26. Window of [Sequence(File)]

- **[Open (left)]**: Opening a sequence setting file (*.aks).
- **[Start]**: Executing the sequence setting.
- **[Start All]**: Executing all sequence settings. Sequences are executed in descending order.
- **[Help]**: Pop up the help window.
- **[Save]**: Saving sequence setting file assignment. The file name is “*.mas”.
- **[Open (right)]**: Opening a saved sequence setting file assignment “*.mas”.
- **[Close]**: Closing the dialog box and finish the process.

*Operating Suggestions*

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” is selected in the sequence the process will be paused and a pop-up message will appear. Click “OK” to continue the process.

![Sequence Pause](image)

Figure 27. Window of [Sequence Pause]
## Measurement Results

### Measurement Condition
- **Measurement unit**: Audio Precision, System two Cascade
- **MCKI**: 256fs (11.2896MHz, 24.576MHz)
- **BICK**: 64fs
- **fs**: 44.1kHz, 96kHz
- **Bit**: 24bit
- **Measurement Mode**: EXT Slave Mode
- **Power Supply**: SVDD=AVDD=TVDD=3.3V, DVDD=1.8V
- **Input Frequency**: 1kHz
- **Measurement Frequency**: 20 ~ 20kHz
- **Temperature**: Room

### Measurement Results

#### 1. ADC

<table>
<thead>
<tr>
<th>Result</th>
<th>Lch</th>
<th>Rch</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC: LIN1/RIN1 → ADC → IVOL, IVOL=0dB, ALC=OFF, MGAIN = +0dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fs=44.1kHz, BW=20kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>85.3</td>
<td>85.2</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>96.1</td>
<td>96.1</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>96.1</td>
<td>96.1</td>
<td>dB</td>
</tr>
<tr>
<td>fs=96kHz, BW=40kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/(N+D) (-1dBFS)</td>
<td>80.4</td>
<td>80</td>
<td>dB</td>
</tr>
<tr>
<td>DR (-60dBFS, A-Weighted)</td>
<td>97.3</td>
<td>97.3</td>
<td>dB</td>
</tr>
<tr>
<td>S/N (A-weighted)</td>
<td>97.3</td>
<td>97.3</td>
<td>dB</td>
</tr>
</tbody>
</table>

#### 2. DAC

<table>
<thead>
<tr>
<th>Result</th>
<th>Lch</th>
<th>Rch</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Headphone-Amp: DAC → HPL/HPR, ALC=OFF, OVOL=DVOL=0dB, RL=16Ω</td>
<td></td>
<td></td>
<td></td>
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<td>80.2</td>
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<td>S/(N+D)</td>
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<tr>
<td>S/N (A-weighted)</td>
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<td>dB</td>
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<th>Rch</th>
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<td>Speaker-Amp: DAC → SPP/SPN, IVOL=DVOL=0dB, RL=8Ω</td>
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<tr>
<td>S/N (A-Weighted)</td>
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<td>dB</td>
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Figure 28. FFT Plot (Input level= -1dBFS)

Figure 29. FFT Plot (Input level= -60dBFS)
Figure 30. FFT Plot (No signal)

Figure 31. THD+N vs. Input Level (fin=1kHz)
Figure 32. THD+N vs. Input Frequency (C24 and C25: Ceramic Capacitor)

In this case, a ceramic capacitor is used LIN1 and RIN1 pin on the AKD4953A-B. As the performance of a ceramic capacitor is not so good about low frequency signal. Refer to Figure 33 about the performance of AK4953A.

Figure 33. THD+N vs. Input Frequency (C24 and C25: Electrolytic Capacitor)
Figure 34. Linearity (fin=1kHz)

Figure 35. Frequency Response (Input level=-1dBFS)
Figure 36. Crosstalk Plot (Input level=-1dBFS)
ADC (LIN1/RIN1 → ADC) (0dB) \hspace{1cm} fs=96kHz

Figure 37. FFT Plot (Input level= -1dBFS)

Figure 38. FFT Plot (Input level= -60dBFS)
Figure 39. FFT Plot (No signal)

Figure 40. THD+N vs. Input Level (fin=1kHz)
In this case, a ceramic capacitor is used LIN1 and RIN1 pin on the AKD4953A-B. As the performance of a ceramic capacitor is not so good about low frequency signal. Refer to Figure 42 about the performance of AK4953A.

Figure 42. THD+N vs. Input Frequency (C24 and C25: Electrolytic Capacitor)
fs=96kHz

Figure 43. Linearity (fin=1kHz)

Figure 44. Frequency Response (Input level=-1dBFS)
Figure 45. Crosstalk Plot (Input level≈-1dBFS)
PLOT DATA
ADC (LIN1/RIN1 \rightarrow ADC) (+20dB) \text{ fs=44.1kHz}

Figure 46. FFT Plot (Input level= -1dBFS)

Figure 47. FFT Plot (Input level= -60dBFS)
Figure 48. FFT Plot (No signal)

Figure 49. THD+N vs. Input Level (fin=1kHz)
Figure 50. THD+N vs. Input Frequency (C24 and C25: Ceramic Capacitor)
In this case, a ceramic capacitor is used at LIN1 and RIN1 pin on the AKD4953A-B. As the performance of a ceramic capacitor is not so good about low frequency signal. Refer to Figure 51 about the performance of AK4953A.

Figure 51. THD+N vs. Input Frequency (C24 and C25: Electrolytic Capacitor)
Figure 52. Linearity (fin=1kHz)

Figure 53. Frequency Response (Input level=-1dBFS)
Figure 54. Crosstalk Plot (Input level=-1dBFS)
ADC (LIN1/RIN1 → ADC) (+20dB)

fs=96kHz

Figure 55. FFT Plot (Input level= -1dBFS)

Figure 56. FFT Plot (Input level= -60dBFS)
Figure 57. FFT Plot (No signal)

Figure 58. THD+N vs. Input Level (fin=1kHz)
In this case, a ceramic capacitor is used on LIN1 and RIN1 pin on the AKD4953A-B. As the performance of a ceramic capacitor is not so good about low frequency signal. Refer to Figure 60 about the performance of AK4953A.

Figure 60. THD+N vs. Input Frequency (C24 and C25: Electrolytic Capacitor)
Figure 61. Linearity (fin=1kHz)

Figure 62. Frequency Response (Input level=-1dBFS)
Figure 63. Crosstalk Plot (Input level=-1dBFS)
Figure 64. FFT Plot (Input level= 0dBFS)

Figure 65. FFT Plot (Input level= -3dBFS)
Figure 66. FFT Plot (No signal)

Figure 67. THD+N vs. Input Level (fin=1kHz)
Figure 68. THD+N vs. Input Frequency (Input level=-3dBFS)

Figure 69. Linearity (fin=1kHz)
Figure 70. Frequency Response (Input level=0dBFS)

Figure 71. Crosstalk Plot (Test Point is device pin)
Figure 72. FFT Plot (Input level= 0dBFS)

Figure 73. FFT Plot (Input level= -3dBFS)
Figure 74. FFT Plot (No signal)

Figure 75. THD+N vs. Input Level (fin=1kHz)
Figure 76. THD+N vs. Input Frequency (Input level=-3dBFS)

Figure 77. Linearity (fin=1kHz)
Figure 78. Frequency Response (Input level=0dBFs)

Figure 79. Crosstalk Plot (Test Point is device pin)
DAC (DAC → SPK, SPKG1-0="00")

fs=44.1kHz

Figure 80. FFT Plot (Input level= -0.5dBFS)

Figure 81. FFT Plot (Input level= -60dBFS)
Figure 82. FFT Plot (No Signal)

Figure 83. THD+N vs. Input Level (fin=1kHz)
Figure 84. THD+N vs. Input Frequency (Input level=-0.5dBFS)

Figure 85. Linearity (fin=1kHz)
Figure 86. Frequency Response (Input level=-0.5dBFS)

Figure 87. THD+N vs. Output Power
REVISION HISTORY

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