AKD4332-Sound Quality Evaluation Board Rev.1

1. GENERAL DESCRIPTION

The AKD4332-SA is a sound quality evaluation board for AK4332; mono advanced 32-bit high sound quality audio DAC with a headphone amplifier. The AKD4332-SA has digital audio interfaces. They can interface to digital audio systems via optical or coaxial connector.

Ordering Guide

AKD4332-SA --- AK4332 Sound Quality Evaluation Board
(Control software is included in this package.)

2. FUNCTION

- AK4332 dual configuration for stereo audio output
- 4 digital audio interfaces
  - Coaxial input (SPDIF)
  - Optical input (SPDIF)
  - 8-pin header for external interfaces (PCM)
  - 12-pin header for external interfaces (PDM / DSD)
- USB Port for Serial Control

Figure 1. AKD4332-SA Block Diagram (Note 1)

Note 1. Circuit diagram is attached at the end of this manual.
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4. Board Outline Diagram

■ Board Diagram

Figure 2. Board Diagram

■ Description

(1) Power Supply and GND connector (J2)
Refer to the “Set up the Power Supply Lines”.

(2) SPDIF input connector (PORT2 / Optical connector, J3 / RCA connector)
SPDIF signal inputs to the AK4118A.
When using J3 (RCA connector), R40 sets to “open” and R41 sets to “4.7ohm”, (Default)
When using PORT2 (Optical connector), R40 sets to “4.7ohm” and R41 sets to “open”.

(3) Analog output connector (J1 / Mini-Jack connector)
Connect to headphone.
(4) PDM or DSD signal input PORT (PORT1 (FPGA) / 2.54mm pitch 12 pin header)
12 pin header for interfacing with external data sources (PDM or DSD signal) can connect to audio system.
When using PORT1 (FPGA), R26, R28, R30 and R35 set to “open” and R27, R29 sets to “0ohm” and R25, R31 set to “10ohm”.

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-</td>
<td>open</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>open</td>
</tr>
<tr>
<td>5</td>
<td>-</td>
<td>open</td>
</tr>
<tr>
<td>7</td>
<td>-</td>
<td>open</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>open</td>
</tr>
<tr>
<td>11</td>
<td>I</td>
<td>PDMCLK</td>
</tr>
</tbody>
</table>

Table 1. Pin Assignment of PORT1 (FPGA)

Table 2. Pin Assignment of PORT5 (DSP)

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
<td>MCKI</td>
</tr>
<tr>
<td>3</td>
<td>I/O</td>
<td>BCLK</td>
</tr>
<tr>
<td>5</td>
<td>I/O</td>
<td>LRCK</td>
</tr>
<tr>
<td>7</td>
<td>I</td>
<td>SDTI</td>
</tr>
</tbody>
</table>

(5) PCM signal input PORT (PORT5 (DSP) / 2.54mm pitch 8 pin header)
8 pin header for interfacing with external data sources (PCM signal) can connect to audio system.
When using PORT5 (DSP), R26, R28, R30 and R35 set to “open” and R27, R29 sets to “0ohm” and R25, R31 set to “10ohm”.

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
<td>MCKI</td>
</tr>
<tr>
<td>3</td>
<td>I/O</td>
<td>BCLK</td>
</tr>
<tr>
<td>5</td>
<td>I/O</td>
<td>LRCK</td>
</tr>
<tr>
<td>7</td>
<td>I</td>
<td>SDTI</td>
</tr>
</tbody>
</table>

(6) USB PORT (PORT4 / USB micro-B)
Connect the USB cable for IBM-AT compatible computers to this port for a connection to a USB port of a PC.
Refer to the “  USB I/F (Serial Control)” for details.

(7) AK4118A (U7)
Digital Audio I/F Transceiver.
Refer to “  AK4118A Setting”.

(8) Power down/up toggle switch (SW1)
Power down/up the AK4332 and AK4118A (Keep “H” during normal operation).
This switch must be set to “L” once upon power up the evaluation board to reset the AK4332 and AK4118A.
5. Operation Sequence

■ Set up the Power Supply Lines

Table 3. Setup of power supply lines (J2 connector)

<table>
<thead>
<tr>
<th>Reference No.</th>
<th>Default Setting</th>
<th>Breakdown</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2(1 pin)</td>
<td>+4.3V~+5.5V [typ:+5.0V]</td>
<td>For regulator (U3, U4, U5)</td>
<td>Must be connected.</td>
</tr>
<tr>
<td>J2(2 pin)</td>
<td>0V</td>
<td>For ground</td>
<td>Must be connected.</td>
</tr>
</tbody>
</table>

■ Evaluation Mode

(1) D/A Evaluation using the AK4118A (DIR) (Coaxial connector)   < Default >

![Diagram](image)

Figure 3. D/A Evaluation using the AK4118A (DIR) (Coaxial connector)

Using the RCA connector (J3).
Setting: R40 = “open” and R41 = “4.7ohm”
R25, R27, R29 and R31 = “open”
R28 and R30 = “0 ohm”
R26 and R35 = “10 ohm”

(2) D/A Evaluation using the AK4118A (DIR) (Optical connector)

![Diagram](image)

Figure 4. D/A Evaluation using the AK4118A (DIR) (Optical connector)

Using the optical connector (PORT2).
Setting: R40 = “4.7ohm” and R41 = “open”
R25, R27, R29 and R31 = “open”
R28 and R30 = “0 ohm”
R26 and R35 = “10 ohm”
(3) D/A Evaluation using the external clock. (PCM data)
  All interface signals including the master clock are supplied externally.

![Figure 5. D/A Evaluation using the external clock. (PCM data)](image)

Using the 8pin header (PORT5)
Setting: R26, R28, R30 and R35 = “open”
R27 and R29 = “0 ohm”
R25 and R31 = “10 ohm”

(4) D/A Evaluation using the external clock. (PDM data, DSD data)
  All interface signals including the master clock are supplied externally.

![Figure 6. D/A Evaluation using the external clock. (PDM data, DSD data)](image)

Using the 12pin header (PORT1)
Setting: R26, R28, R30 and R35 = “open”
R27 and R29 = “0 ohm”
R25 and R31 = “10 ohm”

Table 4. Setting of evaluation mode

<table>
<thead>
<tr>
<th>Evaluation mode</th>
<th>(1) &lt;Default&gt;</th>
<th>(2)</th>
<th>(3)</th>
<th>(4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>connector</td>
<td>J3</td>
<td>PORT2</td>
<td>PORT5</td>
<td>PORT1</td>
</tr>
<tr>
<td>Signal input</td>
<td>SPDIF</td>
<td>SPDIF</td>
<td>PCM</td>
<td>PDM / DSD</td>
</tr>
<tr>
<td>R40</td>
<td>open</td>
<td>4.7 ohm</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>R41</td>
<td>4.7 ohm</td>
<td>open</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>R25</td>
<td>open</td>
<td>open</td>
<td>10 ohm</td>
<td>10 ohm</td>
</tr>
<tr>
<td>R26</td>
<td>10 ohm</td>
<td>10 ohm</td>
<td>open</td>
<td>open</td>
</tr>
<tr>
<td>R27</td>
<td>open</td>
<td>open</td>
<td>0 ohm</td>
<td>0 ohm</td>
</tr>
<tr>
<td>R28</td>
<td>0 ohm</td>
<td>0 ohm</td>
<td>open</td>
<td>open</td>
</tr>
<tr>
<td>R29</td>
<td>open</td>
<td>open</td>
<td>0 ohm</td>
<td>0 ohm</td>
</tr>
<tr>
<td>R30</td>
<td>0 ohm</td>
<td>0 ohm</td>
<td>open</td>
<td>open</td>
</tr>
<tr>
<td>R31</td>
<td>open</td>
<td>open</td>
<td>10 ohm</td>
<td>10 ohm</td>
</tr>
<tr>
<td>R35</td>
<td>10 ohm</td>
<td>10 ohm</td>
<td>open</td>
<td>open</td>
</tr>
</tbody>
</table>
- AK4118A Setting

Table 5. AK4118A Master Clock Setting

<table>
<thead>
<tr>
<th>OCKS1 (R24)</th>
<th>OCKS0 (R23)</th>
<th>MCKO1</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>256fs</td>
</tr>
</tbody>
</table>

Default setting of OCKS1 and OCKS0 are connected to GND via R24 and R23 respectively.

- Power ON

Power-down reset by SW1 (PDN) must be made once after power up the evaluation board. Put the SW1 to “L” for power-down reset of the AK4332 and AK4118A, and the return them to “H” to release the power-down states.

[SW1] (PDN): Reset the AK4332 and AK4118A (Keep “H” during normal operation).

This switch must be set to “L” once upon power up the evaluation board to reset the AK4332 and AK4118A.

- USB I/F (Serial Control)

Figure 7 shows a connection of a PC and an evaluation board. Two AK4332s on the AKD4332-SA can be controlled via USB port with a PC.

Connect PORT4 (USB connector) to a PC with micro USB cable. The software is included in the AKD4332-SA package.

Figure 7. Connection via the PC

■ Evaluation Board and Control Software Settings

1. Set up the evaluation board.
2. Connect the evaluation board to PC using a Micro USB cable.
3. The USB control is recognized as HID (Human Interface Device) on the PC.
4. Double-click the icon “AKD4332-SA.exe” to open the control program. (Note 2.)
5. When the screen does not display “AKDUSBIF-B” at bottom left, reconnect the PC using the USB cable, and push the [InitPort] button.
6. Begin evaluation by following the procedure below.

![Control Software Manual](image)

**Figure 8. Window of Control Soft**

Note 2. The AK4332 and AK4118A should be reset by the PDN pin ("L" -> "H") after the power supplies are applied.

Note 3. [MIX] button cannot be controlled on “AKD4332-SA.exe”.

Note 4. When push [InitPort] button, AK4332(U1) is set to HPL path and AK4332(U2) is set to HPR path respectively and DAC Adjustment1, DAC Adjustment2 resistors are set to fixed data.

Note 5. [InitPort] button must be push, after reset AK4332 and AK4118 by the PDN pin (“L” -> “H”).
Operation Overview

Function and Register map are controlled by this control software. These can be selected by the upper tabs.

Frequently used Buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window.

1. [Init Port]: Init the connection to PC. Click this button when connecting USB cable after the control software is set up. And some registers are set to fixed data.
   - Addr.07LH = “01H”
   - Addr.07RH = “02H”
   - Addr.26H = “02H”
   - Addr.27H = “C0H”

2. [Write Default]: Register Initialization. When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Read]: Executes read commands for all registers displayed.

4. [All Write]: Executes write commands for all registers displayed.

5. [Script Save]: Save the current register setting.
Tab MainFunc

1. [MainFunc] Tab: Function Control

When a button in the “Function” frame is clicked, a sequential process is executed.
(Refer to the “1-1. [Function] Block” section for details of each function button execution, or “1-3. Path and Various Setting Block” section for details of each functional register setting.)

![Diagram of MainFunc Window]

Figure 9. [MainFunc] Window

- [Function] block: Execute a sequential process shown on each button. (Refer to 1-1)
- Volume Control block: Execute a volume setting. (Refer to 1-2)
- Path and Various Setting block: Execute a various function setting. (Refer to 1-3)
1-1. [Function] Block

A function button executes the sequence process shown on each button and updates several registers. These functions are mainly for path settings.

Table 6. Sequence Process Setting

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
<th>Input</th>
<th>Output</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM Mode</td>
<td>Headphone Output</td>
<td>SDTI</td>
<td>HPL</td>
<td>SDTI→AK4332(U1)→HPL</td>
</tr>
<tr>
<td>(fs=48kHz, HPG=-4dB)</td>
<td>(MCKI use)</td>
<td></td>
<td>HPR</td>
<td>SDTI→AK4332(U2)→HPR</td>
</tr>
<tr>
<td>PDM 1-bit Mode</td>
<td>Headphone Output</td>
<td>PDMDI</td>
<td>HPL</td>
<td>PDMDI→AK4332(U1)→HPL</td>
</tr>
<tr>
<td>(PDMCLK=12.288MHz, HPG=-4dB)</td>
<td>(PDMCLK use)</td>
<td></td>
<td>HPR</td>
<td>PDMDI→AK4332(U2)→HPR</td>
</tr>
<tr>
<td>DSD Mode</td>
<td>Headphone Output</td>
<td>PDMDI</td>
<td>HPL</td>
<td>PDMDI→AK4332(U1)→HPL</td>
</tr>
<tr>
<td>(DSDCLK=3.072MHz, HPG=-4dB)</td>
<td>(DSDCLK use)</td>
<td></td>
<td>HPR</td>
<td>PDMDI→AK4332(U2)→HPR</td>
</tr>
</tbody>
</table>

The Setting of I/F mode is not changed. The default values are follows. I/F mode : 24bit I2S Justified.
1-1-1. [PCM Mode (fs = 48kHz, HPG = -4dB)] Sequential process

When [PCM Mode] button in the main window is clicked, the sequence for Headphone output is executed.

Address "07LH" and "07RH" are fixed.
Addr.07LH: LDAC bit="1"
Addr.07RH: RDAC bit="1"

Address "26H" and "27H" are fixed.
Addr.26H = "02H"
Addr.27H = "C0H"
1-1-2. [PDM 1-bit Mode (PDMCLK = 12.288MHz, HPG = -4dB)] Sequential process

When [PDM 1-bit Mode] button in the main window is clicked, the sequence for Headphone output is executed.

Figure 12. [PDM 1-bit Mode] Setting (After)

Address “07LH” and "07RH" are fixed.
Addr.07LH: LDAC bit="1"
Addr.07RH: RDAC bit="1"

Address “26H” and “27H” are fixed.
Addr.26H = "02H"
Addr.27H = "C0H"
1-1-3. [DSD Mode (DSDCLK = 3.072MHz, HPG = -4dB)] Sequential process

When [DSD Mode] button in the main window is clicked, the sequence for Headphone output is executed.

![Diagram of DSD Mode Setting](image)

**Figure 13. [DSD Mode] Setting (After)**

- **Address “07LH” and “07RH” are fixed.**
  - Addr.07LH: LDAC bit="1"
  - Addr.07RH: RDAC bit="1"

- **Address “26H” and “27H” are fixed.**
  - Addr.26H = “02H”
  - Addr.27H = “C0H”
1-2. Volume Control by Slider

The volume can also be changed by slider. When a value is input in the edit box, the slider is moved to the value that selected by the edit box. Use the mouse or arrow keys on the keyboard for fine tuning.

![Volume Control Block Diagram]

Figure 14. Volume Control Block
1-3. Path and Various Setting Block

The Path which can be used is displayed. The FS and CM bits, etc… can be set up. [PCM I/F], [PDM 1-bit I/F], [DSD I/F], [Headphone] -- each setting dialog can be opened.

![Path and Various Setting Block Diagram]

**Figure 15. [Path and Various Setting] Block**

- [PCM I/F] Button: Opens “PCM I/F Setting” dialog box.
- [PDM 1-bit I/F] Button: Opens “PDM 1-bit I/F Setting” dialog box.
- [DSD I/F] Button: Opens “DSD I/F Setting” dialog box.
- [Headphone] Button: Opens “Headphone Setting” dialog box.
- [Slave] Button: Master Mode/Slave Mode is changed.
- [Power-Down/Up] Button: Power OFF/ON is changed. *(Note 6) (Note 7)*
- [Audio I/F] Combo Box: Audio I/F is changed.
- [Digital Filter] Combo Box: Digital Filter is changed.

**Note 6.** The default value of HP Gain is 0dB and OVL bits is set to 0dB.
(Recommend value of HPG bits is -4dB)

**Note 7.** There are some registers which are set up automatically at Power-Up/Down.
(Refer to the next table)

<table>
<thead>
<tr>
<th>Register</th>
<th>Setup value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Up</strong></td>
<td></td>
</tr>
<tr>
<td>PMPLL</td>
<td>“1” is set at PLL mode.</td>
</tr>
<tr>
<td>PMCP1, PMCP2, PMLDO1P,</td>
<td>“1”</td>
</tr>
<tr>
<td>PMLDO1N, PMDA, PMHP, PMTIM</td>
<td>* Process is executed in order of the sequence of datasheet.</td>
</tr>
<tr>
<td><strong>Power Down</strong></td>
<td></td>
</tr>
<tr>
<td>PMPLL, PMCP1, PMCP2, PMLDO1P,</td>
<td>“0”</td>
</tr>
<tr>
<td>PMLDO1N, PMDA, PMHP, PMTIM</td>
<td>* Process is executed in order of the sequence of datasheet.</td>
</tr>
</tbody>
</table>
1-3-1. [PCM I/F]: [PCM I/F Setting] Dialog Box

Click the [PCM I/F] button in the main window to open PCM I/F setting dialog box. When PDM bit is "0" and [Power-Down/Up] Button is “Power-Down”, PCM I/F can be set up. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![Figure 16. [PCM I/F setting] Window](image)

1-3-2. [PDM 1-bit I/F]: [PDM 1-bit I/F Setting] Dialog Box

Click the [PDM 1-bit I/F] button in the main window to open PDM 1-bit I/F setting dialog box. When PDM bit is ”1” and PDMMODE bit is “0”, PDM 1-bit I/F can be set up. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![Figure 17. [PDM 1-bit I/F setting] Window](image)

1-3-3. [DSD I/F]: [DSD I/F Setting] Dialog Box

Click the [DSD I/F] button in the main window to open DSD I/F setting dialog box. When PDM bit is ”1” and PDMMODE bit is “1”, DSD I/F can be set up. The settings on this dialog are interlocked with the settings on register map. (Refer to the datasheet for register definitions.)

![Figure 18. [DSD I/F setting] Window](image)
1-3-4. [Headphone]: [Headphone Setting] Dialog Box

Click the [Headphone] button in the main window to open Headphone setting dialog box. The settings on this dialog are interlocked with the settings on register map.
(Refer to the datasheet for register definitions.)

![Headphone Setting](image)

Figure 19. [Headphone setting] Window

1-3-5. [Audio I/F]: [Audio I/F Setting] Combo Box

Click the [Audio I/F] Combo box in the main window to open Audio I/F setting list. The settings on this dialog are interlocked with the settings on register map.
(Refer to the datasheet for register definitions.)

![Audio I/F Setting](image)

Figure 20. [Audio I/F] Combo box

1-3-6. [Digital Filter]: [Digital Filter Setting] Combo Box

Click the [Digital Filter] Combo box in the main window to open Digital Filter setting list. When PDM bit is "0", Digital Filter can be set up. The settings on this dialog are interlocked with the settings on register map.
(Refer to the datasheet for register definitions.)

![Digital Filter Setting](image)

Figure 21. [Digital Filter] Combo box
2. [Script] Tab: Script Function

This tab is for script file executing.

As a script file is selected, the program is executed automatically.
By clicking the [Repeat] button, the selected script file will be executed once again.

![Figure 22. [Script] Window](image)

<table>
<thead>
<tr>
<th>Command</th>
<th>notation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[SCRIPT]</td>
<td>-</td>
<td>Header of script file. A data error will be detected without this header.</td>
</tr>
<tr>
<td>; Comment</td>
<td>-</td>
<td>The line following to “;” is recognized as comment and ignored.</td>
</tr>
</tbody>
</table>
| W:<address>,<data> | base 16 (HEX) | Register write is executed.  
    Address : 1 byte  
    Date : 1 byte |
| T,<wait>     | base 10 (DN) | Wait some micro sec.  
    50msec wait. |

Table 7. Command of Script
3. [RegMap] Tab: Register Map

This tab is for register read and write.

Each register on the register map are push-button switch. The register is updated by mouse operation. Button Down indicates “1” and the register name is shown in red (when read-only the name is shown in dark red). Button Up indicates “0” and the register name is shown in blue (when read-only the name is shown in gray).

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “0” or “1”.

![Figure 23. [RegMap] Window](image-url)
3-1. [Write]: Data Write Dialog

Select the [Write] button located on the right of each corresponding address when changing two or more registers on the same address simultaneously.

Click the [Write] button located on the right of each corresponded address for a pop-up dialog box.

When the check box next to the register name is checked, the data will become “1”. When the check box is not checked, the data will become “0”.

Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

![Figure 24. [RegWrite] Window](image)

3-2. [Read]: Data Read

Click the [Read] button located on the right of each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand Address: Data window.
Button Down indicates “1” and the register name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “0” and the register name is shown in blue (when read-only the name is shown in gray).
# 7. Revision History

<table>
<thead>
<tr>
<th>Date (YY/MM/DD)</th>
<th>Manual Revision</th>
<th>Board Revision</th>
<th>Reason</th>
<th>Page</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>18/10/29</td>
<td>KM130500</td>
<td>1</td>
<td>First edition</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>19/03/18</td>
<td>KM130501</td>
<td>1</td>
<td>Change</td>
<td>4</td>
<td>Table1 was changed.</td>
</tr>
<tr>
<td>19/03/18</td>
<td>KM130501</td>
<td>1</td>
<td>Change</td>
<td>6</td>
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