



AKD4430-SB

AK4430 Evaluation Board Rev.0

General Description

AKD4430-SB is an evaluation board for AK4430 (192kHz sampling 24Bit Stereo $\Delta \Sigma$ DAC with 2Vrms Output). AKD4430-SB has a digital audio interface (AK4115) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4430.

■ **Ordering Guide**

AKD4430-SB ---- AK4430 Evaluation Board

Function

- On-board digital audio interface. (AK4115)

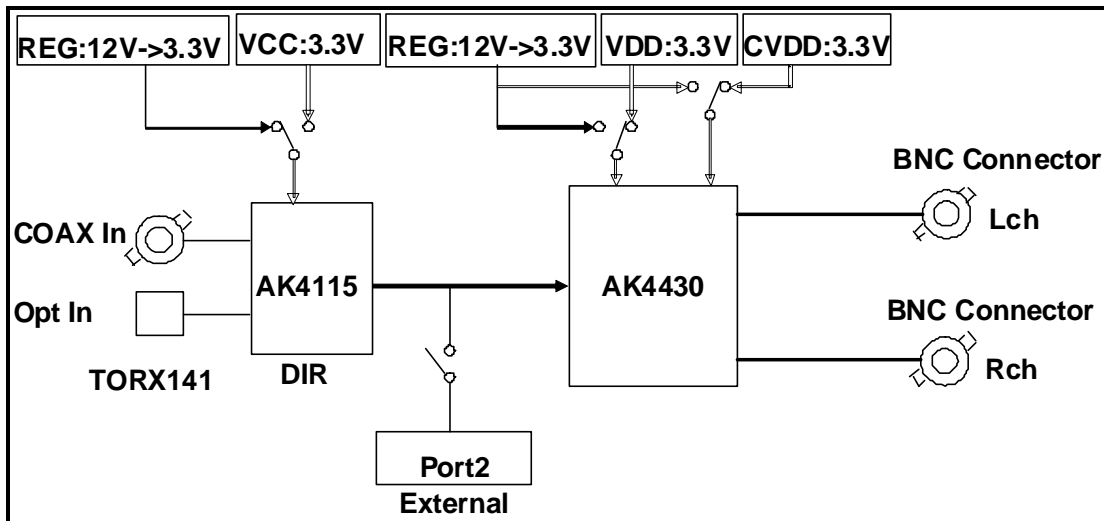


Figure 1. AKD4430-SB Block diagram
 (* Circuit diagram are attached at the end of this manual.)

Board Outline Chart

■ Outline Chart

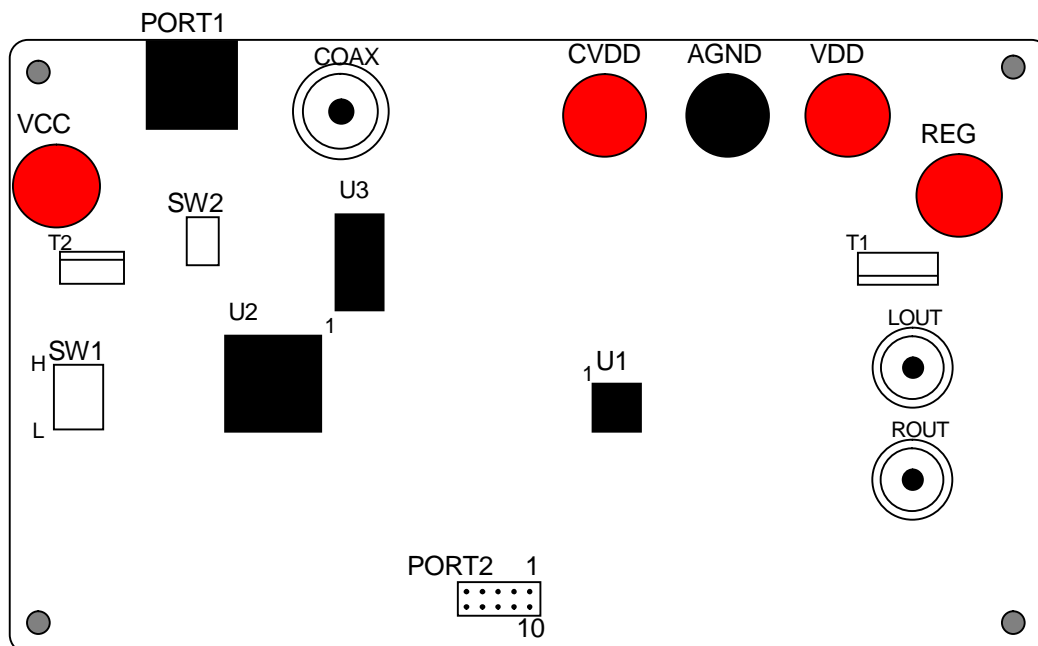


Figure 2. AKD4430-SB Outline Chart

■ Comment

- (1) LOUT, ROUT (BNC-JACK)
It is analog signal output Jack. The signal is output from LOUT/ROUT pins.
- (2) COAX, PORT1, PORT2 (Digital signal connector)
COAX (BNC-JACK): Digital signal (SPDIF, Fs: 24~48kHz) is input to the AK4115. (Default)
PORT1 (Optical Connector): Optical digital signal (SPDIF, Fs: 32~48kHz) is input to the AK4115.
PORT2 (10 pin header): The clock and data can be input and output with this connector.
- (3) REG, VDD, AGND, CVDD, VCC
These are the power supply connectors. Connect power supply with these pins.
As for the detail comments, refer to the setup of power supply in P3.
- (4) SW1, SW2 (Switch)
SW1: Setting of frequency of MCKO that is output from AK4115.
SW2: Reset of AK4115. Keep "H" during normal operation.

■ Operation sequence

- 1) Set up the power supply lines.
Each supply line should be distributed from the power supply unit.

Name of jack	Color of jack	Typ Voltage	Voltage Range	Using	Default Setting
VCC1 (Note 1)	Red	+12V	+7~+15V	AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit (Regulator:T2)	Connected to +12V
VDD1	Red	+3.3V	+3~+3.6V	VDD of AK4430	Open
CVDD1	Red	+3.3V	+3~+3.6V	CVDD of AK4430	Open
AGND2	Black	0V	0V	Ground	Connected to GND (Should be connected)
REG (Note 2)	Red	+12V	+7V~+15V	VDD, CVDD of AK4430 (Regulator:T1)	Connected to +12V

Table 1.Set up of power supply lines

Note 1) In case of using +3.3V power supply to connect VCC1, It is possible to supply the voltage to AK4115 and the Logic circuit without using Regulator.

In this case, change to R36: Open → Short (0 Ω); R34,R35: Short (0 Ω) → Open

Note 2) In case of using +12V power supply to connect REG, Use regulator: T1 can supply AK4430 with clean voltage. (Default)

In this case, change to R25,R44: Short (0 Ω) → Open; R37,R43:Open → Short (0 Ω); VDD, CVDD should be open.

- 2) DIP Switch setting:

Refer to Table 2 and Table 3

- 3) Power Down:

The AK4115 should be reset once by bringing SW2 (AK4115 PDN) “L” upon power-up.

■ Evaluation mode

1. Using DIR (Optical Link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1: TORX141). It is possible to evaluate the AK4430 by using CD disk.

Setting: R19: Open → 470Ω; R33: short (0Ω) → Open

2. Using DIR (COAX) (Default)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4430 by using CD disk.

Setting: R19: Open; R33: short (0Ω); (Default)

* COAX is recommended for an evaluation of the Sound quality.

3. Supply all interface signals that include master clock via PORT2 from external equipments..

Setting: R11: 5.1Ω → Open
R12, R13, R14: 51Ω → Open
R15, R16, R17, R18: Open → 51Ω ? or short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

■ Setting of DIP switch

[SW1]: AK4115 setting

No.	Pin	OFF (“L”)	ON (“H”)	Default の状態
1	OCKS0	AK4115’s Master Clock setting Look Table 3		L
2	OCKS1			H

Table 2. SW1 setting

OCKS1	OCKS0	MCLK Frequency	Default
0	0/1	256fs @ fs=96kHz	
1	0	512fs @ fs=48kHz	
1	1	128fs @ fs=192kHz	

Table 3. MCLK clock setting

■ Setting of SW2 switch

[SW2] (PDN): Reset of AK4115. Keep “H” during normal operation.

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722 (No.00454)
- MCLK : 512fs, 256fs, 128fs
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : REG(+12/3.3V)=VCC1=+12V, AGND2=GND
(Regulator VDD=CVDD=+3.3V , Regulator VCC=+3.3V)
- Interface : DIR
- Temperature : Room

Table Data

fs=44.1kHz, MCLK=512fs, BICK=64fs

Parameter	Input signal	Measurement filter	Lch	Rch	Unit
THD+N	1kHz, 0dBFS	20kHz LPF	-91.5	-91.4	dB
DR	1kHz, -60dBFS	20kHz LPF, A-weighted	104.3	104.4	dB
S/N	"0" data	20kHz LPF, A-weighted	104.3	104.4	dB

fs=96kHz, MCLK=256fs, BICK=64fs

Parameter	Input signal	Measurement filter	Lch	Rch	Unit
THD+N	1kHz, 0dBFS	40kHz LPF	-90.3	-90.1	dB
DR	1kHz, -60dBFS	40kHz LPF, A-weighted	103.8	103.8	dB
S/N	"0" data	40kHz LPF, A-weighted	103.8	103.8	dB

fs=192kHz, MCLK=128fs, BICK=64fs

Parameter	Input signal	Measurement filter	Lch	Rch	Unit
THD+N	1kHz, 0dBFS	40kHz LPF	-88.7	-88.5	dB
DR	1kHz, -60dBFS	40kHz LPF, A-weighted	103.5	103.5	dB
S/N	"0" data	40kHz LPF, A-weighted	103.7	103.7	dB

Plot Data

fs=44.1kHz

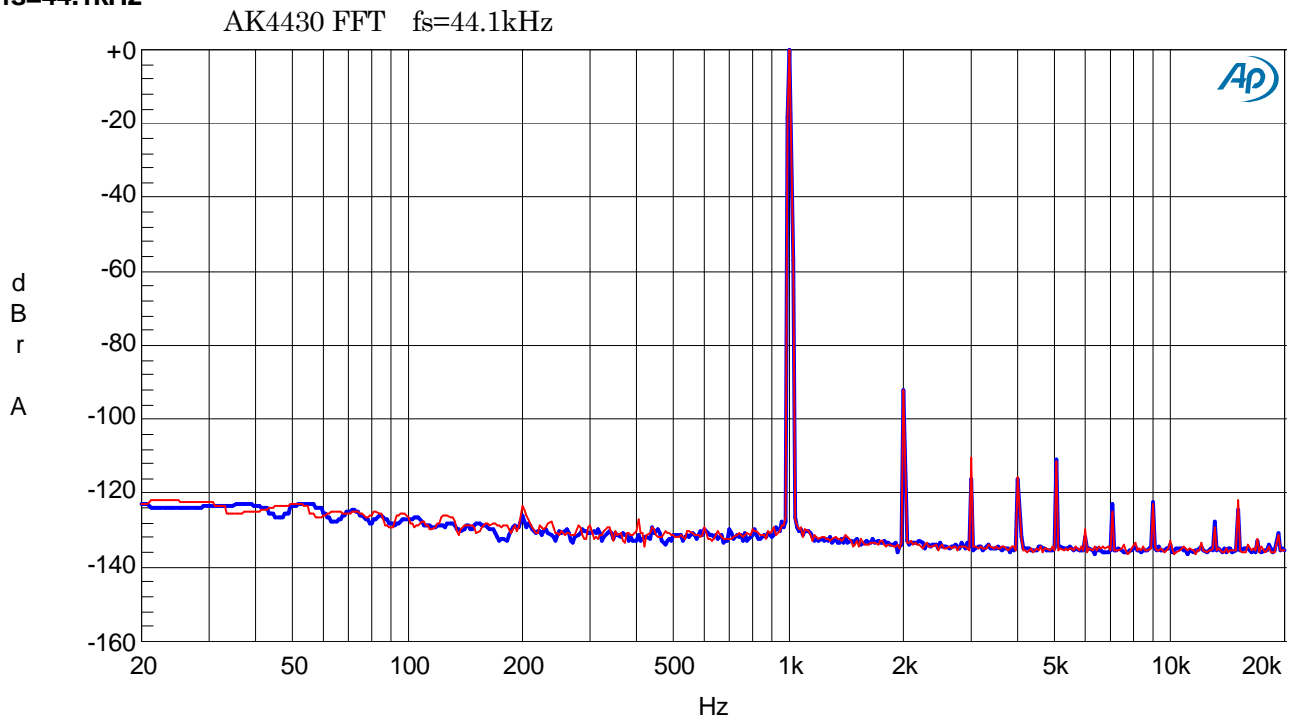


Figure 1. FFT (0dBFS Input ,fin=1kHz)

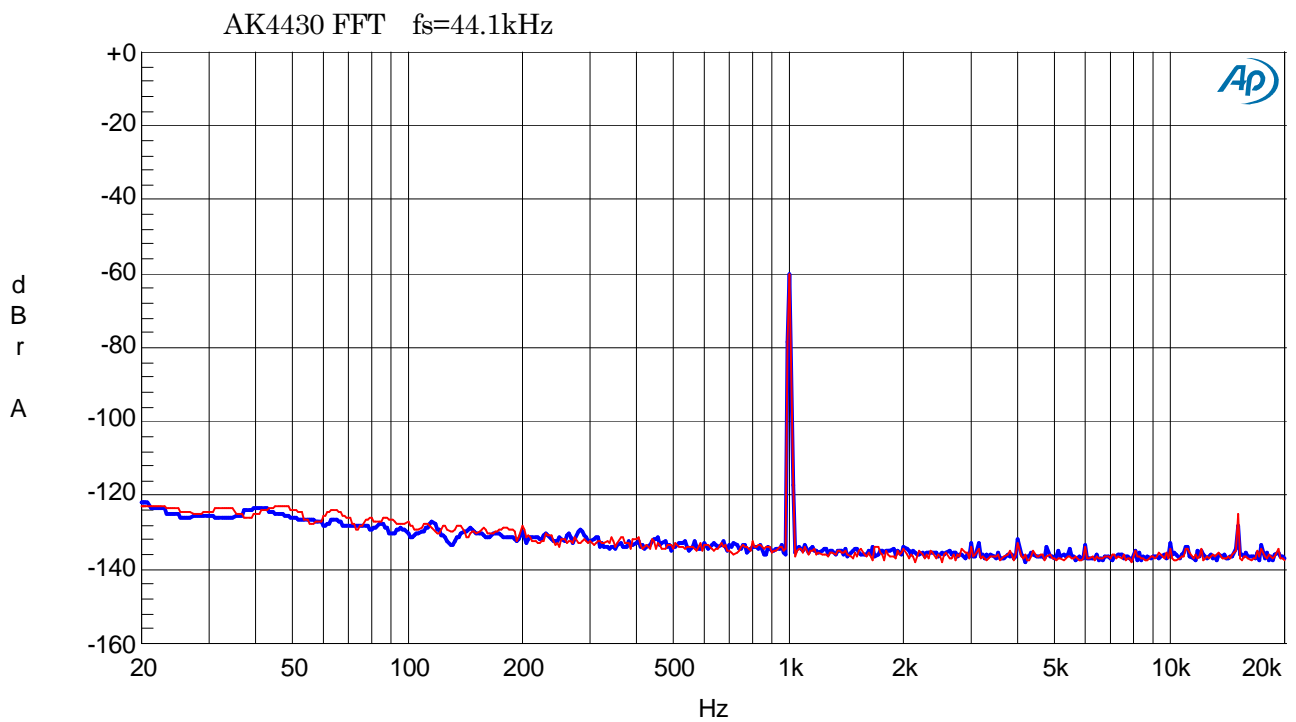


Figure 2. FFT (-60dBFS Input, fin=1kHz)

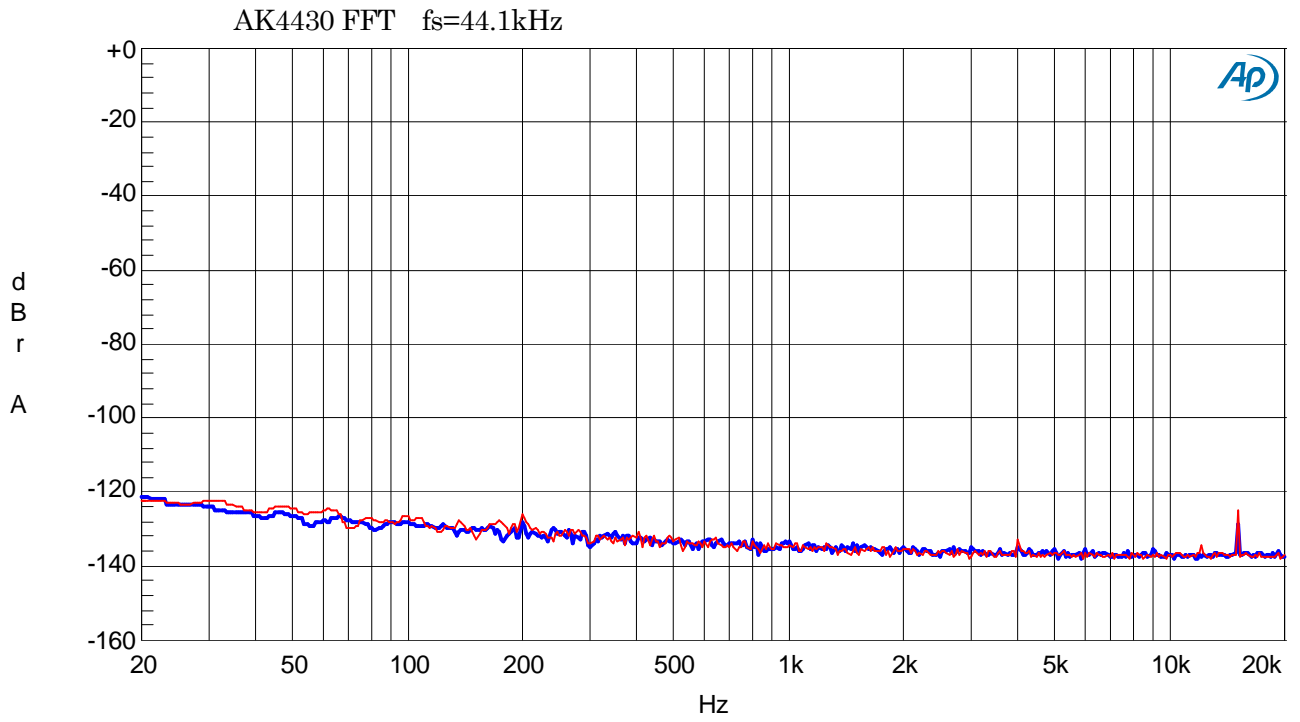


Figure 3. FFT (No Signal)

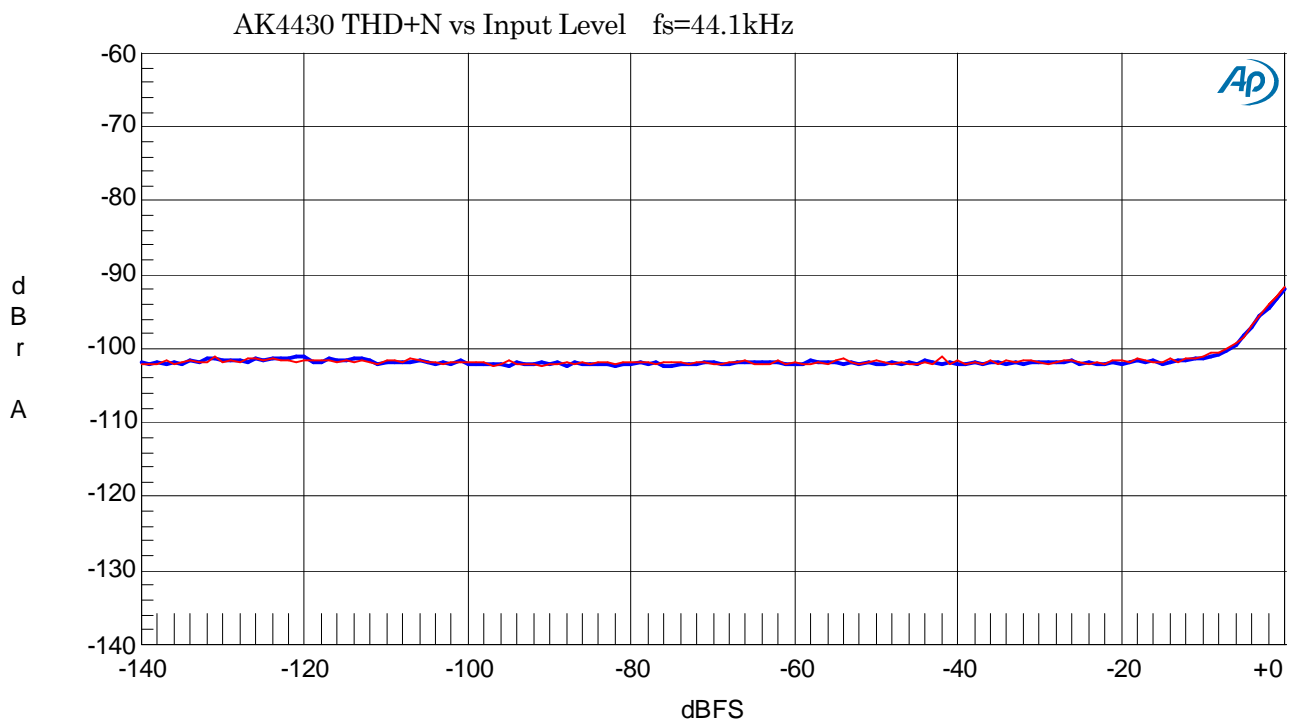


Figure 4. THD + N vs Input Level (fin=1kHz)

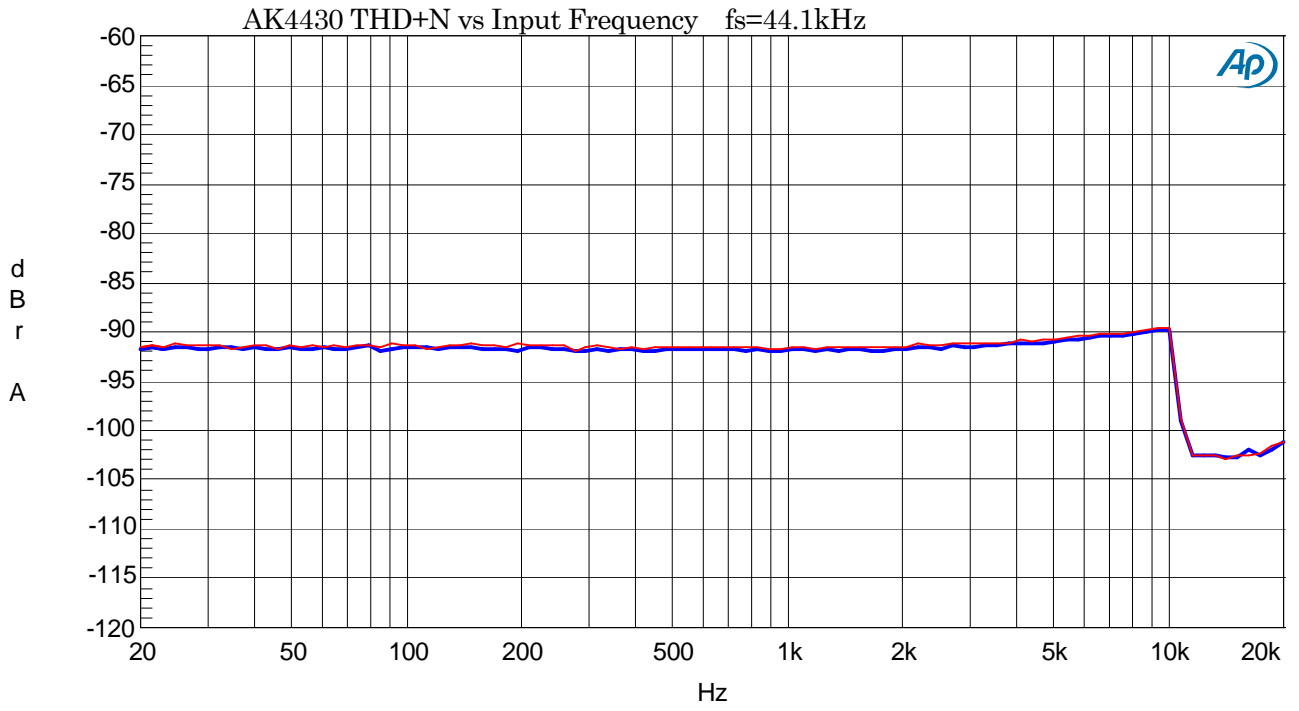


Figure 5. THD + N vs Input Frequency (0dBFS Input)



Figure 6. Linearity (fin=1kHz)

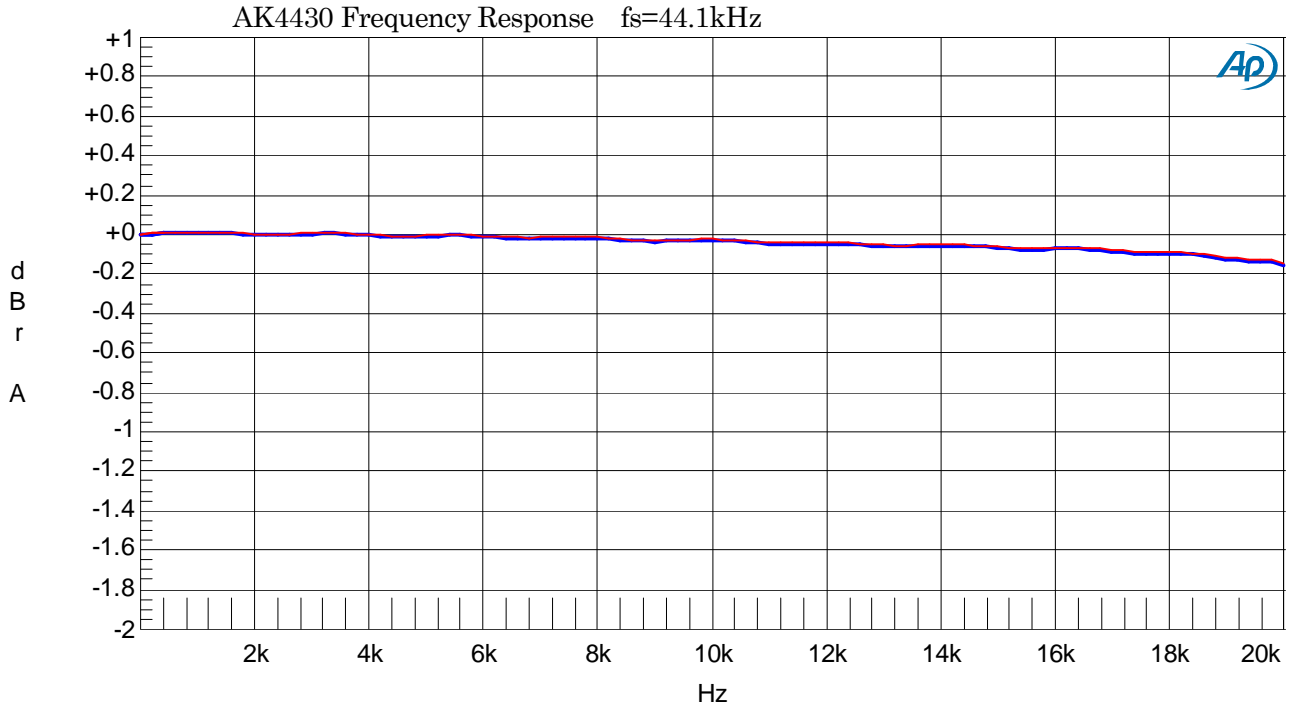


Figure 7. Frequency Response (0dBFS Input)

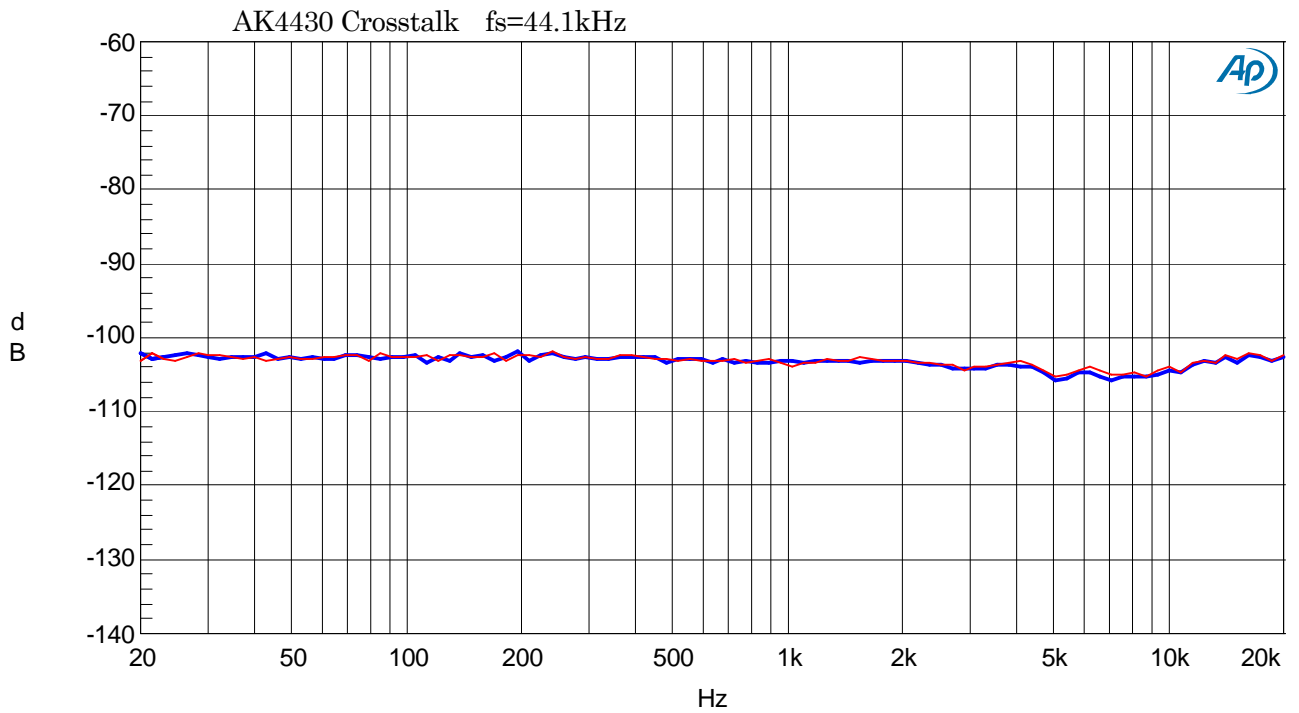


Figure 8. Crosstalk (0dBFS Input)

fs=96kHz

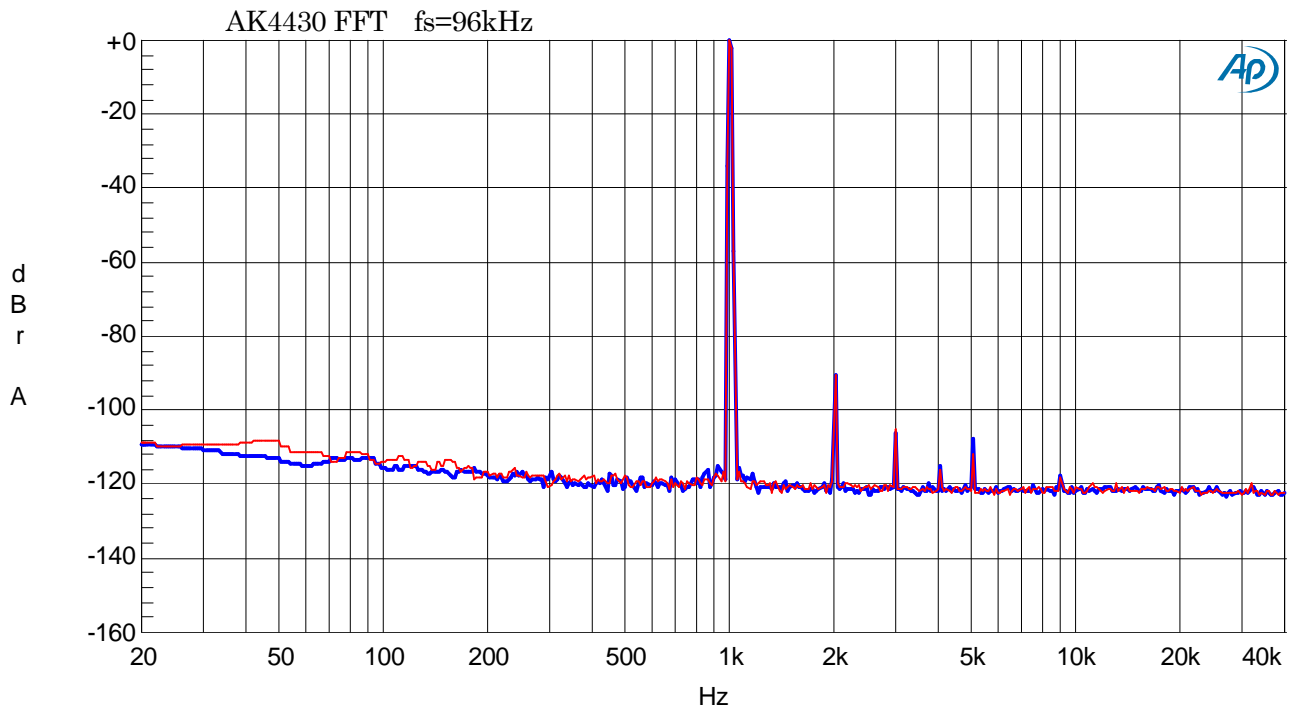


Figure 9.FFT (0dBFS Input, fin=1kHz)

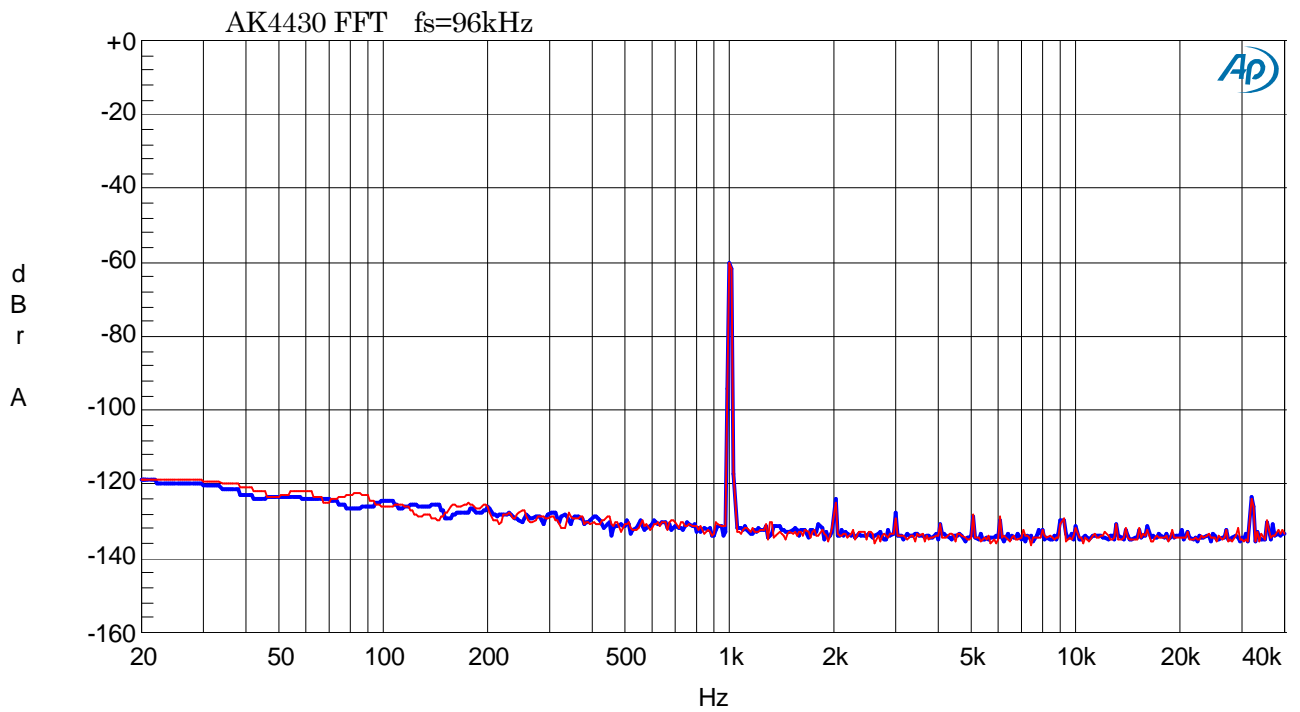


Figure 10. FFT (-60dBFS Input, fin=1kHz)

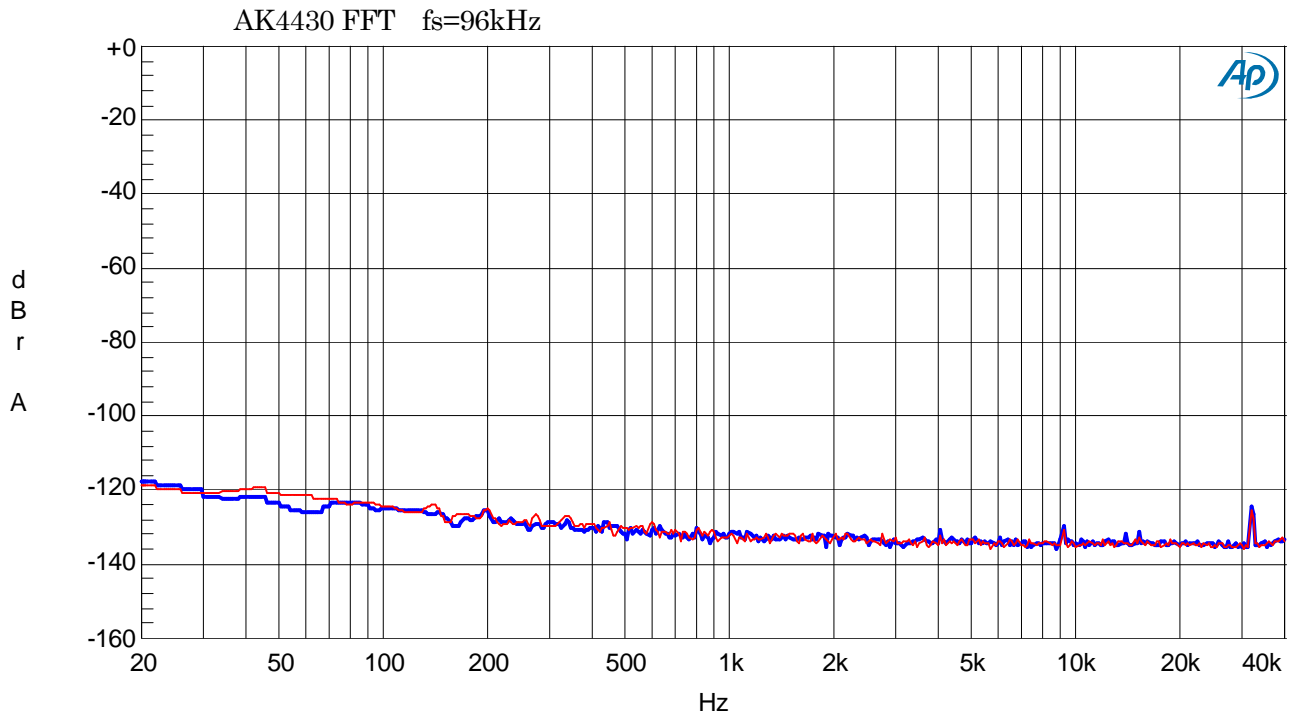


Figure 11.FFT (No Signal)

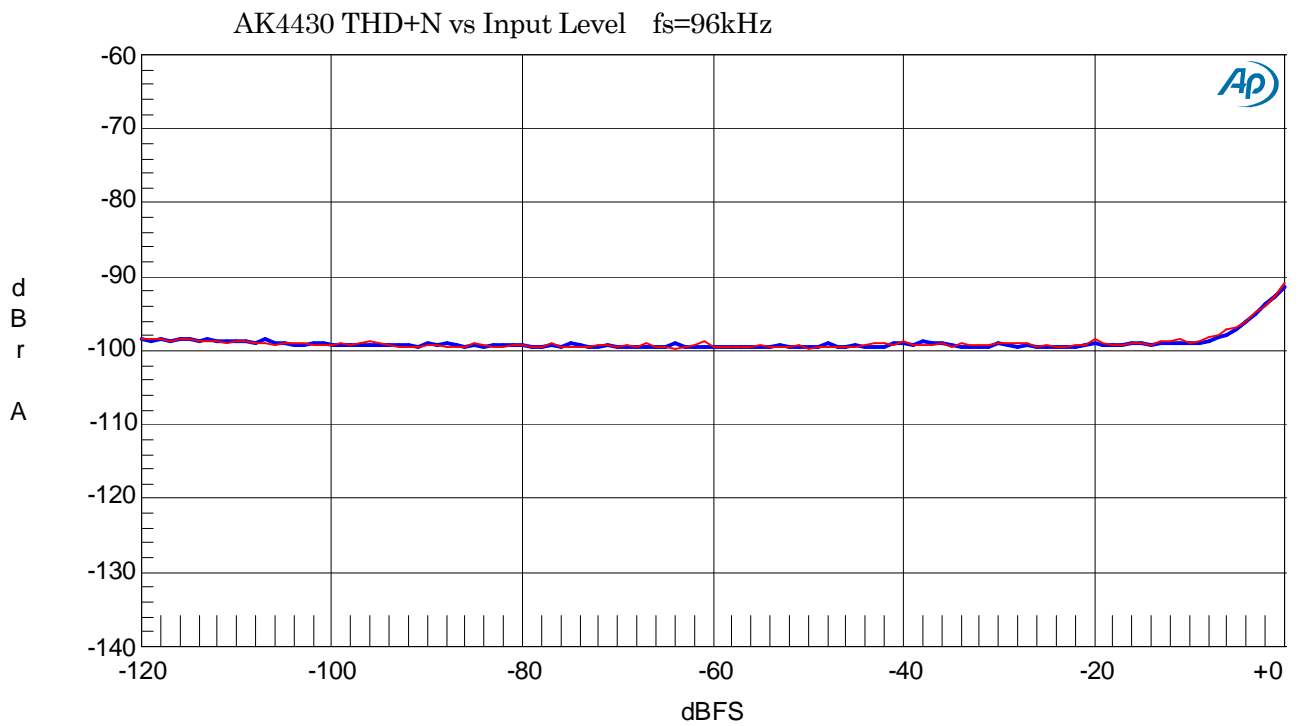


Figure 12. THD+N vs Input Level (fin=1kHz)

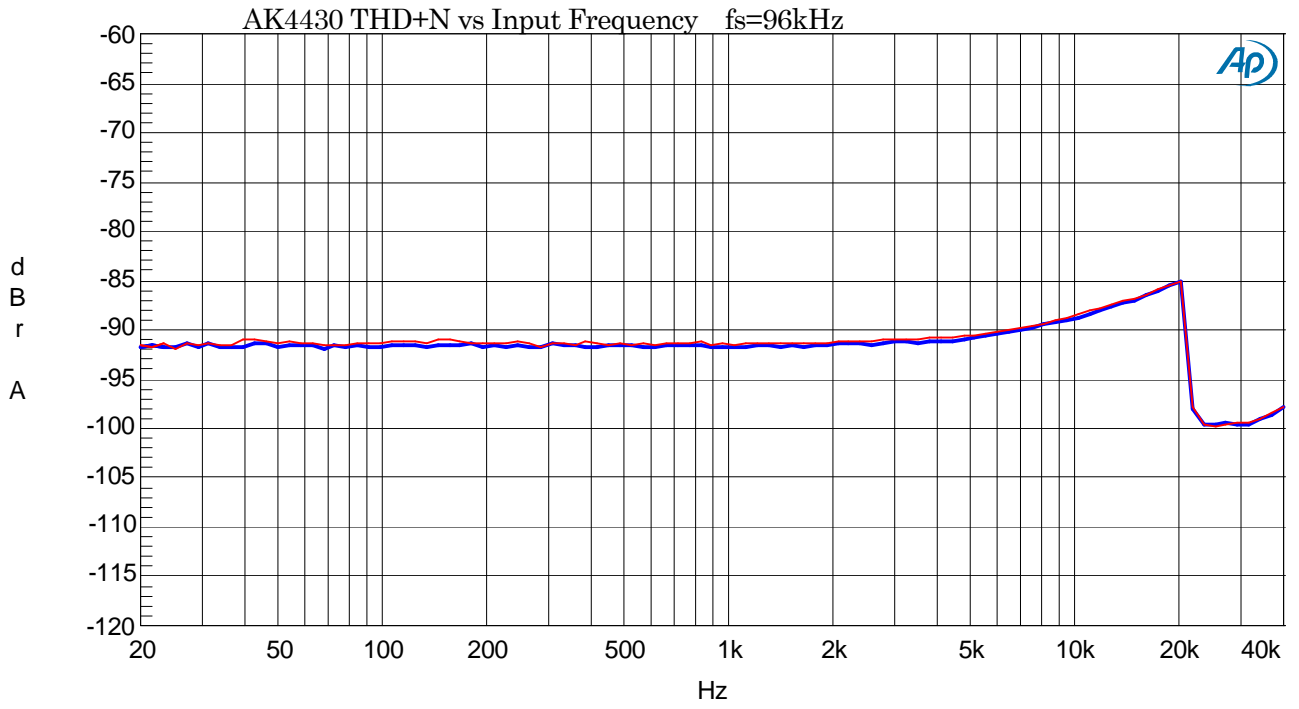


Figure 13. THD+N vs Input Frequency (0dBFS Input)

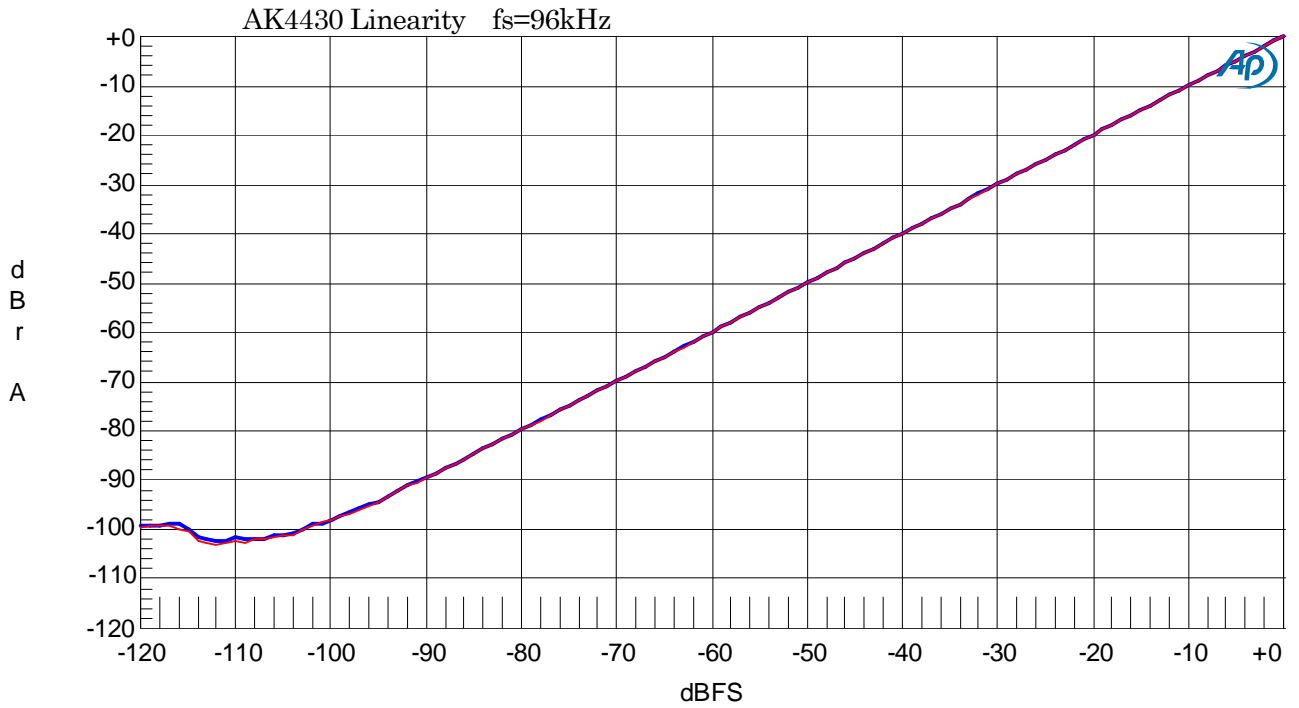


Figure 14. Linearity (fin=1kHz)

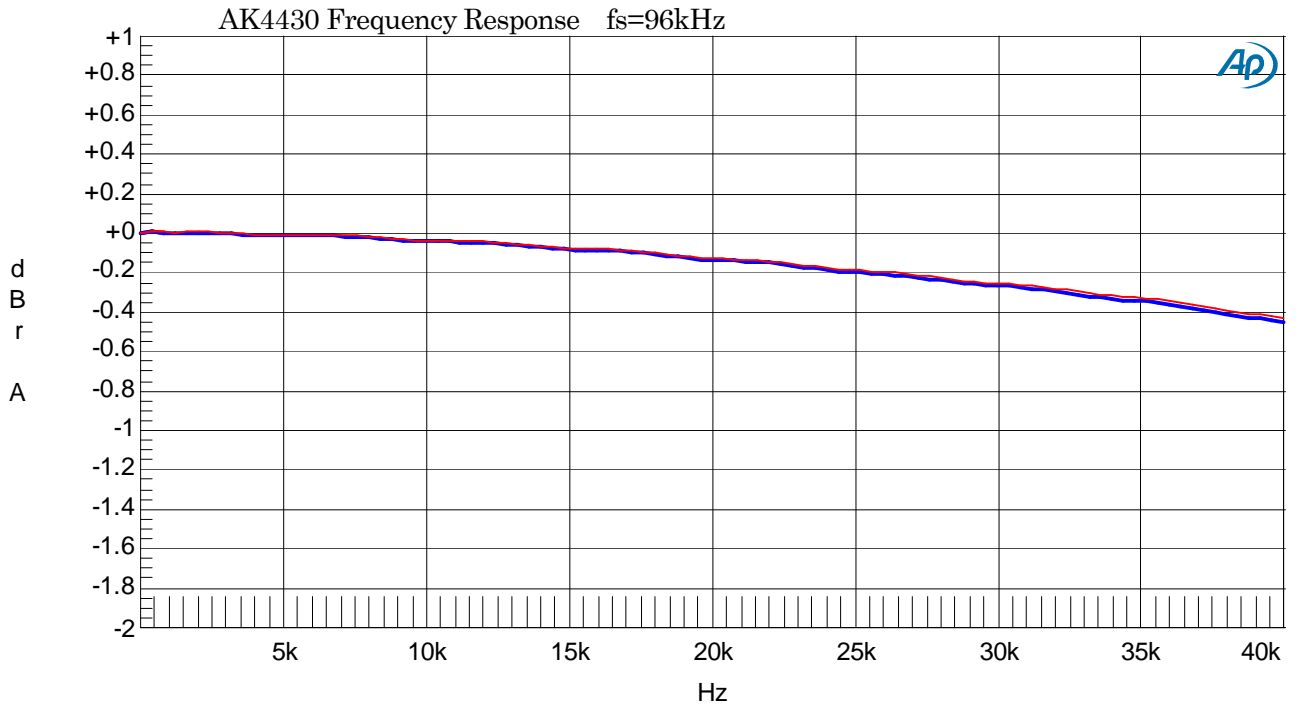


Figure 15. Frequency Response (0dBFS Input)

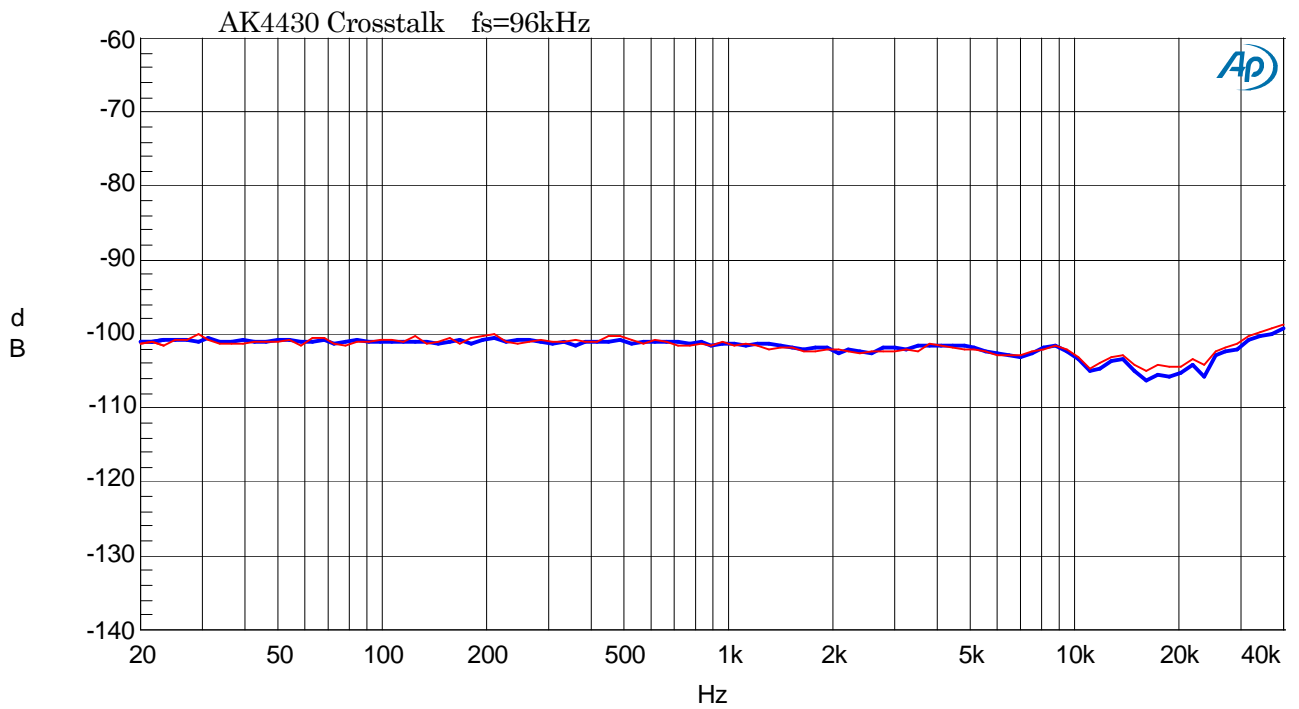


Figure 16. Crosstalk (0dBFS Input)

fs=192kHz

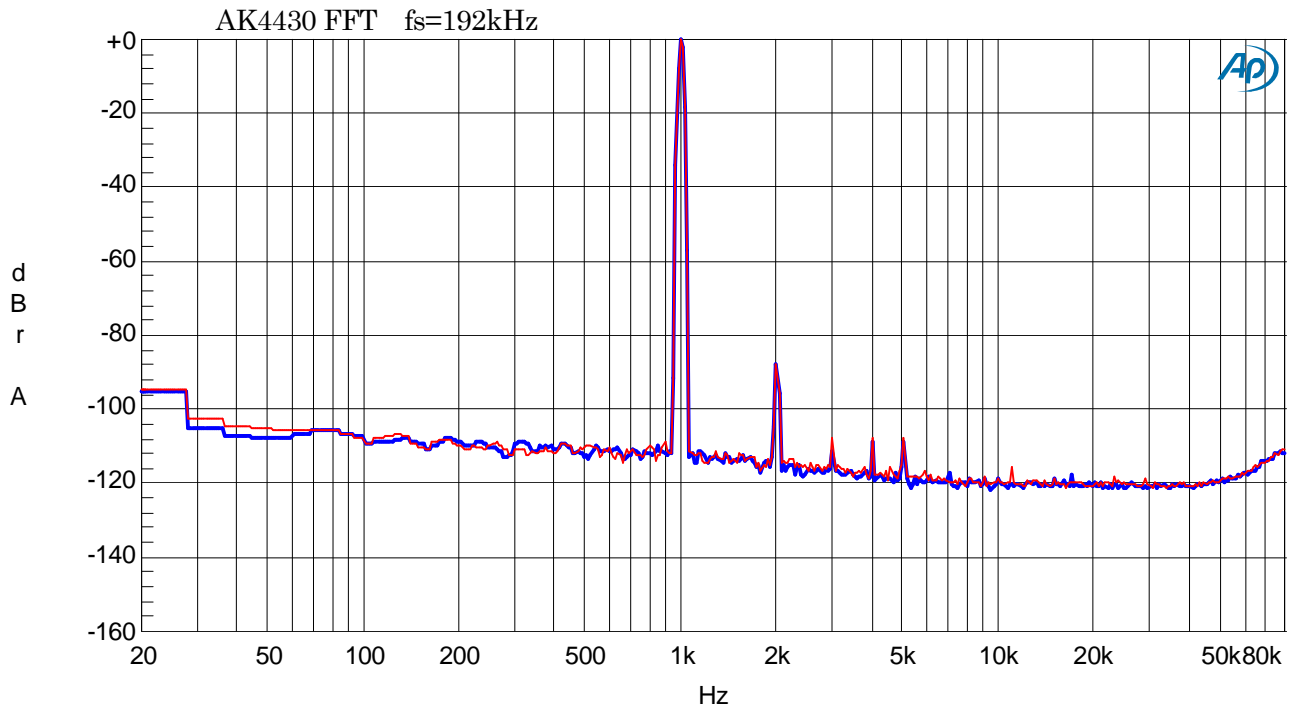


Figure 17.FFT (0dBFS Input, fin=1kHz)

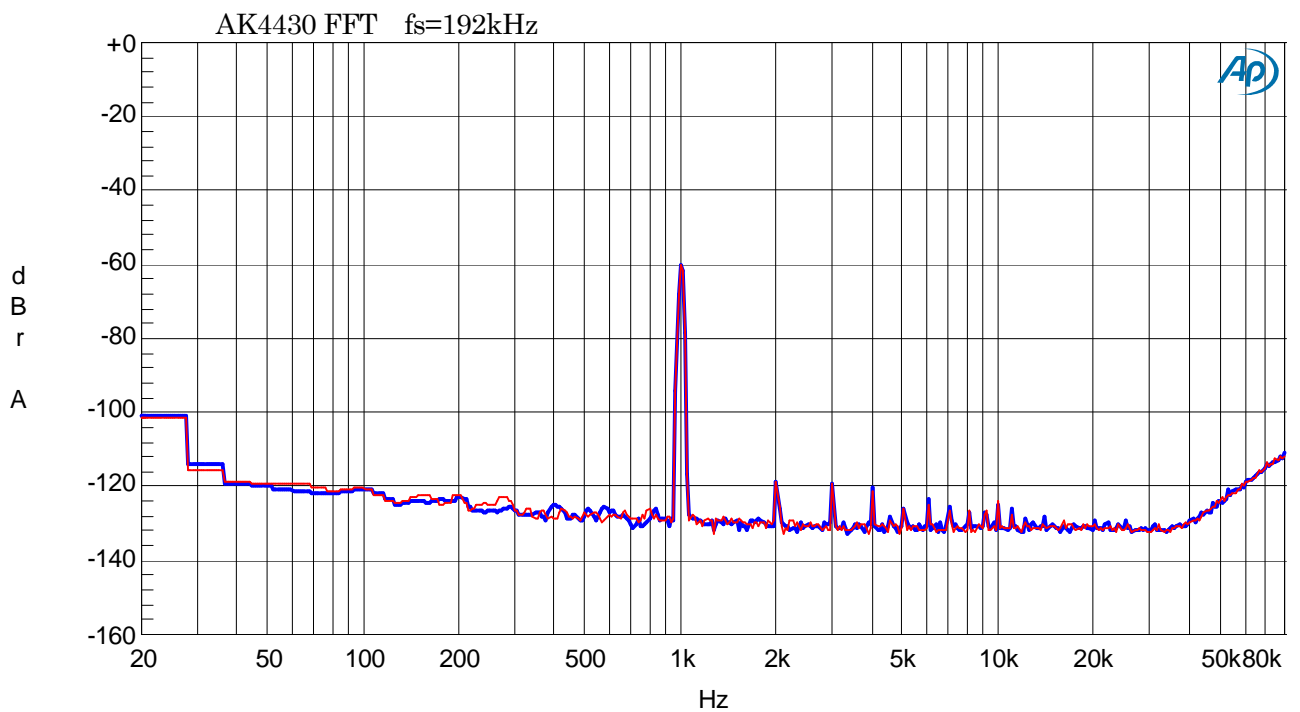


Figure 18.FFT (-60dBFS Input, fin=1kHz)

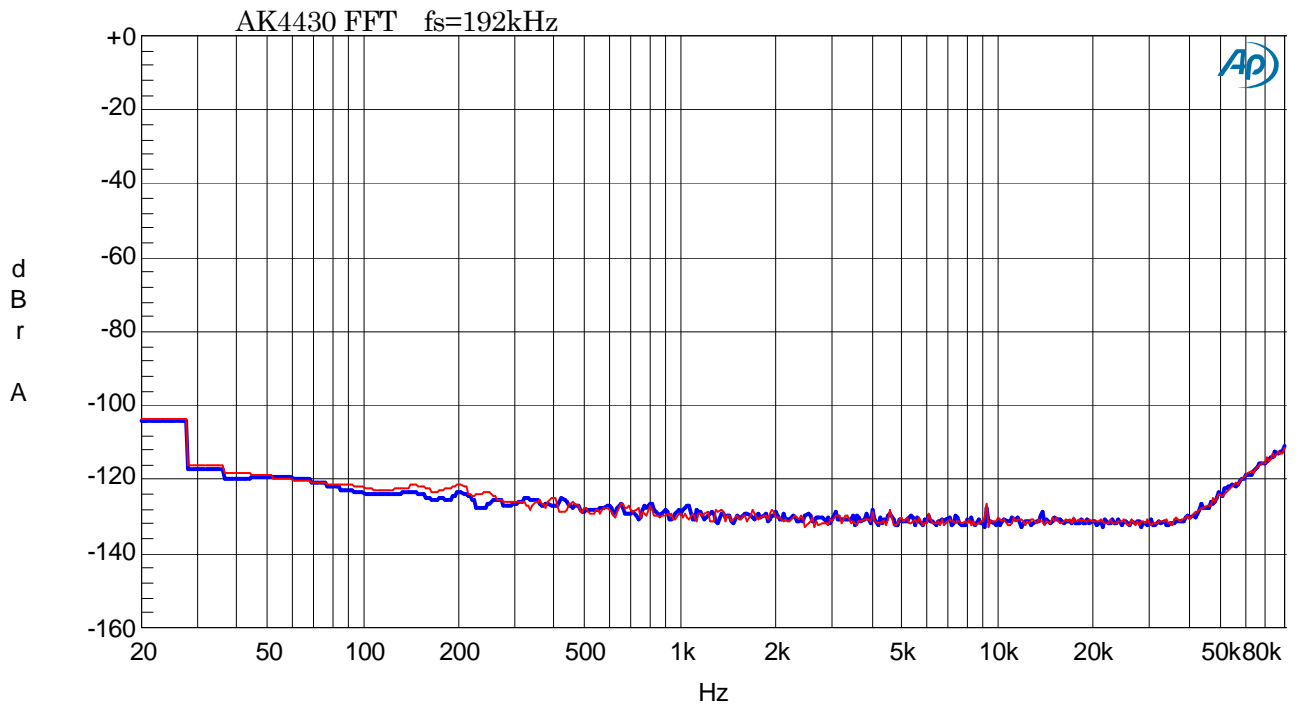


Figure 19.FFT (No Signal)

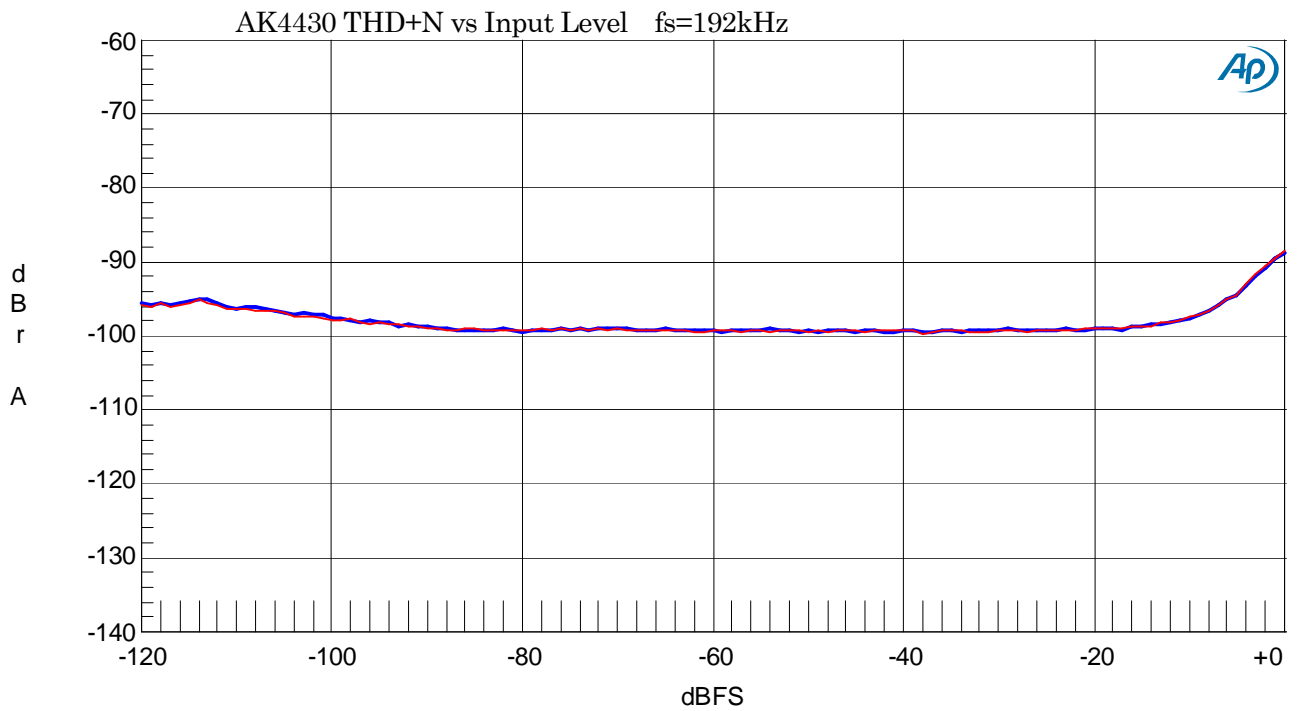


Figure 20.TH D+N vs Input Level (fin=1kHz)

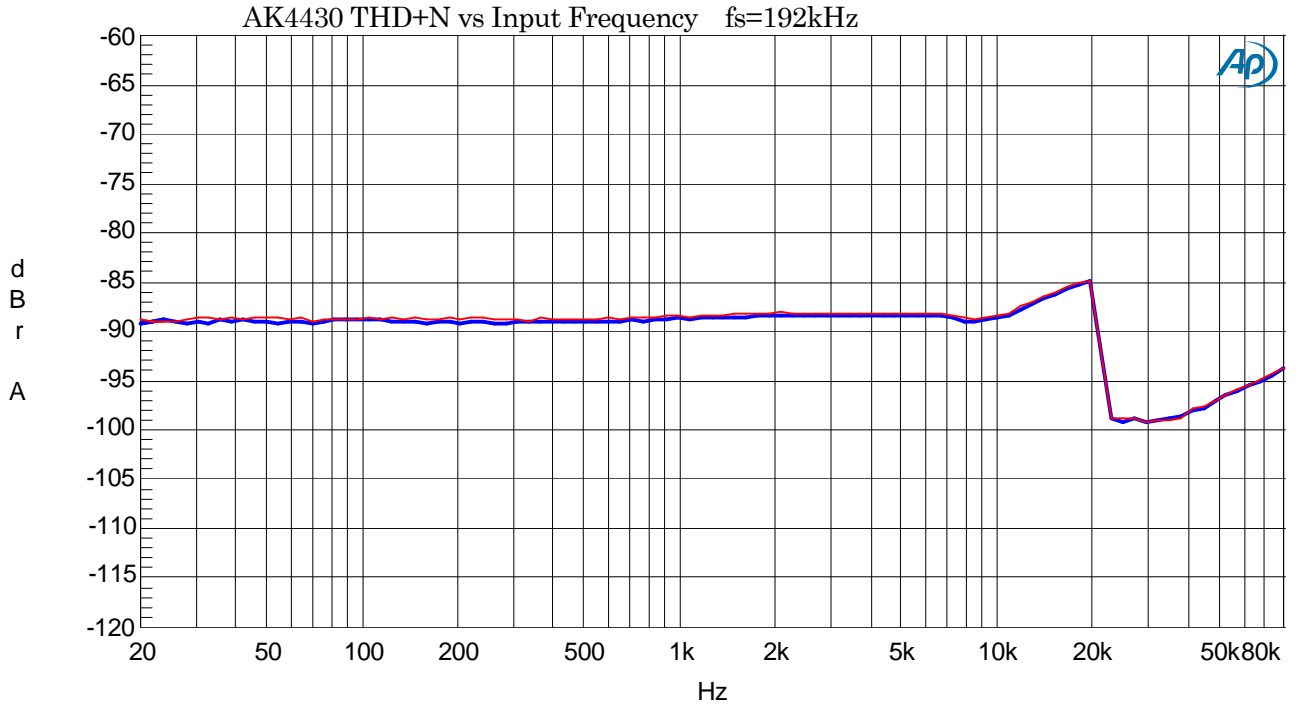


Figure 21. THD+N vs Input Frequency (0dB Input)

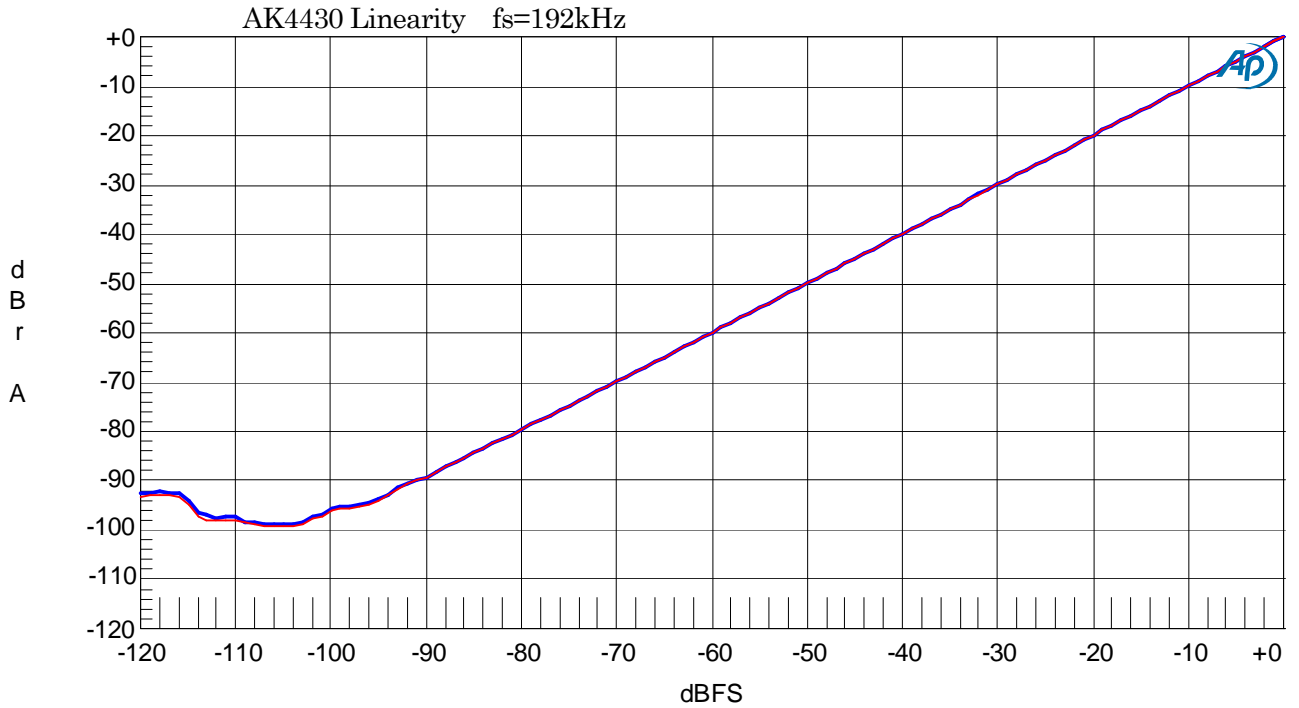


Figure 22. Linearity (fin=1kHz)

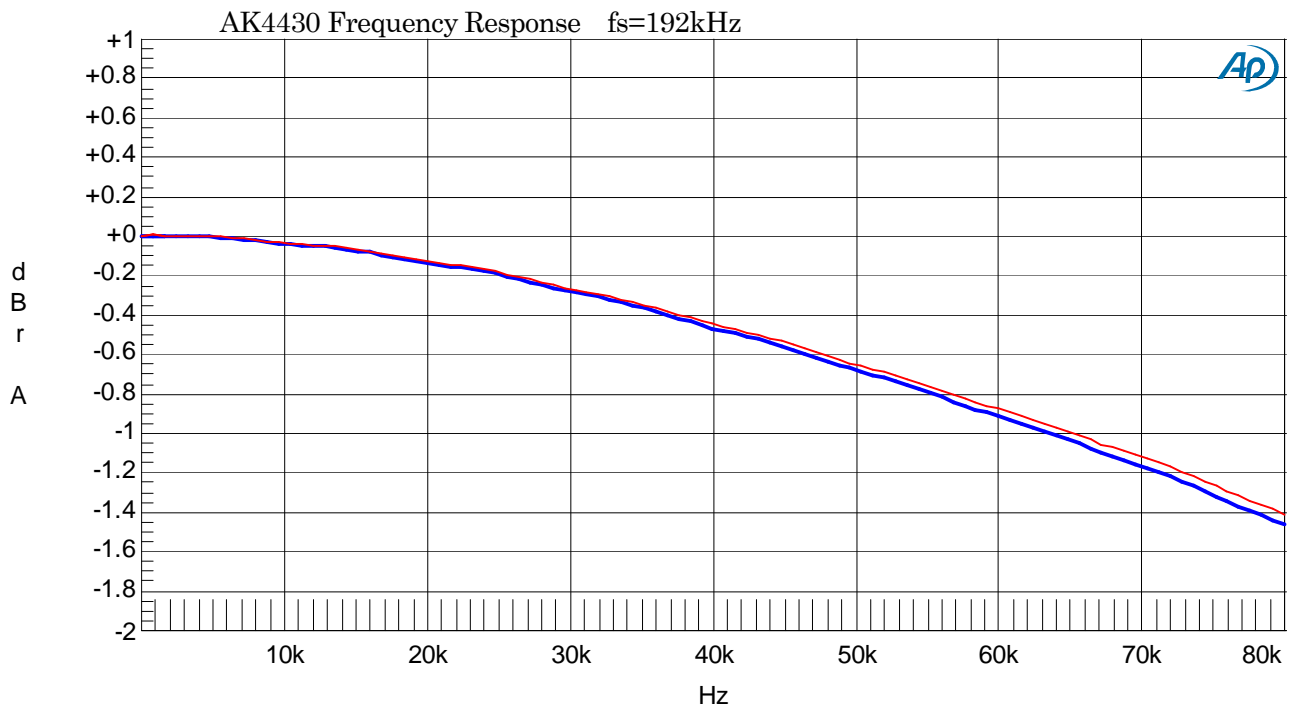


Figure 23. Frequency Response (0dBFS Input)

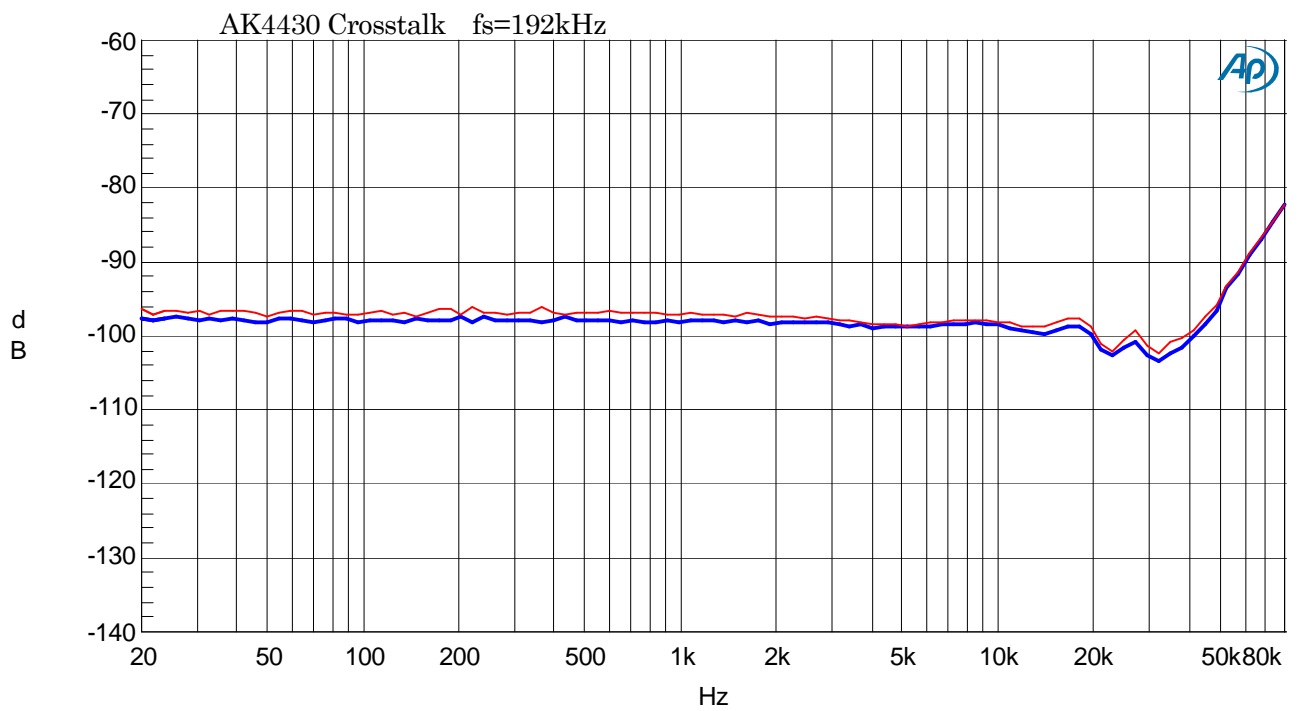


Figure 24. Crosstalk (0dBFS Input)

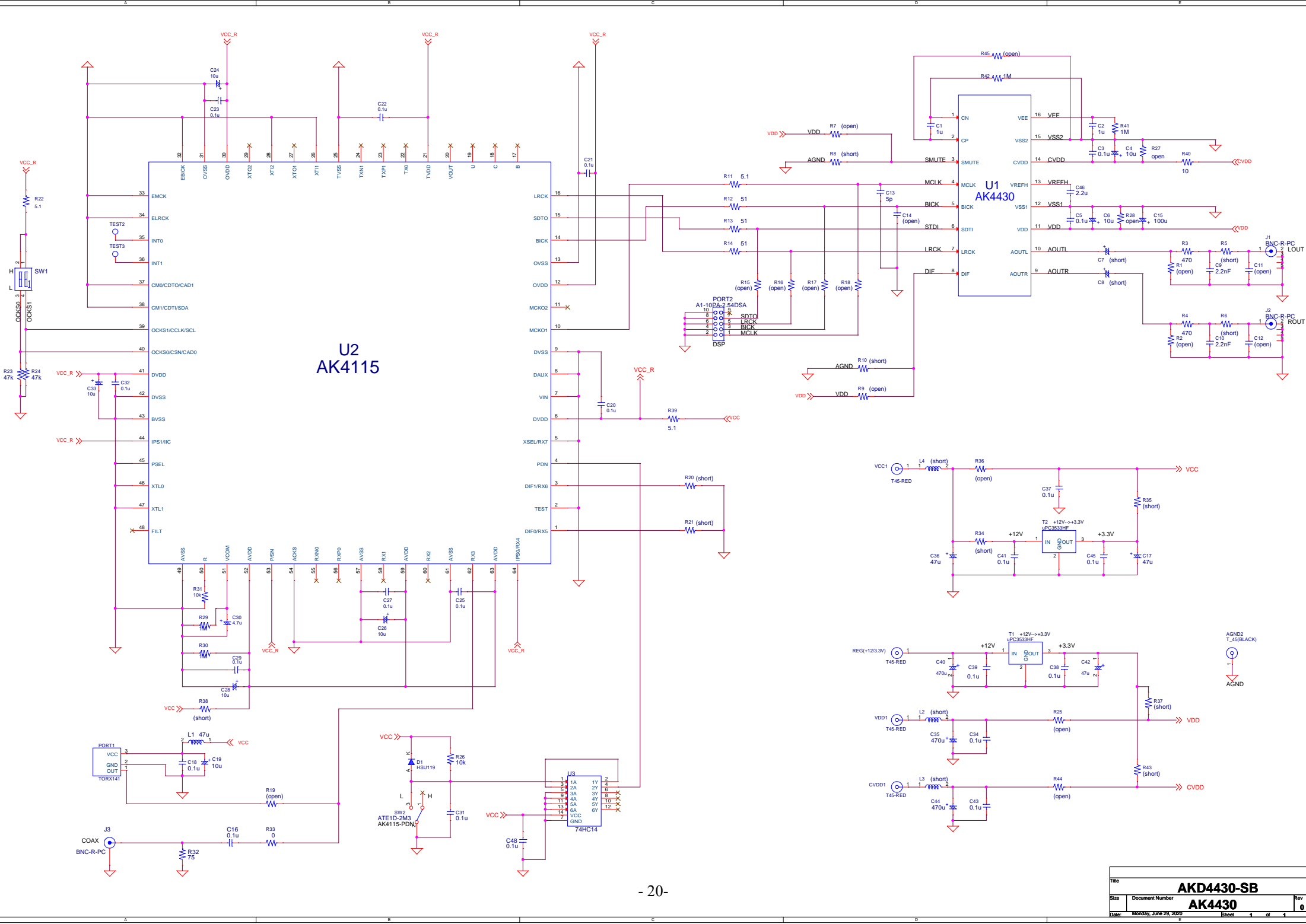
REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
20/06/12	KM134700	0	First Edition	-	
20/06/29	KM134701	0	addition	-	Schematic addition

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