AKD4430-SA is an evaluation board for AK4430 (192kHz sampling 24Bit Stereo ΔΣ DAC with 2Vrms Output). AKD4430-SA has a digital audio interface (AK4115) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4430.

**Ordering Guide**

AKD4430-SA ---- AK4430 Evaluation Board

**Function**

- On-board digital audio interface. (AK4115)

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**Figure 1.** AKD4430-SA Block diagram

(* Circuit diagram are attached at the end of this manual.*)
## Comment

1. **LOUT, ROUT (BNC-JACK)**
   - It is analog signal output Jack. The signal is output from LOUT/ROUT pins.

2. **COAX, PORT1, PORT2 (Digital signal connector)**
   - **COAX (BNC-JACK):** Digital signal (SPDIF, Fs: 24\textasciitilde 48kHz) is input to the AK4115. (Default)
   - **PORT1 (Optical Connecter):** Optical digital signal (SPDIF, Fs: 32\textasciitilde 48kHz) is input to the AK4115.
   - **PORT2 (10 pin header):** The clock and data can be input and output with this connector.

3. **REG, VDD, AGND, CVDD, VCC**
   - These are the power supply connectors. Connect power supply with these pins.
   - As for the detail comments, refer to the setup of power supply in P3.

4. **SW1, SW2 (Switch)**
   - **SW1:** Setting of frequency of MCKO that is output from AK4115.
   - **SW2:** Reset of AK4115. Keep “H” during normal operation.
Operation sequence

1) Set up the power supply lines.
   Each supply line should be distributed from the power supply unit.

<table>
<thead>
<tr>
<th>Name of jack (Note 1)</th>
<th>Color of jack</th>
<th>Typ Voltage</th>
<th>Voltage Range</th>
<th>Using</th>
<th>Default Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC1</td>
<td>Red</td>
<td>+12V</td>
<td>+7V~+15V</td>
<td>AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit (Regulator:T2)</td>
<td>Connected to +12V</td>
</tr>
<tr>
<td>VDD1</td>
<td>Red</td>
<td>+3.3V</td>
<td>+3V~+3.6V</td>
<td>VDD of AK4430</td>
<td>Open</td>
</tr>
<tr>
<td>CVDD1</td>
<td>Red</td>
<td>+3.3V</td>
<td>+3V~+3.6V</td>
<td>CVDD of AK4430</td>
<td>Open</td>
</tr>
<tr>
<td>AGND2</td>
<td>Black</td>
<td>0V</td>
<td>0V</td>
<td>Ground</td>
<td>Connected to GND (Should be connected)</td>
</tr>
<tr>
<td>REG (Note 2)</td>
<td>Red</td>
<td>+12V</td>
<td>+7V~+15V</td>
<td>VDD, CVDD of AK4430 (Regulator:T1)</td>
<td>Connected to +12V</td>
</tr>
</tbody>
</table>

Note 1) In case of using +3.3V power supply to connect VCC1, It is possible to supply the voltage to AK4115 and the Logic circuit without using Regulator.
In this case, change to R36: Open ➔ Short (0 Ω); R34,R35: Short (0 Ω) ➔ Open

Note 2) In case of using +12V power supply to connect REG, Use regulator: T1 can supply AK4430 with clean voltage. (Default)
In this case, change to R25,R44: Short (0 Ω) ➔ Open; R37,R43:Open ➔ Short (0 Ω); VDD, CVDD should be open.

2) DIP Switch setting:
   Refer to Table 2 and Table 3

3) Power Down:
   The AK4115 should be reset once by bringing SW2 (AK4115 PDN) “L” upon power-up.

Evaluation mode

1. Using DIR (Optical Link)
   The DIR generates MCLK, BCK, LRCK and SDATA from the received data through optical connector (PORT1: TORX141). It is possible to evaluate the AK4430 by using CD disk.
   Setting: R19: Open ➔ 470 Ω; R33: short (0 Ω) ➔ Open

2. Using DIR (COAX) (Default)
   The DIR generates MCLK, BCK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4430 by using CD disk.
   Setting: R19: Open; R33: short (0 Ω); (Default)
   ※ COAX is recommended for an evaluation of the Sound quality.

3. Supply all interface signals that include master clock via PORT2 from external equipments..
   Setting: R11: 5.1Ω ➔ Open
   R12, R13, R14: 51Ω ➔ Open
   R15, R16, R17, R18: Open ➔ 51Ω or short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.
### Setting of DIP switch

**[SW1]: AK4115 setting**

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>OFF (“L”)</th>
<th>ON (“H”)</th>
<th>Defaultの状態</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OCKS0</td>
<td>AK4115’s Master Clock setting</td>
<td>Look Table 3</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>OCKS1</td>
<td></td>
<td></td>
<td>H</td>
</tr>
</tbody>
</table>

Table 2. SW1 setting

<table>
<thead>
<tr>
<th>OCKS1</th>
<th>OCKS0</th>
<th>MCLK Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0/1</td>
<td>256fs @ fs=96kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>512fs @ fs=48kHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>128fs @ fs=192kHz</td>
</tr>
</tbody>
</table>

Default

Table 3. MCLK clock setting

### Setting of SW2 switch

**[SW2](PDN): Reset of AK4115. Keep “H” during normal operation.**
Measurement Results

[Measurement condition]
- Measurement unit: Audio Precision System two Cascade (AP2)
- MCLK: 512fs, 256fs, 128fs
- BCK: 64fs
- fs: 44.1kHz, 96kHz, 192kHz
- Bit: 24bit
- Power Supply: VDD=CVDD=3.3V
- Interface: DIR
- Temperature: Room

Table Data

**fs=44.1kHz**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input signal</th>
<th>Measurement filter</th>
<th>Lch</th>
<th>Rch</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/(N+D)</td>
<td>1kHz, 0dB</td>
<td>20kLPF</td>
<td>91.8</td>
<td>92.2</td>
</tr>
<tr>
<td>DR</td>
<td>1kHz, -60dB</td>
<td>20kLPF SPCL, A-weighted</td>
<td>104.5</td>
<td>104.5</td>
</tr>
<tr>
<td>S/N</td>
<td>“0” data</td>
<td>20kLPF SPCL, A-weighted</td>
<td>104.7</td>
<td>104.7</td>
</tr>
</tbody>
</table>

**fs=96kHz**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input signal</th>
<th>Measurement filter</th>
<th>Lch</th>
<th>Rch</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/(N+D)</td>
<td>1kHz, 0dB</td>
<td>40kLPF</td>
<td>91.4</td>
<td>91.9</td>
</tr>
<tr>
<td>DR</td>
<td>1kHz, -60dB</td>
<td>40kLPF SPCL, A-weighted</td>
<td>104.4</td>
<td>104.4</td>
</tr>
<tr>
<td>S/N</td>
<td>“0” data</td>
<td>40kLPF SPCL, A-weighted</td>
<td>104.6</td>
<td>104.6</td>
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</tbody>
</table>

**fs=192kHz**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input signal</th>
<th>Measurement filter</th>
<th>Lch</th>
<th>Rch</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/(N+D)</td>
<td>1kHz, 0dB</td>
<td>40kLPF</td>
<td>89.5</td>
<td>89.9</td>
</tr>
<tr>
<td>DR</td>
<td>1kHz, -60dB</td>
<td>40kLPF SPCL, A-weighted</td>
<td>104.0</td>
<td>103.9</td>
</tr>
<tr>
<td>S/N</td>
<td>“0” data</td>
<td>40kLPF SPCL, A-weighted</td>
<td>104.5</td>
<td>104.4</td>
</tr>
</tbody>
</table>
Plot Data

fs=44.1kHz

![AK4430 FFT](image)

Figure 3. FFT (0dB Input, fin=1kHz)

![AK4430 FFT](image)

Figure 4. FFT (-60dB Input, fin=1kHz)
Figure 5. FFT (No Signal)

Figure 6. FFT (Out of Band Noise)
AK4430 THD+N vs Input Level
fs=44.1kHz

Figure 7. THD + N vs Input Level (fin=1kHz)

AK4430 THD+N vs Input Frequency
fs=44.1kHz

Figure 8. THD + N vs Input Frequency (0dB Input)
Figure 9. Linearity (fs=44.1kHz)

Figure 10. Frequency Response (0dB Input)
Figure 11. Crosstalk (0dB Input)

Figure 12. FFT (0dB Input, fin=1kHz)
Figure 13. FFT (-60dB Input, fin=1kHz)

Figure 14. FFT (No Signal)
AK4430 THD+N vs Input Level
fs=96kHz

Figure 15. THD+N vs Input Level (fin=1kHz)

AK4430 THD+N vs Input Frequency
fs=96kHz

Figure 16. THD+N vs Input Frequency (0dB Input)
Figure 17. Linearity (fin=1kHz)

Figure 18. Frequency Response (0dB Input)
Figure 19. Crosstalk (0dB Input)

Figure 20. FFT (0dB Input, fin=1kHz)
Figure 21. FFT (-60dB Input, fin=1kHz)

Figure 22. FFT (No Signal)
AK4430 THD+N vs Input Level
fs=192k

Figure 23. THD+N vs Input Level (fin=1kHz)

AK4430 THD+N vs Input Frequency
fs=192kHz

Figure 24. THD+N vs Input Frequency (0dB Input)
Figure 25. Linearity (fin=1kHz)

Figure 26. Frequency Response (0dB Input)
AK4430 Crosstalk
fs=192kHz

Figure 27. Crosstalk (0dB Input)
**REVISION HISTORY**

<table>
<thead>
<tr>
<th>Date</th>
<th>Manual Revision</th>
<th>Board Revision</th>
<th>Reason</th>
<th>Page</th>
<th>Contents</th>
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<td>09/11/04</td>
<td>KM101700</td>
<td>0</td>
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<tr>
<td>10/04/13</td>
<td>KM101701</td>
<td>1</td>
<td>Modification</td>
<td>5-18</td>
<td>Update of measurement results and Plots.</td>
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