AK4490R
Quality Oriented 32-Bit 2ch DAC

1. General Description
The AK4490R is a new generation Premium 32-bit 2ch DAC with new technologies, achieving industry’s leading level low distortion characteristics and wide dynamic range. The AK4490R integrates a newly developed switched capacitor filter “OSR Doubler”, making it capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4490R has five types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4490R accepts up to 768kHz PCM data and 11.2MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in network audios and USB-DACs.

Application: AV Receivers, CD/SACD player, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, Car Audios, Automotive External Amplifiers, Measurement Equipment, Control Systems, Public Audios (PA), Smart Cellular Phones, IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems

2. Features
- THD+N: -112dB
- DR, S/N: 120dB (2Vrms), 123dB (Mono Mode)
- 256 Times Over Sampling
- Sampling Rate: 8kHz ~ 768kHz
- 32-bit 8x Digital Filter
  - Short Delay Sharp Roll-off, GD = 6.0/fs,
  - Short Delay Slow Roll-off, GD = 5.0/fs
  - Sharp Roll-off
  - Slow Roll-off
  - Low Dispersion Short Delay Filter
  - Super Slow Roll-off
- High Tolerance to Clock Jitter
- Low Distortion/ Low Noise High Performance Differential Amplifier Output
- DSD64, DSD128, DSD256 Input Support
  - Filter1 (fc = 39kHz, DSD64 mode), Filter2 (fc = 76kHz, DSD64 mode)
- Digital De-emphasis for 32, 44.1 and 48kHz sampling
- Soft Mute
- Digital Attenuator (255 levels and 0.5dB step + mute)
- Mono Mode
- External Digital Filter Interface
- Audio I/F Format: 24/32 bit MSB justified, 16/20/24/32 bit LSB justified, I²S, DSD, TDM
- Master Clock
  - 8kHz ~ 32kHz: 256fs or 384fs or 512fs or 768fs or 1152fs
  - 32kHz ~ 54kHz: 256fs or 384fs or 512fs or 768fs
  - 54Hz ~ 108kHz: 256fs or 384fs
  - 108kHz ~ 216kHz: 128fs or 192fs
  - 216kHz ~ 388kHz: 32fs or 48fs or 64fs or 96fs
  - 388kHz ~ 776kHz: 16fs or 32fs or 48fs or 64fs
- 3-wire, I²C-bus Register Control Interface, or Pin Control
- Power Supply:
  - TVDD = AVDD = 3.0 ~ 3.6V (by internal LDO), VDDL/R = 4.75 ~ 5.25V
  - TVDD = AVDD = DVDD ~ 3.6V (by external supply), DVDD = 1.7V ~ 1.98V
  - VDDL/R = 4.75 ~ 5.25V
• Operational Temperature: -40 ~ 85 °C
• Digital Input Level: CMOS
• Package: 48-pin LQFP
Figure 1. Block Diagram

<table>
<thead>
<tr>
<th>Block</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM Data Interface</td>
<td>Execute serial/parallel conversion of SDATA input data by synchronizing with LRCK and BICK and generate TDM output data.</td>
</tr>
<tr>
<td>DSD Data Interface</td>
<td>1-bit data that is input from DSDL and DSDR pins is received by synchronizing with DCLK.</td>
</tr>
<tr>
<td>DSD Filter</td>
<td>FIR filter that reduces high frequency noise of DSD input data.</td>
</tr>
<tr>
<td>DATT, Soft Mute</td>
<td>Apply DATT and Soft Mute process to input data.</td>
</tr>
<tr>
<td>De-emphasis &amp; Interpolator</td>
<td>A digital filter that applies De-emphasis process to input data and executes over sampling.</td>
</tr>
<tr>
<td>ΔΣ Modulator</td>
<td>Output multi-bit data to SCF. This block consists of a third-order digital delta-sigma modulator.</td>
</tr>
<tr>
<td>SCF</td>
<td>Convert multi bit output of ΔΣ Modulator into analog signal. This block consists of the switched capacitor DAC</td>
</tr>
<tr>
<td>Control Register</td>
<td>Keep register settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I2C-Bus (SCL, SDA) control mode.</td>
</tr>
<tr>
<td>Clock Divider</td>
<td>Divide Master Clock. In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.</td>
</tr>
<tr>
<td>MCLK Stop Detection</td>
<td>It is the detection circuit of MCLK input or no input.</td>
</tr>
<tr>
<td>Bias, Vref</td>
<td>It outputs common voltage VCML/R that is generated by reference voltage VREFHL/R and VREFLL/R.</td>
</tr>
<tr>
<td>LDO</td>
<td>It is the power supply circuit for internal digital circuit. Its power supply voltage is typical 1.8V.</td>
</tr>
</tbody>
</table>
4. Package

■ Outline Dimensions (48-pin LQFP)

![Diagram of package dimensions]

■ Material & Terminal Finish

- **Package Molding Compound:** Epoxy, Halogen (Br and Cl) free
- **Lead Frame Material:** EFTEC-64T
- **Terminal Surface Treatment:** Solder (Pb free) plate
1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4490REQ
4) AKM Logo
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