AKD7719B-A

AK7719B Evaluation Board Rev.0

GENERAL DESCRIPTION

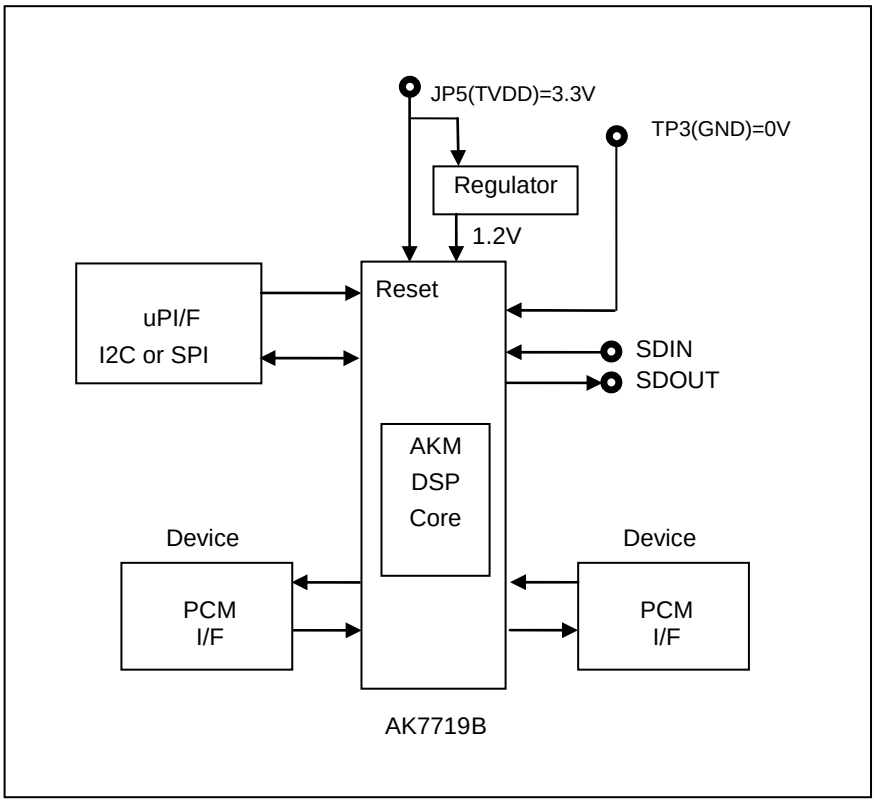
The AKD7719B-A is an evaluation kit for the AK7719B; a digital signal processor (DSP) with digital interface ports. The built-in asynchronous sample rate converters (SRC) enable flexible connectivity in various system configurations. It realizes an easy evaluation of the audio system by just connecting to the target product via digital input and output pins. A USB connection is adopted for control interface, enabling to develop DSP codes with a PC.

■ Ordering Guide

AKD7719B-A --- Evaluation board for AK7719B
(Main-board：AKD7719B-A-MAIN , Sub-board：AKD7719B-A-SUB)
USB Control Box
Control Software

FUNCTION

☐ Write/Read RAM: Access to PRAM, CRAM, OFFRAM and Registers
☐ Digital Audio Interface
- Test pin header

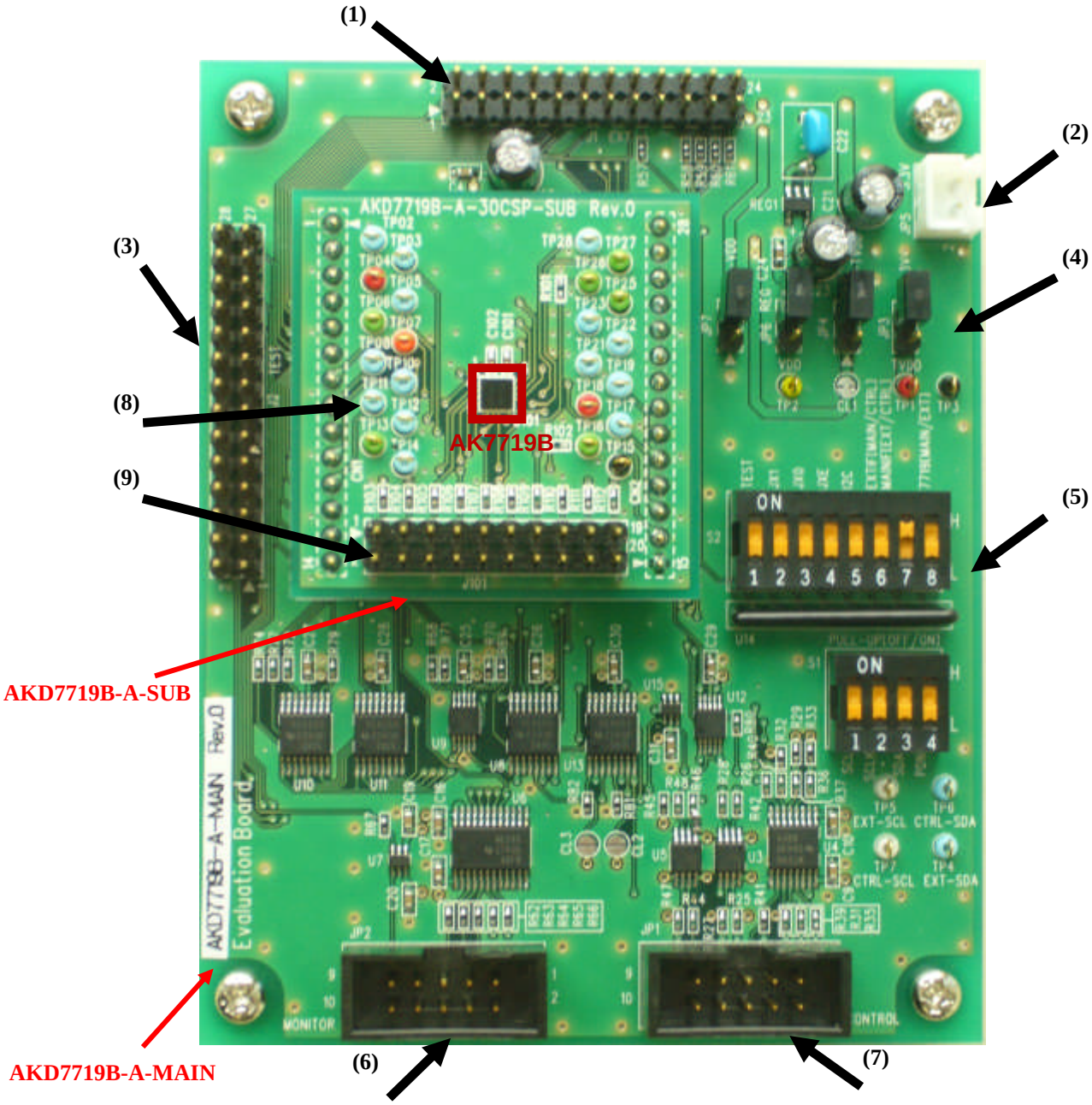


AKD7719B-A-MAIN + AKD7719B-A-SUB

Figure 1. AKD7719B-A Block Diagram

EVALUATION BORAD

■ Board View



AKD7719B-A-MAIN + AKD7719B-A-SUB

Figure 2. AKD7719B-A Board View

■ Description

AKD7719B-A-MAIN

No.	Name	Function
(1)	EXT (J1) (24 pin Header)	External System Signal Connector.
(2)	3.3V (JP5)	3.3V Power Supply Terminal. Use attached connection cable.
(3)	TEST (J2) (28 pin Header)	External System Connector
(4)	Jumper (JP3, JP4, JP6, JP7)	Power Supply Select Jumper
(5)	DIP Switch (S1, S2)	Pin and Signal Select Switches
(6)	MONITOR (JP2) (10 pin Header)	AKD77XX-HFS MONITOR Board Connector. (for HF Tuning)
(7)	CONTROL (JP1) (10 pin Header)	USB Control Box Connector
(8)	TEST (TP02-TP28) (Test pin Header)	External System Connector and Monitor Pin (on Sub-Board)
(9)	EXT (J101) (20 pin Header)	External System Connector (on Sub-Board)

AKD7719B-A-MAIN

EXT(24 / 27 pin Header) Pin Layout

・24pin Pin Header [J1] :

Pin No.	Name	I/O	Function
1	EXT-BCLK1	I	These pins are connected to the AK7719B via Buffer Level Shifter
2	EXT-JX0/BCLK3	I/O	
3	EXT-SYNC1	I	
4	EXT-JX1/SYNC3	I/O	
5	EXT-SDIN1	I	
6	EXT-SDIN3	I/O	
7	EXT-SDOUT1	O	
8	EXT-SDOUT3/GP0	I/O	
9	EXT-BCLK2	O	
10	EXT-SDIN4	I	
11	EXT-SYNC2	O	
12	EXT-SDOUT4/GP1	I/O	
13	EXT-SDIN2	I	
14	EXT-STO/RDY	O	
15	EXT-SDOUT2	O	
16	EXT-PDN	I/O	
17	EXT-CSN/SCL	I/O	This pin is used when controlling the AK7719B via EXT. Refer to DIPSW Setting
18	open	-	
19	EXT-SO/SDA	I/O	This pin is used when controlling the AK7719B via EXT. Refer to DIPSW Setting
20	GND	-	GND
21	EXT-SCLK/CAD0	I/O	This pin is used when controlling the AK7719B via EXT. Refer to DIPSW Setting
22	EXT-VDD+1.2V	O	This pin is used for VDD supply via EXT. Refer to JP Setting
23	EXT-SI/CAD1	I/O	This pin is used when controlling the AK7719B via EXT. Refer to DIPSW Setting
24	EXT-TVDD	O	This pin is used for TVDD supply via EXT. Refer to JP Setting

・27pin Pin Header [J2] :

Pin No.	Name	I/O	Function
1	EXT-BCLK1	I	These pins are connected to the AK7719B via Buffer Level Shifter
2	GND	-	
3	EXT-SYNC1	I	
4	GND	-	
5	EXT-SDIN1	I	
6	GND	-	
7	EXT-SDOUT1	O	
8	GND	-	
9	EXT-BCLK2	O	
10	GND	-	
11	EXT-SYNC2	O	
12	GND	-	
13	EXT-SDIN2	I	
14	GND	-	
15	EXT-SDOUT2	O	
16	GND	-	
17	EXT-JX0/BCLK3	I/O	
18	GND	-	
19	EXT-JX1/SYNC3	I/O	
20	GND	-	
21	EXT-SDIN3	I/O	
22	GND	-	
23	EXT-SDOUT3/GP0	I/O	
24	GND	-	
25	EXT-SDIN4	I	
26	GND	-	
27	EXT-SDOUT4/GP1	I/O	

AKD7719B-A-SUB (AKD7719B-A-30CSP-SUB)

EXT(20pin Header) Pin / TEST Pin Layout

・20pin Pin Header [J101] :

Pin No.	Name	I/O	Function
1	SYNC2-I	I	These pins are connected to the AK7719B.
2	GND	-	
3	BCLK2-I	I	
4	GND	-	
5	SYNC4-I	I	
6	GND	-	
7	BCLK4-I	I	
8	GND	-	
9	SYNC5-O	O	
10	GND	-	
11	SYNC5-I	I	
12	GND	-	
13	BCLK5-O	O	
14	GND	-	
15	BCLK5-I	I	
16	GND	-	
17	SDIN5-I	I	
18	GND	-	
19	SDOUT5-O	O	
20	GND	-	

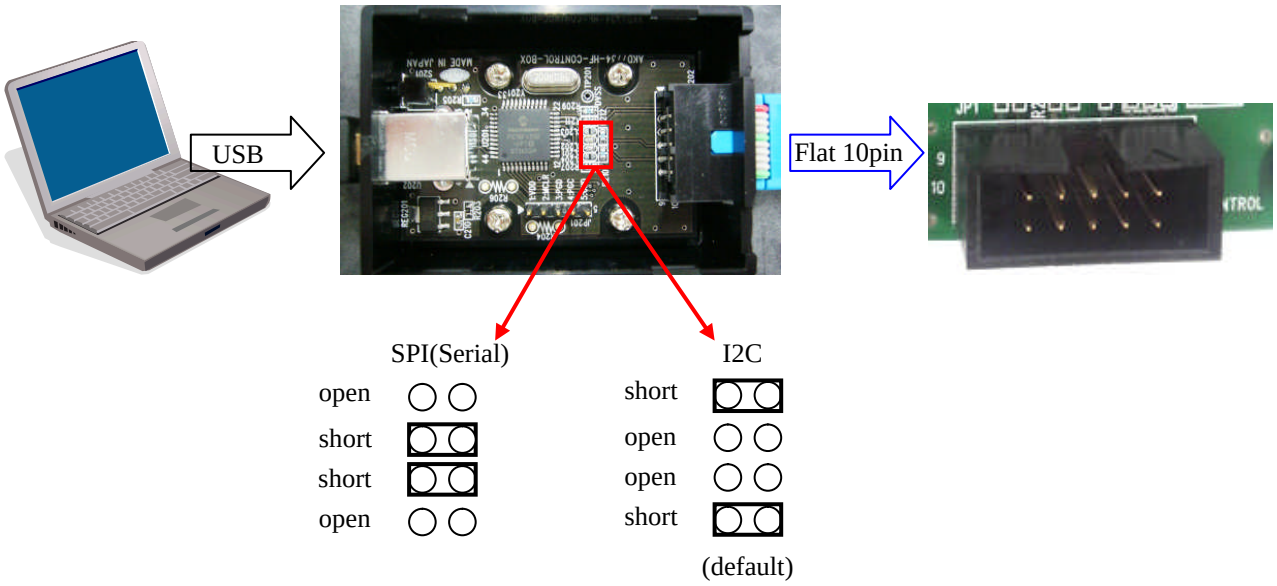
・TEST Pin Header [TP02 – TP28] :

Pin No.	Name	I/O	Function
02	SYNC3/JX1-I	I	These pins are connected to the AK7719B.
03	SDIN2-I	I	
04	TVDD	-	
05	SDIN4-I	I	
06	SDOUT2-O	O	
07	SO/SDA-IO	I/O	
08	SCLK/CAD0-I	I	
10	CSN/SCL-I	I	
11	SI/CAD1-I	I	
12	I2C-I	I	
13	SDOUT4/GP1/STO /RDY-O	O	
14	TEST-I	I	
15	VSS	-	
16	BCLK2-O	O	
17	BCLK3/JX0-I	I	
18	VDD	-	
19	SYNC1-I	I	
21	BCLK1-I	I	
22	PDN-I	I	
23	SDIN1-I	I	
25	SDOUT1-O	O	
26	SYNC2-O	O	
27	SDOUT3/GP0-O	O	
28	SDIN3-I	I	

■ Control Box

The AKD7719B-A should be connected to a PC via an USB control box. The USB control box is connected to a PC with an USB cable and the AKD7719B-A with 10-pin flat cable.

Set jumper pins to select control I/F (I2C or SPI).



The switch of I2C labeled on S2 should be set when changing SPI/I2C.

■ Operation Sequence

AKD7719B-A-MAIN

(1) Jumper and Test Pin Setting (near the Power Supply)

Name	Setting	Using	Default Setting
JP3 3.3V	Open	External TVDD supply on TP1	Short
	Short	TVDD = 3.3V fixed	
JP4 EXT-TVDD	Open	External TVDD supply on the 24pin of J1. (JP3: not connected)	Open
	Short	EXT-TVDD = TVDD	
JP6 REG	Open	External VDD input supply VDD on TP2	Short
	Short	VDD+1.2V fixed	
JP7 EXT-VDD	Open	VDD = JP6(REG)	Open
	Short	External VDD supply on the 22pin of J1. (JP6: not connected)	

Table 1. Jumper Pin Setting

Name	Color	Typ Voltage	Voltage Range	Using
TP1 TVDD	Red	+3.3V	+1.6~+3.6V	TVDD of AK7719
TP2 VDD	Yellow	+1.2V	+1.1~+1.3V	VDD of AK7719
TP3 GND	Black	0V	0V	Ground

Table 2. Test Pin Setting

(2) CutLand Setting

Name	Setting	Using	Default Setting
CL1 7719-TVDD	Open	7719-TVDD independent supply	Short
	Short	7719-TVDD = TVDD	
CL2 CAD0	Open	CAD0 pin = L	Open
	Short	CAD0 pin = H	
CL3 CAD1	Open	CAD1 pin = L	Open
	Short	CAD1 pin = H	

Table 3. CutLand Setting

(3) DIP Switch Setting

		Name	Setting	Using		Default Setting
S1	8	7719[MAIN/EXT]	OFF(MAIN)	Default setting fixed.		OFF
			ON(EXT)			
	7	MAINIF[EXT/CTRL]	OFF(EXT)	Default setting fixed.		ON
			ON(CTRL)			
	6	EXTIF[MAIN/CTRL]	OFF(MAIN)	Default setting fixed.		OFF
			ON(CTRL)			
	5	I2C	OFF	I2C pin = "L"		OFF
			ON	I2C pin = "H"		
	4	JXE	OFF	DIPSW control of JX0/1 for the AK7719B(MAIN or EXT) is invalid.		OFF
			ON	DIPSW control of JX0/1 for the AK7719B(MAIN or EXT) is valid.		
	3	JX0	OFF	JX0 pin = "L"	Valid when JXE = ON	OFF
			ON	JX0 pin = "H"		
	2	JX1	OFF	JX1 pin = "L"		OFF
			ON	JX1 pin = "H"		
	1	TEST	OFF	TEST = "L"		OFF
			ON	TEST = "H"		
S2	1	PULL-UP[OFF/ON]	OFF	PULL-UP OPEN (CSN/SCL)		OFF
			ON	PULL-UP (CSN/SCL)		
	2	PULL-UP[OFF/ON]	OFF	PULL-UP OPEN (SCLK/CAD0)		
			ON	PULL-UP (SCLK/CAD0)		
	3	PULL-UP[OFF/ON]	OFF	PULL-UP OPEN (SO/SDA)		
			ON	PULL-UP (SO/SDA)		
	4	PULL-UP[OFF/ON]	OFF	PULL-UP OPEN (PDN)		
			ON	PULL-UP (PDN)		

Table 4. DIPSW Setting

Control Interface Setting

AK7719B	I/F	connection	DIP Switch				
			I2C	EXTIF	MAINIF	7719	
MAIN on board	I2C	CONTROL	ON	OFF	ON	OFF	
	SPI	CONTROL	OFF	OFF	ON	OFF	(default)
EXT * not on board	I2C	CONTROL	ON	ON	ON	ON	

(*: Used when controlling the AK7719B which is externally connected.)

(4) Set up connectors. (refer to Evaluation Mode)
(5) Power On.
(6) Run the control software (AK7719B.exe) and download the appropriate script file. (see script section)

■ Evaluation Mode

Refer to the AK7719B datasheet for audio interface format.

(1) Evaluation Port : Port#1 to Port#2 and Port#2 to Port#1
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	INPUT	Sub J101-1 SYNC2	1fs=8kHz
BCLK2	INPUT	Sub J101-3 BCLK2	64fs=512kHz
SDIN2	INPUT	J2-13 EXT-SDIN2	I^2S, 16bit data
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	Data Monitor
SYNC3	INPUT	Sub TP02 SYNC3	-
BCLK3	INPUT	Sub TP17 BCLK3	-
SDIN3	INPUT	Sub TP28 SDIN3	-
SDOUT3	OUTPUT	Sub TP27 SDOUT3	-
SYNC4	INPUT	Sub J101-5 SYNC4	-
BCLK4	INPUT	Sub J101-7 BCLK4	-
SDIN4	INPUT	J2-25 EXT-SDIN4	-
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	-
SYNC5	INPUT	Sub J101-11 SYNC5	-
BCLK5	INPUT	Sub J101-15 BCLK5	-
SDIN5	INPUT	Sub J101-17 SDIN5	-
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	-

(2) Evaluation Port : Port#1 to Port#3 and Port#3 to Port#1
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	INPUT	Sub J101-1 SYNC2	-
BCLK2	INPUT	Sub J101-3 BCLK2	-
SDIN2	INPUT	J2-13 EXT-SDIN2	-
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	-
SYNC3	INPUT	Sub TP02 SYNC3	1fs=8kHz
BCLK3	INPUT	Sub TP17 BCLK3	64fs=512kHz
SDIN3	INPUT	Sub TP28 SDIN3	I^2S, 16bit data
SDOUT3	OUTPUT	Sub TP27 SDOUT3	Data Monitor
SYNC4	INPUT	Sub J101-5 SYNC4	-
BCLK4	INPUT	Sub J101-7 BCLK4	-
SDIN4	INPUT	J2-25 EXT-SDIN4	-
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	-
SYNC5	INPUT	Sub J101-11 SYNC5	-
BCLK5	INPUT	Sub J101-15 BCLK5	-
SDIN5	INPUT	Sub J101-17 SDIN5	-
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	-

(3) Evaluation Port : Port#1 to Port#4 and Port#4 to Port#1
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	INPUT	Sub J101-1 SYNC2	-
BCLK2	INPUT	Sub J101-3 BCLK2	-
SDIN2	INPUT	J2-13 EXT-SDIN2	-
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	-
SYNC3	INPUT	Sub TP02 SYNC3	-
BCLK3	INPUT	Sub TP17 BCLK3	-
SDIN3	INPUT	Sub TP28 SDIN3	-
SDOUT3	OUTPUT	Sub TP27 SDOUT3	-
SYNC4	INPUT	Sub J101-5 SYNC4	1fs=8kHz
BCLK4	INPUT	Sub J101-7 BCLK4	64fs=512kHz
SDIN4	INPUT	J2-25 EXT-SDIN4	I^2S, 16bit data
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	Data Monitor
SYNC5	INPUT	Sub J101-11 SYNC5	-
BCLK5	INPUT	Sub J101-15 BCLK5	-
SDIN5	INPUT	Sub J101-17 SDIN5	-
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	-

(4) Evaluation Port : Port#1 to Port#5 and Port#5 to Port#1
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	INPUT	Sub J101-1 SYNC2	-
BCLK2	INPUT	Sub J101-3 BCLK2	-
SDIN2	INPUT	J2-13 EXT-SDIN2	-
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	-
SYNC3	INPUT	Sub TP02 SYNC3	-
BCLK3	INPUT	Sub TP17 BCLK3	-
SDIN3	INPUT	Sub TP28 SDIN3	-
SDOUT3	OUTPUT	Sub TP27 SDOUT3	-
SYNC4	INPUT	Sub J101-5 SYNC4	-
BCLK4	INPUT	Sub J101-7 BCLK4	-
SDIN4	INPUT	J2-25 EXT-SDIN4	-
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	-
SYNC5	INPUT	Sub J101-11 SYNC5	1fs=8kHz
BCLK5	INPUT	Sub J101-15 BCLK5	64fs=512kHz
SDIN5	INPUT	Sub J101-17 SDIN5	I^2S, 16bit data
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	Data Monitor

(5) Evaluation Port : Port#1 to Port#2 and Port#2 to Port#1, Port2=Master
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	OUTPUT	Sub J101-1 SYNC2	SYNC Monitor
BCLK2	OUTPUT	Sub J101-3 BCLK2	BCLK Monitor
SDIN2	INPUT	J2-13 EXT-SDIN2	I^2S, 16bit data
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	Data Monitor
SYNC3	INPUT	Sub TP02 SYNC3	-
BCLK3	INPUT	Sub TP17 BCLK3	-
SDIN3	INPUT	Sub TP28 SDIN3	-
SDOUT3	OUTPUT	Sub TP27 SDOUT3	-
SYNC4	INPUT	Sub J101-5 SYNC4	-
BCLK4	INPUT	Sub J101-7 BCLK4	-
SDIN4	INPUT	J2-25 EXT-SDIN4	-
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	-
SYNC5	INPUT	Sub J101-11 SYNC5	-
BCLK5	INPUT	Sub J101-15 BCLK5	-
SDIN5	INPUT	Sub J101-17 SDIN5	-
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	-

(6) Evaluation Port : Port#1 to Port#5 and Port#5 to Port#1, Port5=Master
Format : fs=8kHz, BCLK=64fs, I^2S 16bit data

	Condition	Name	Clocks
SYNC1	INPUT	J2-3 EXT-SYNC1	1fs=8kHz
BCLK1	INPUT	J2-1 EXT-BCLK1	64fs=512kHz
SDIN1	INPUT	J2-5 EXT-SDIN1	I^2S, 16bit data
SDOUT1	OUTPUT	J2-7 EXT-SDOUT1	Data Monitor
SYNC2	INPUT	Sub J101-1 SYNC2	-
BCLK2	INPUT	Sub J101-3 BCLK2	-
SDIN2	INPUT	J2-13 EXT-SDIN2	-
SDOUT2	OUTPUT	J2-15 EXT-SDOUT2	-
SYNC3	INPUT	Sub TP02 SYNC3	-
BCLK3	INPUT	Sub TP17 BCLK3	-
SDIN3	INPUT	Sub TP28 SDIN3	-
SDOUT3	OUTPUT	Sub TP27 SDOUT3	-
SYNC4	INPUT	Sub J101-5 SYNC4	-
BCLK4	INPUT	Sub J101-7 BCLK4	-
SDIN4	INPUT	J2-25 EXT-SDIN4	-
SDOUT4	OUTPUT	J2-27 EXT-SDOUT4	-
SYNC5	OUTPUT	Sub J101-11 SYNC5	SYNC Monitor
BCLK5	OUTPUT	Sub J101-15 BCLK5	BCLK Monitor
SDIN5	INPUT	Sub J101-17 SDIN5	I^2S, 16bit data
SDOUT5	OUTPUT	Sub J101-J19 SDOUT5	Data Monitor

CONTROL SOFTWARE MANUAL

■ Setup of the Evaluation Board and Control Software

(1) Power the AKD7719B-A evaluation board on and connect it with a USB control box.

(2) Connect the USB control box to a PC with a USB cable.
The USB control box will be recognized as HID (Human Interface Device). When it can not be recognized correctly (e.g., unknown device is connected), please push reset button [yellow] on the USB control box.

(3) Install AK7719B.exe to the PC. Then ready to evaluate.

The start-up image of control software is as below.

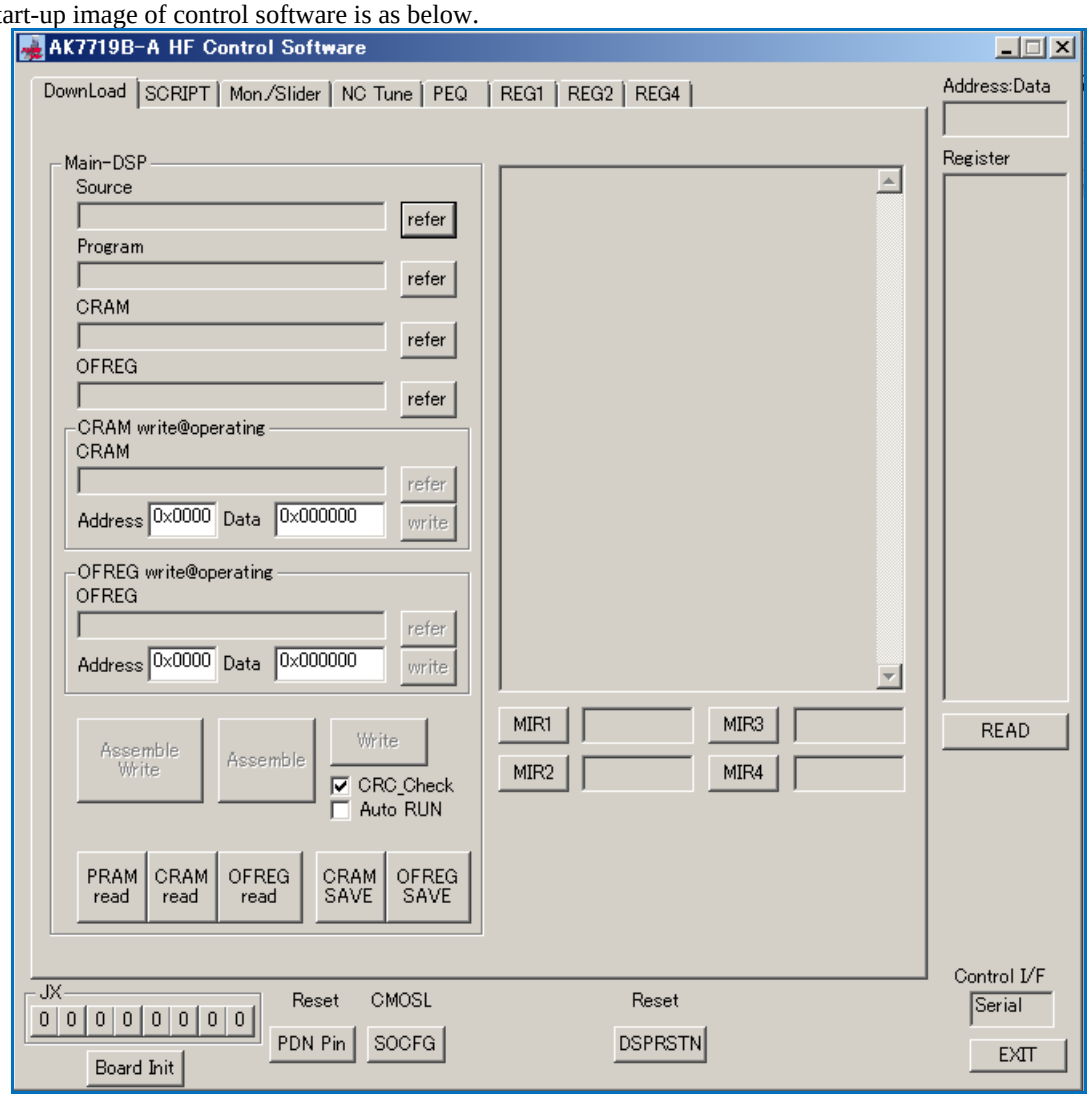


Figure 3. Start-up Image of Control Software (AK7719B_A_HF.exe)

(4) Push the “Board Init” button to make sure that this control software access registers. Only if just pushing the “PDN Pin” button this cannot access the registers.

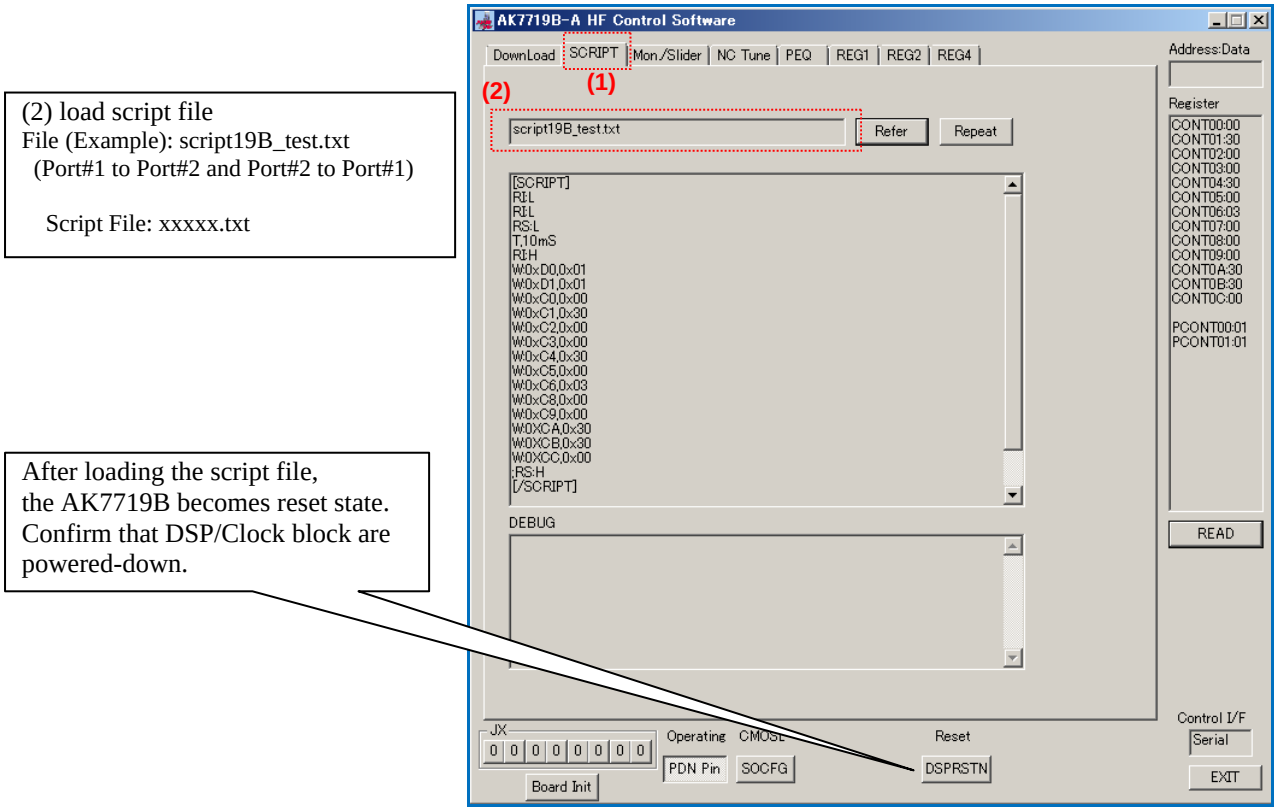
When the connection of PC with the USB control box is removed, it is required to restart the control software.

■ Download the DSP Program and Registers Software

1. Register Setting and Code Downloading

1-1. Register Setting

(1) Select the SCRIPT tab to set register values.



(2) “script19B_test.txt” runs under the condition below.
FSMode00: 8kHz / 16bit Linear / I2S

1-2. Code Downloading

There are four code areas as shown below.

Code Area	Alias	Function
Control Register	CONT	AK7719B operation mode setup
Program RAM	PRAM	Storage RAM for program code
Coefficient RAM	CRAM	Storage RAM for parameter used by program code
Offset Register	OFREG	Pointer for delay RAM address

Table 5. AK7719B Code Area

(Note 1) All codes (CONT, PRAM, CRAM and OFREG) will be provided by AKM.

(1) Click the DownLoad tab and see if the file to be downloaded.

(2) Program, CRAM, OFREG to be downloaded
PRAM File (Example): DSP19B_test.obj
(Port#1 to Port#2 and Port#2 to Port#1)

PRAM File: xxxxx.obj
CRAM File: xxxxx.cra
OFREG File: xxxxx.off

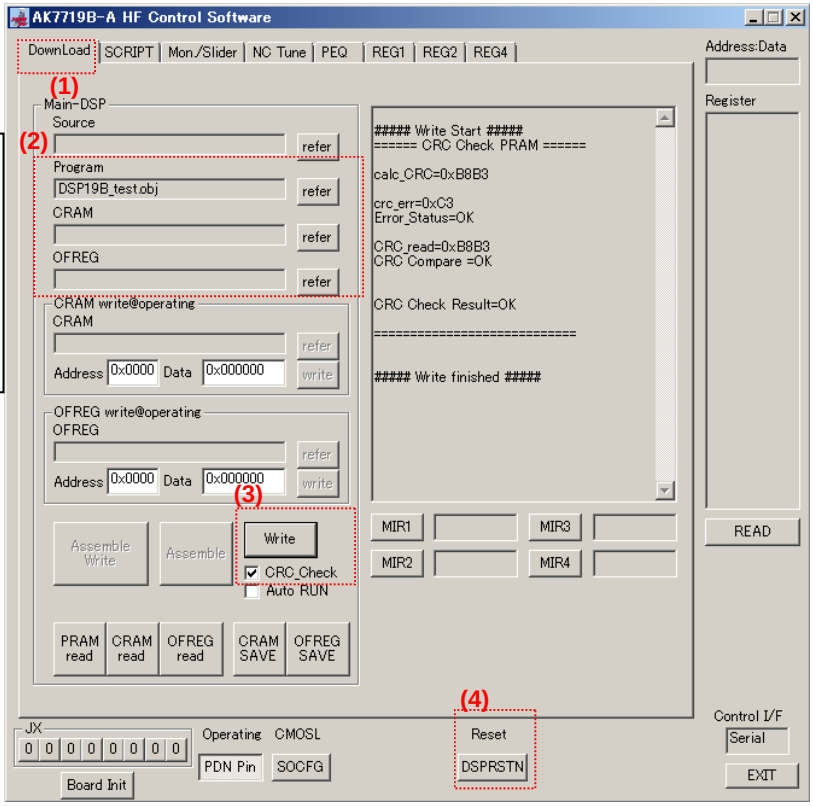


Figure 4. [Download] Dialogue of Control Software

(3) Check the “CRC_Check” box, click the Write button to download DSP programs into the AK7719B.
If a write error is occurred, check if the clocks are provided to the AK7719B.

(4) Click the DSPRSTN botton. Confirm Run state of the DSPRSTN button
Now, the AK7719B is in running state. Input signal to the Port#1(SDIN1) is output from SDOUT2 or 3 or 4 or 5.

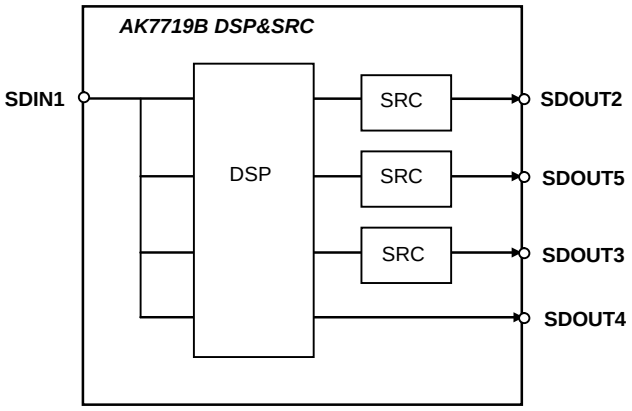


Figure 3. Signal Flow

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
13/04/09	KM113200	0	First edition		

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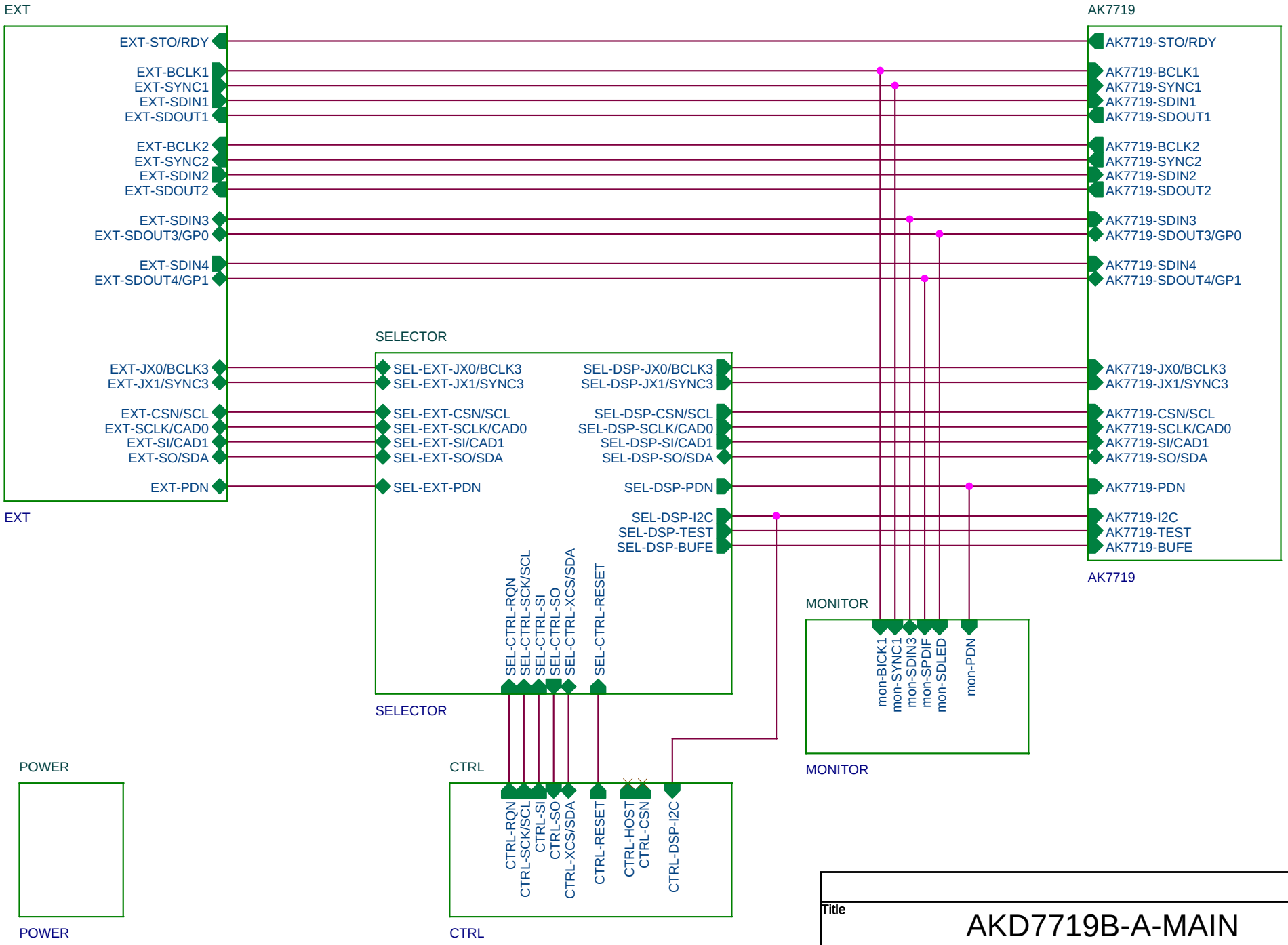

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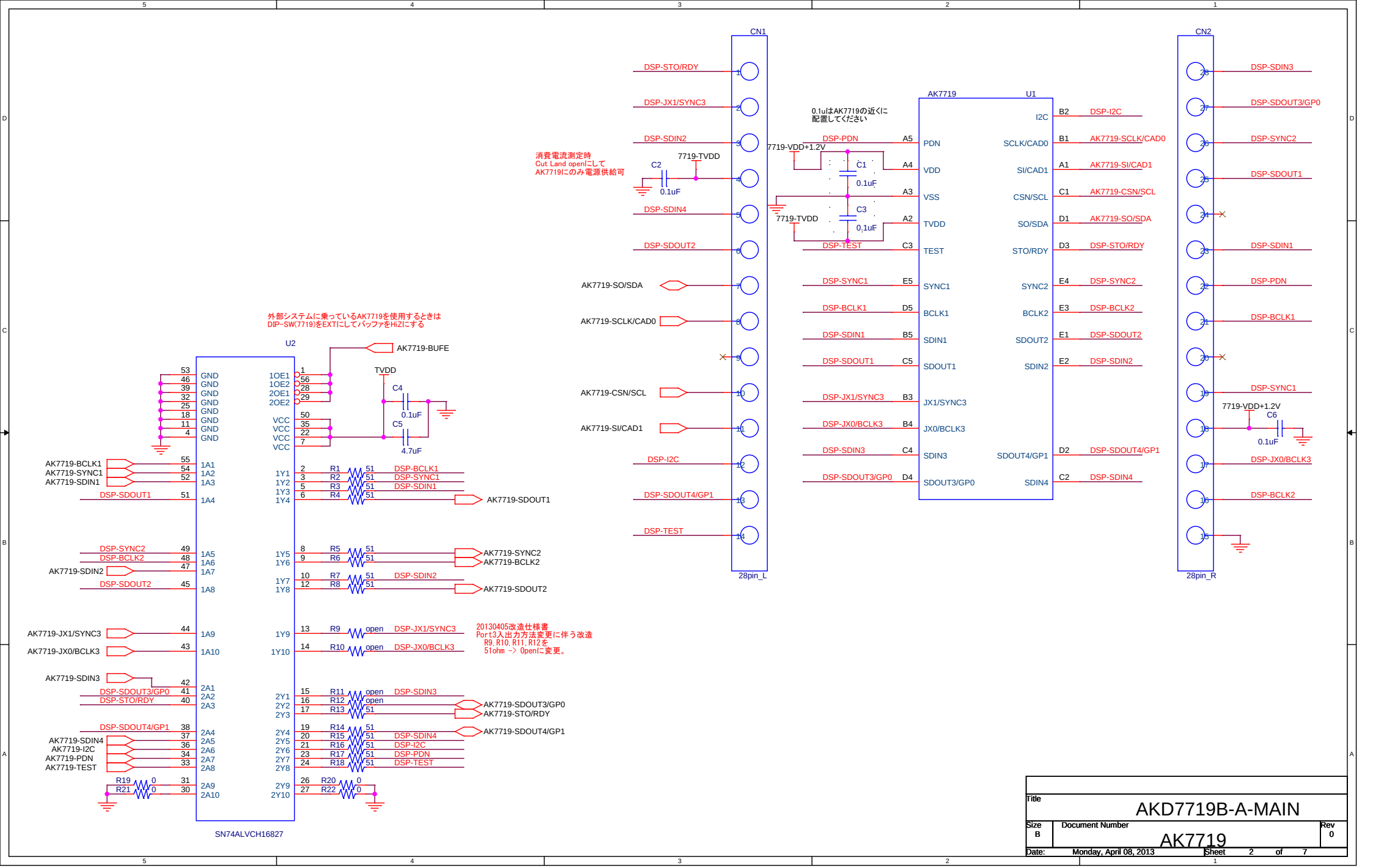
CN1
DSP-STO/RDY
DSP-JX1/SYNC3
DSP-SDIN2
DSP-SDIN4
DSP-SDOUT2
AK7719-SO/SDA
AK7719-SCLK/CAD0
AK7719-CSN/SCL
AK7719-SI/CAD1
DSP-I2C
DSP-SDOUT4/GP1
DSP-TEST
28pin_L
消費電流測定時
Cut Land openにして
AK7719にのみ電源供給可
7719-TVDD
C2
0.1uF
0.1uはAK7719の近くに
配置してください
7719-VDD+1.2V
C1
C3
AK7719
U1
PDN
VDD
VSS
TVDD
TEST
SYNC1
BCLK1
SDIN1
SDOUT1
JX1/SYNC3
JX0/BCLK3
SDIN3
SDOUT3/GP0
I2C
SCLK/CAD0
SI/CAD1
CSN/SCL
SO/SDA
STO/RDY
SYNC2
BCLK2
SDOUT2
SDIN2
SDOUT4/GP1
SDIN4
CN2
28pin_R
外部システムに乗っているAK7719を使用するときは
DIP-SW(7719)をEXTにしてバッファをHiZにする
U2
AK7719-BUFE
TVDD
C4
C5
4.7uF
GND
1OE1
1OE2
2OE1
2OE2
VCC
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1A9
1A10
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
2A9
2A10
1Y1
1Y2
1Y3
1Y4
1Y5
1Y6
1Y7
1Y8
1Y9
1Y10
2Y1
2Y2
2Y3
2Y4
2Y5
2Y6
2Y7
2Y8
2Y9
2Y10
AK7719-BCLK1
AK7719-SYNC1
AK7719-SDIN1
DSP-SDOUT1
DSP-SYNC2
DSP-BCLK2
AK7719-SDIN2
DSP-SDOUT2
AK7719-JX1/SYNC3
AK7719-JX0/BCLK3
AK7719-SDIN3
DSP-SDOUT3/GP0
DSP-STO/RDY
DSP-SDOUT4/GP1
AK7719-SDIN4
AK7719-I2C
AK7719-PDN
AK7719-TEST
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
DSP-BCLK1
DSP-SYNC1
DSP-SDIN1
AK7719-SDOUT1
AK7719-SYNC2
AK7719-BCLK2
DSP-SDIN2
AK7719-SDOUT2
DSP-JX1/SYNC3
DSP-JX0/BCLK3
20130405改造仕様書
Port3入出力方法変更に伴う改造
R9,R10,R11,R12を
51ohm -> Openに変更。
DSP-SDIN3
AK7719-SDOUT3/GP0
AK7719-STO/RDY
AK7719-SDOUT4/GP1
DSP-SDIN4
DSP-I2C
DSP-PDN
DSP-TEST
SN74ALVCH16827
DSP-SDIN3
DSP-SDOUT3/GP0
DSP-SYNC2
DSP-SDOUT1
DSP-SDIN1
DSP-PDN
DSP-BCLK1
DSP-SYNC1
DSP-BCLK2
DSP-JX0/BCLK3
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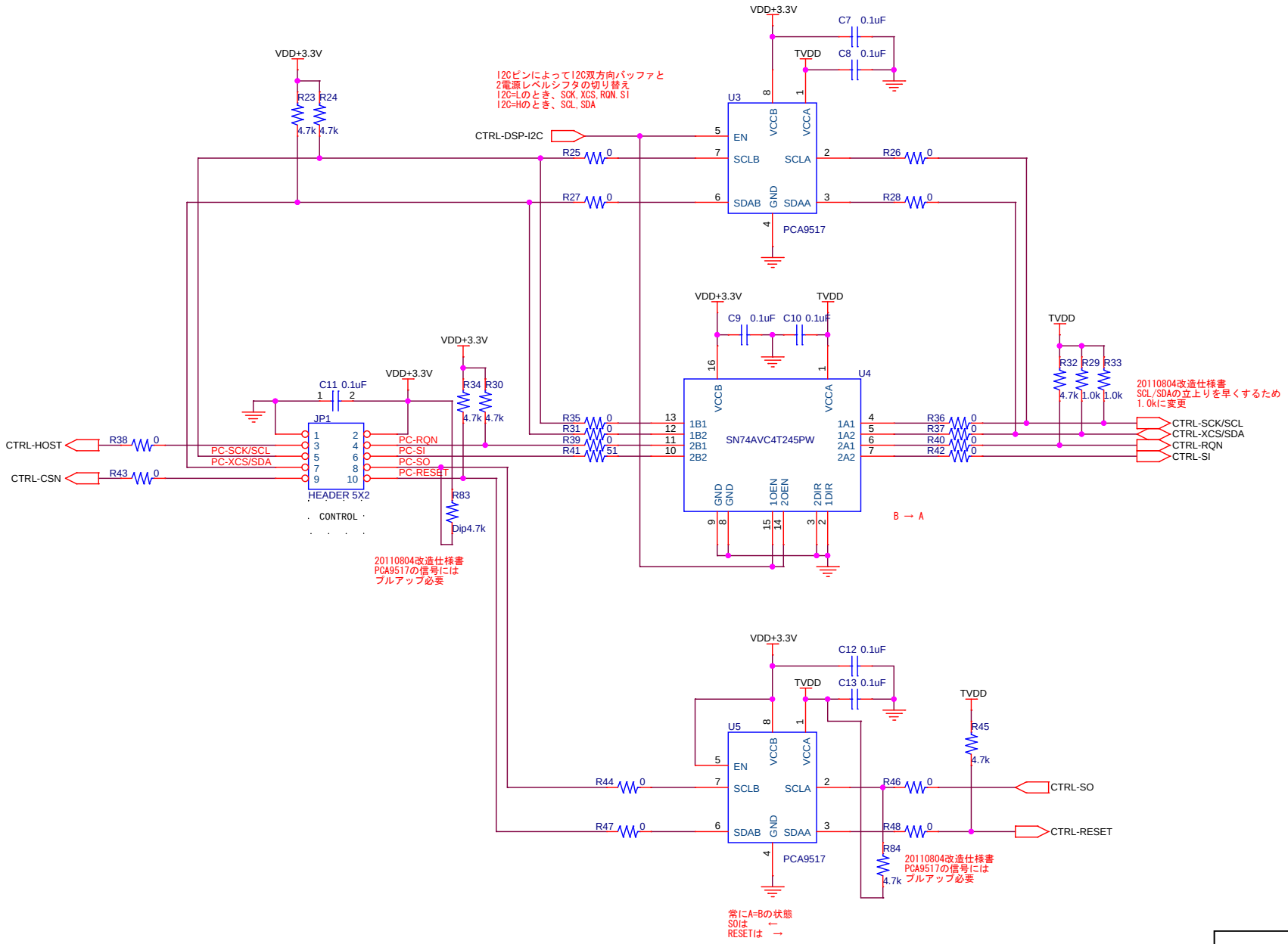

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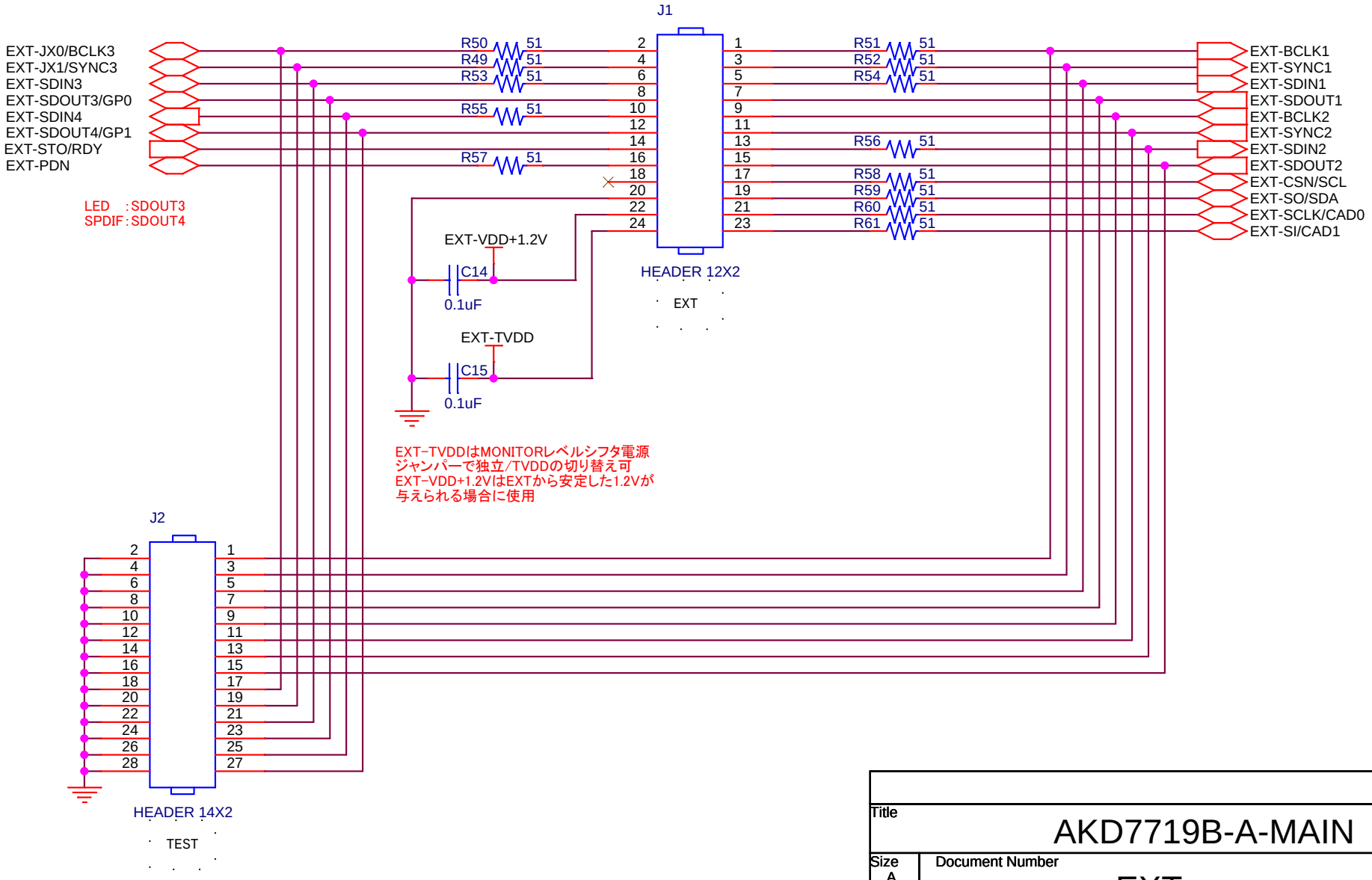

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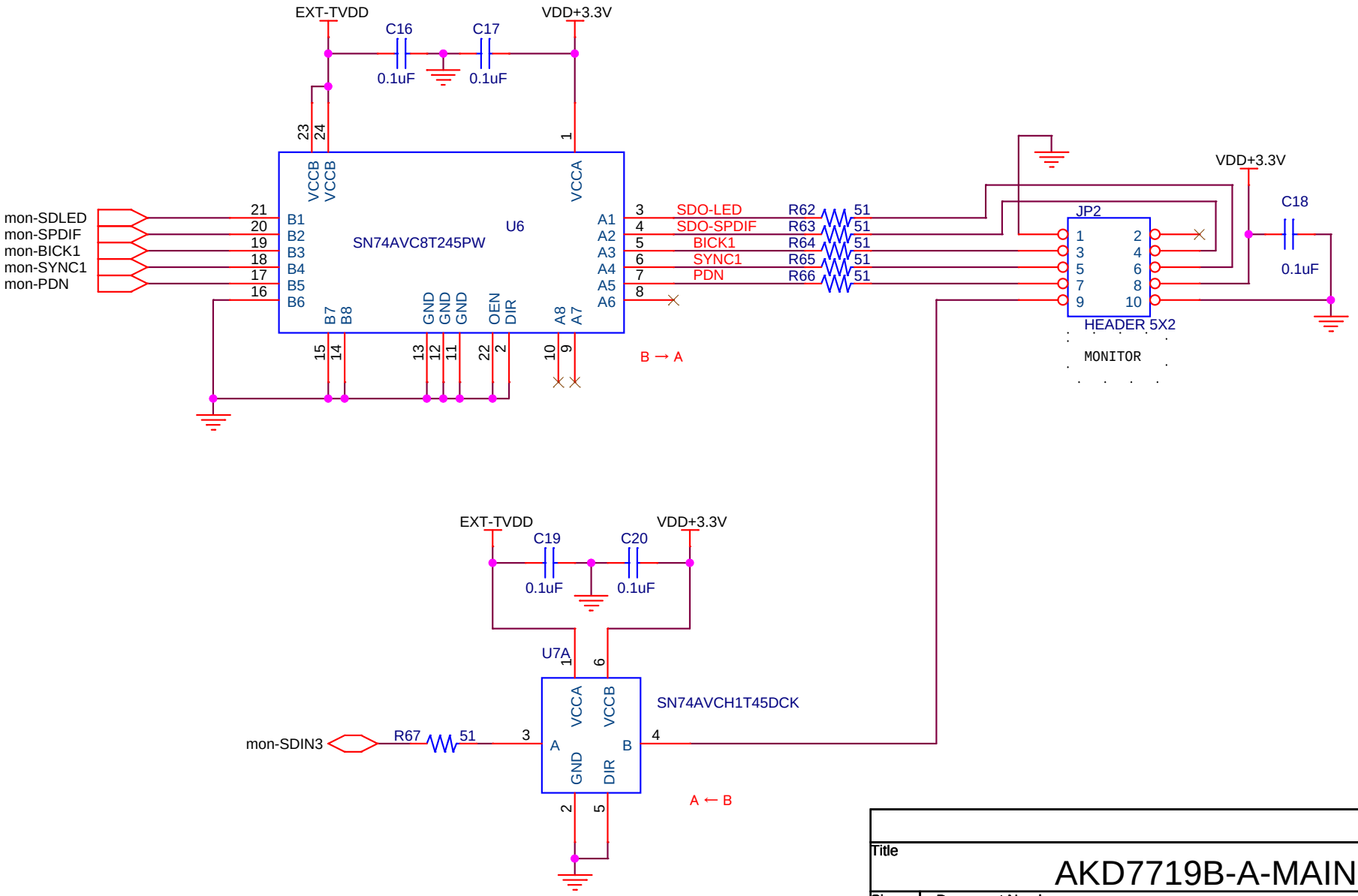

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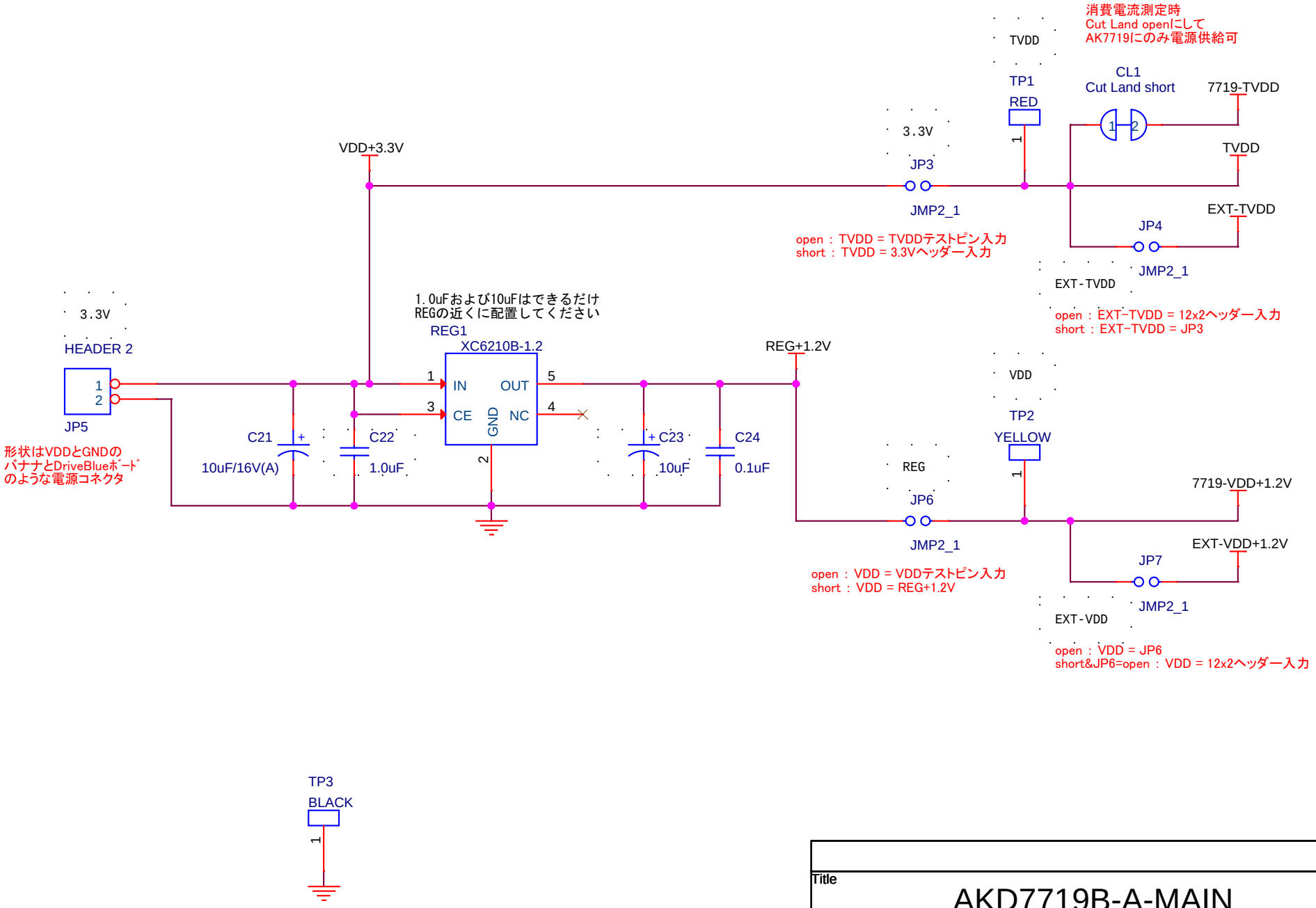

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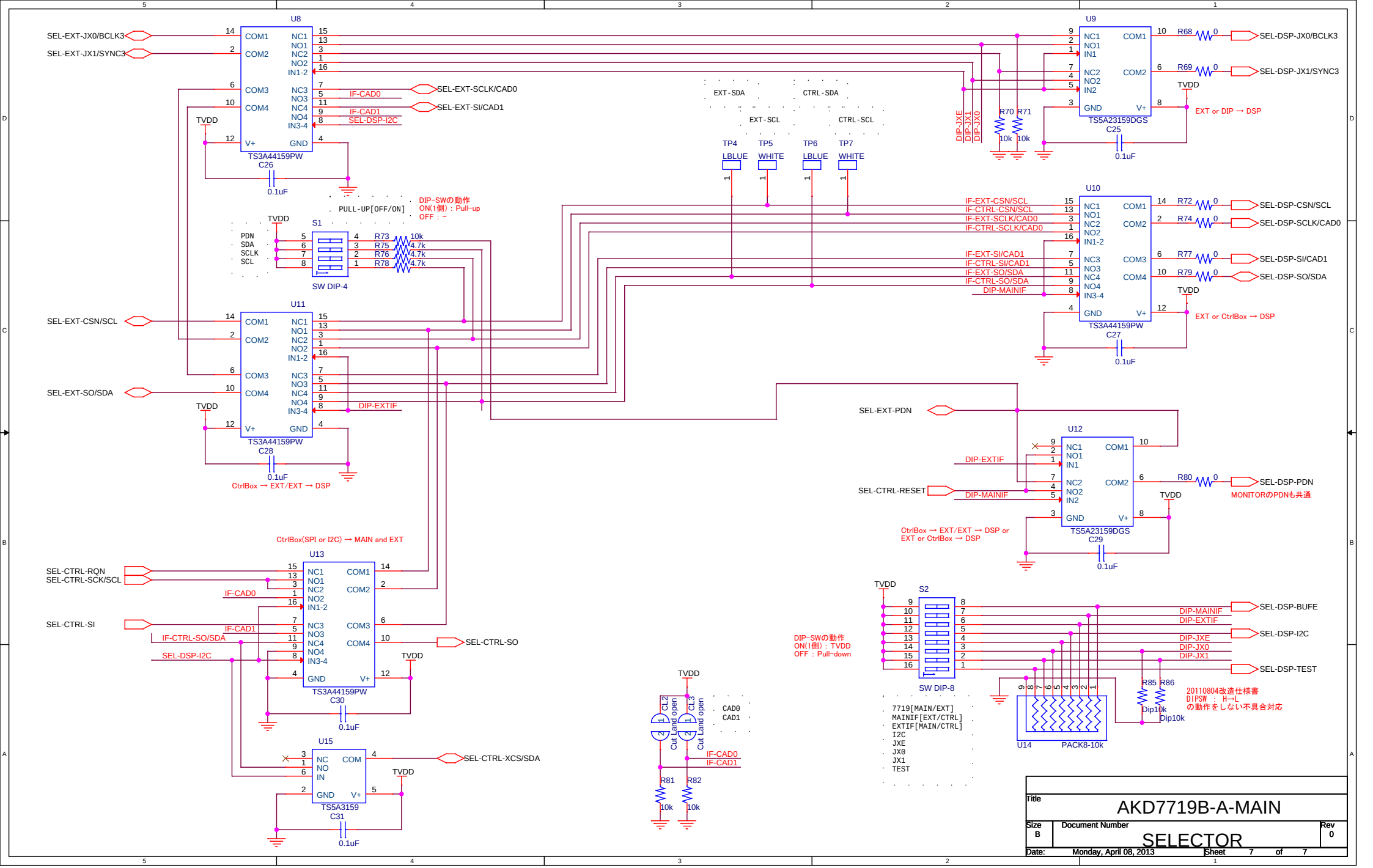
U8
SEL-EXT-JX0/BCLK3
SEL-EXT-JX1/SYNC3
COM1
COM2
COM3
COM4
V+
GND
NC1
NO1
NC2
NO2
IN1-2
NC3
NO3
NC4
NO4
IN3-4
IF-CAD0
IF-CAD1
SEL-DSP-I2C
SEL-EXT-SCLK/CAD0
SEL-EXT-SI/CAD1
TVDD
TS3A44159PW
C26
0.1uF
U9
SEL-DSP-JX0/BCLK3
SEL-DSP-JX1/SYNC3
R68
R69
R70
R71
10k
TS5A23159DGSC25
EXT or DIP → DSP
EXT-SDA
CTRL-SDA
EXT-SCL
CTRL-SCL
DIP-JXE
DIP-JX1
DIP-JX0
TP4
TP5
TP6
TP7
LBLUE
WHITE
PULL-UP[OFF/ON]
DIP-SWの動作
ON(1側)：Pull-up
OFF：−
S1
PDN
SDA
SCLK
SCL
R73
R75
R76
R78
4.7k
SW DIP-4
U10
IF-EXT-CSN/SCL
IF-CTRL-CSN/SCL
IF-EXT-SCLK/CAD0
IF-CTRL-SCLK/CAD0
IF-EXT-SI/CAD1
IF-CTRL-SI/CAD1
IF-EXT-SO/SDA
IF-CTRL-SO/SDA
DIP-MAINIF
SEL-DSP-CSN/SCL
SEL-DSP-SCLK/CAD0
SEL-DSP-SI/CAD1
SEL-DSP-SO/SDA
R72
R74
R77
R79
TS3A44159PW
C27
EXT or CtrlBox → DSP
U11
SEL-EXT-CSN/SCL
SEL-EXT-SO/SDA
DIP-EXTIF
C28
CtrlBox → EXT/EXT → DSP
SEL-EXT-PDN
U12
SEL-CTRL-RESET
SEL-DSP-PDN
MONITORのPDNも共通
R80
TS5A23159DGSC29
CtrlBox → EXT/EXT → DSP or
EXT or CtrlBox → DSP
CtrlBox(SPI or I2C) → MAIN and EXT
U13
SEL-CTRL-RQN
SEL-CTRL-SCK/SCL
SEL-CTRL-SI
SEL-CTRL-SO
TS3A44159PW
C30
U15
SEL-CTRL-XCS/SDA
TS5A3159
C31
CL2
CL3
Cut Land open
CAD0
CAD1
R81
R82
S2
DIP-SWの動作
ON(1側)：TVDD
OFF：Pull-down
SW DIP-8
7719[MAIN/EXT]
MAINIF[EXT/CTRL]
EXTIF[MAIN/CTRL]
I2C
JXE
JX0
JX1
TEST
SEL-DSP-BUFE
SEL-DSP-I2C
SEL-DSP-TEST
R85
R86
Dip10k
U14
PACK8-10k
20110804改造仕様書
DIPSW ： H→L
の動作をしない不具合対応
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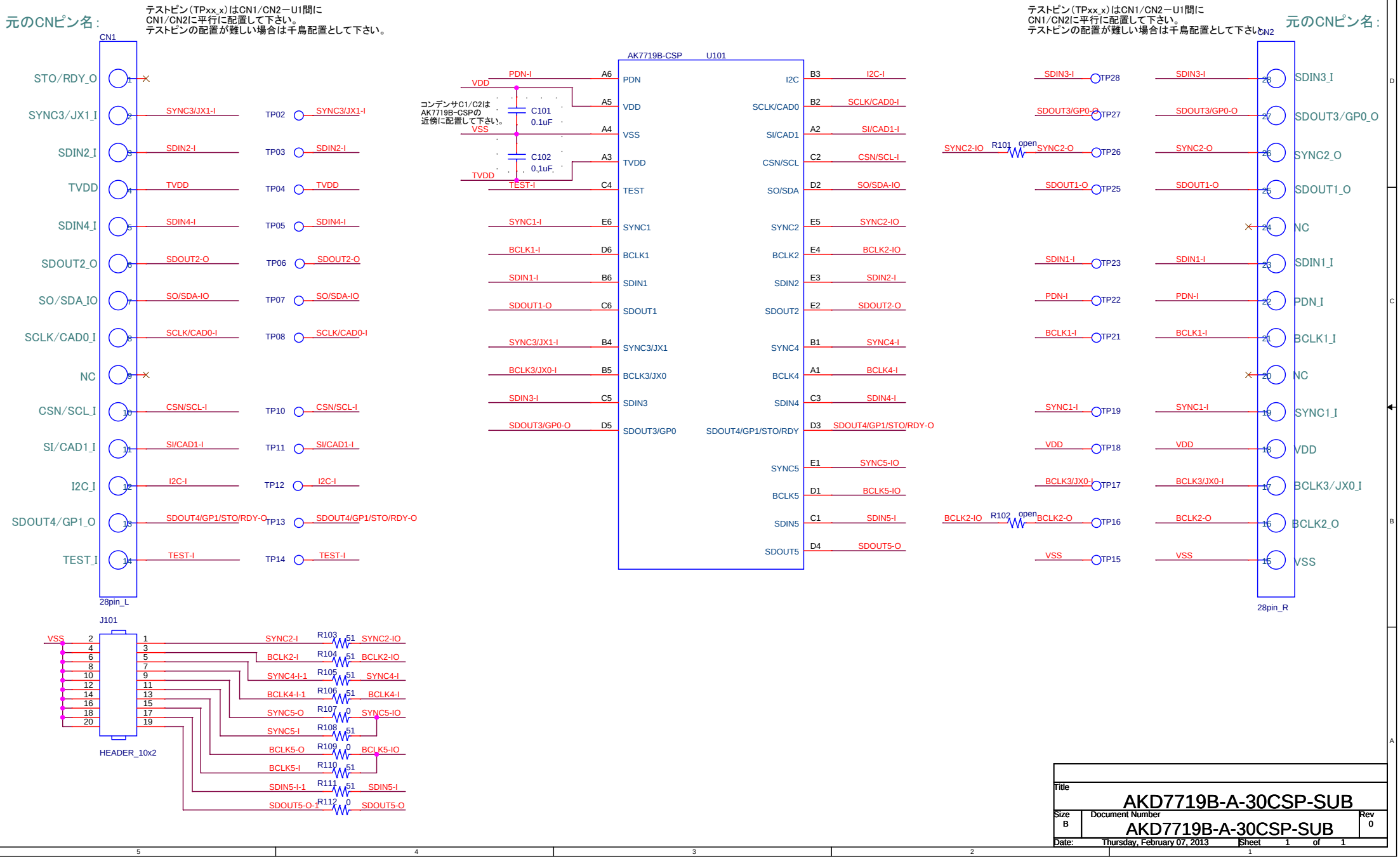

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