AK7758

DSP with Stereo CODEC + Mic/Lineout Amp

1. General Description

The AK7758 is a highly integrated digital signal processor, a stereo audio CODEC, a MIC pre-amplifier, a line-out amplifier, digital audio I/F. The main and sub DSPs have 3072step at fs = 48kHz parallel processing power. As the AK7758 is a RAM based DSP, it is programmable for user requirements such as high performance hands free function and acoustic effects. The AK7758 is available in a space saving small 36-pin QFN package.

2. Features

□ **DSP**
- **Word Length: 28-bit (Simple floating point)**
- **Instruction Cycle: Maximum 6.8ns (3072fs at fs=48kHz)**
- **Multiplier: 24 x 24 → 48-bit (double precision available)**
- **Divider: 24 / 24 → 24-bit (with floating point normalization function)**
- **ALU: 52-bit arithmetic operation (with overflow margin 4-bit)**
- **Program RAM (PRAM): 6144 x 36-bit**
- **Coefficient RAM (CRAM): 4096 x 24-bit**
- **Data RAM (DRAM): 4096 x 28-bit (24-bit floating point)**
- **Offset Register (OFREG): 32 x 14-bit**
- **Delay RAM (DLRAM): 16384 x 28-bit**
- **JX pins (Interrupt)**

□ **Sub DSP**
- **Word Length: 28-bit (Simple floating point)**
- **Instruction Cycle: Maximum 6.8ns (3072fs at fs=48kHz)**
- **Multiplier: 24 x 24 → 48-bit (double precision available)**
- **Divider: 24 / 24 → 24-bit (with floating point normalization function)**
- **ALU: 52bit arithmetic operation (with overflow margin 4bit)**
- **Program RAM (PRAM): 1024 x 36-bit**
- **Coefficient RAM (CRAM): 3072 x 24-bit**
- **Data RAM (DRAM): 3072 x 28-bit**
- **Delay RAM (DLRAM): 3072 x 28-bit**

□ **Two Digital Interfaces (I/F 1, I/F 2)**
- **Digital Signal Input Port (6ch) MSB justified 24-bit/ LSB justified 24, 20, 16-bit and I^2S**
- **Digital Signal Output Port (8ch) MSB justified 24-bit/ LSB justified 24, 20, 16-bit and I^2S**
- **Short / Long Frame**
- **TDM 128fs (4ch), 192fs (6ch), 256fs (8ch) Formats**

□ Stereo 24-bit ADC:
- **Sampling Frequency: fs = 8kHz ~ 48kHz**
- **ADC Characteristics: S/(N+D): 91dB; DR, S/N: 102dB**
- **Stereo Analog Input Selector (Differential, Single-ended Input)**
- **Stereo Analog Input Range Adjustment Amplifier (Single-ended Input)**
- **Channel Independent Analog Gain Amplifier for Microphone (0 ~ 18dB(2dB Step),18dB~36dB(3dB Step))**
- **Analog DRC (Adjustable Dynamic Range)**
- **Channel Independent Digital Volume (24dB ~ -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**

□ Line Input
- **Single-ended**
- **Line Amplifier (21dB ~ -21dB, 3dB Step, Mute)**

□ Stereo 24-bit DAC
- **Sampling Frequency: fs = 8kHz ~ 48kHz**
- **Digital Volume (12dB ~ -115dB, 0.5dB Step, Mute)**

□ Line Output
- **Single-ended**
- **S/(N+D): 89dB; DR, S/N: 106dB**
- **Stereo Analog Volume (+0 ~ -28dB, 2.0dB Step, Mute)**

□ Analog Mixer

□ Digital Mixer

□ 2ch Digital Microphone Interface

□ 3 types Analog Direct Path

□ PLL Circuit

□ I^2C bootloader
- **EEPROM Mat Selectable**

□ µP Interface: SPI, I^2CBUS(400kHz Fast-Mode)

□ Power Supply:

Analog	**AVDD: 3.0V ~ 3.6V (typ. 3.3V)**
Digital 1	**LVDD: 3.0V ~ 3.6V (typ. 3.3V)**
Digital 2	**DVDD: 1.14V ~ 1.3V (typ. 1.2V)**
	(External Power Supply or Internal Regulator is selectable)
I/F	**TVDD1/2: 1.7V ~ 3.6V (typ. 3.3V)**

□ Operating Temperature Range: -40 ~ 85°C

□ Package: 36-pin QFN (0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

4.1. Device Block Diagram

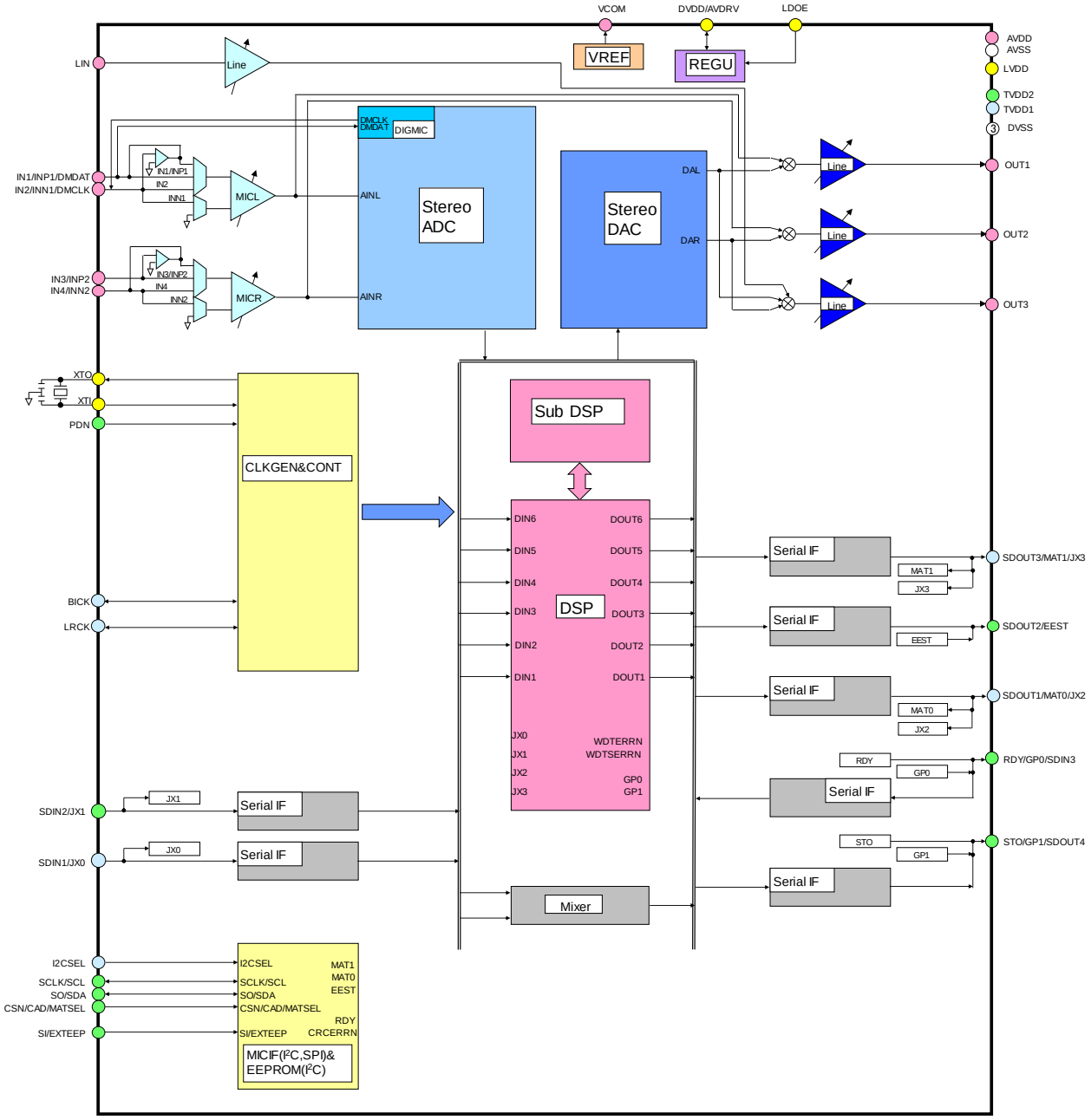


Figure 1. Whole Block Diagram

4.2. DSP Block Diagram

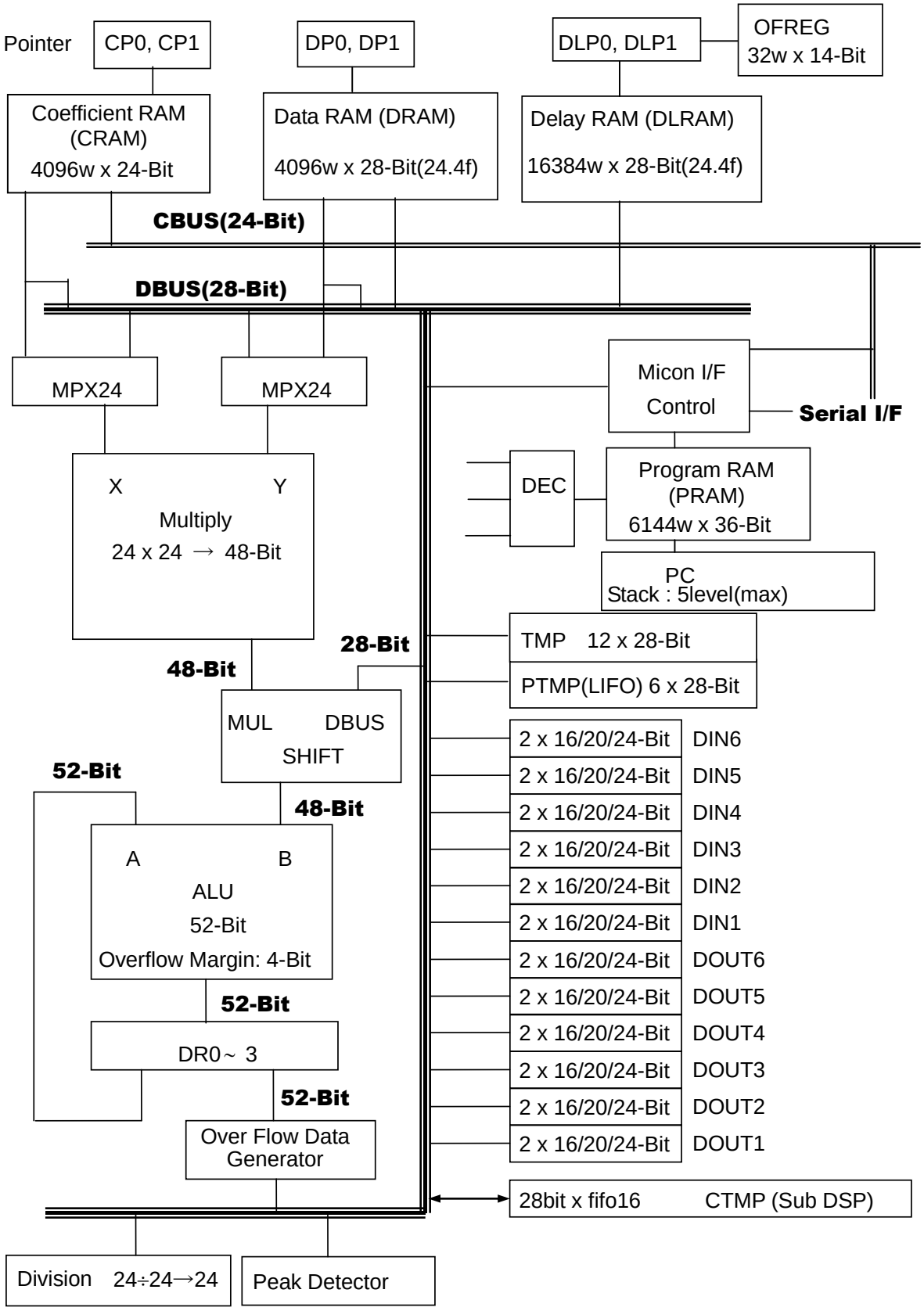


Figure 2. DSP Block Diagram

4.3. Sub DSP Block Diagram

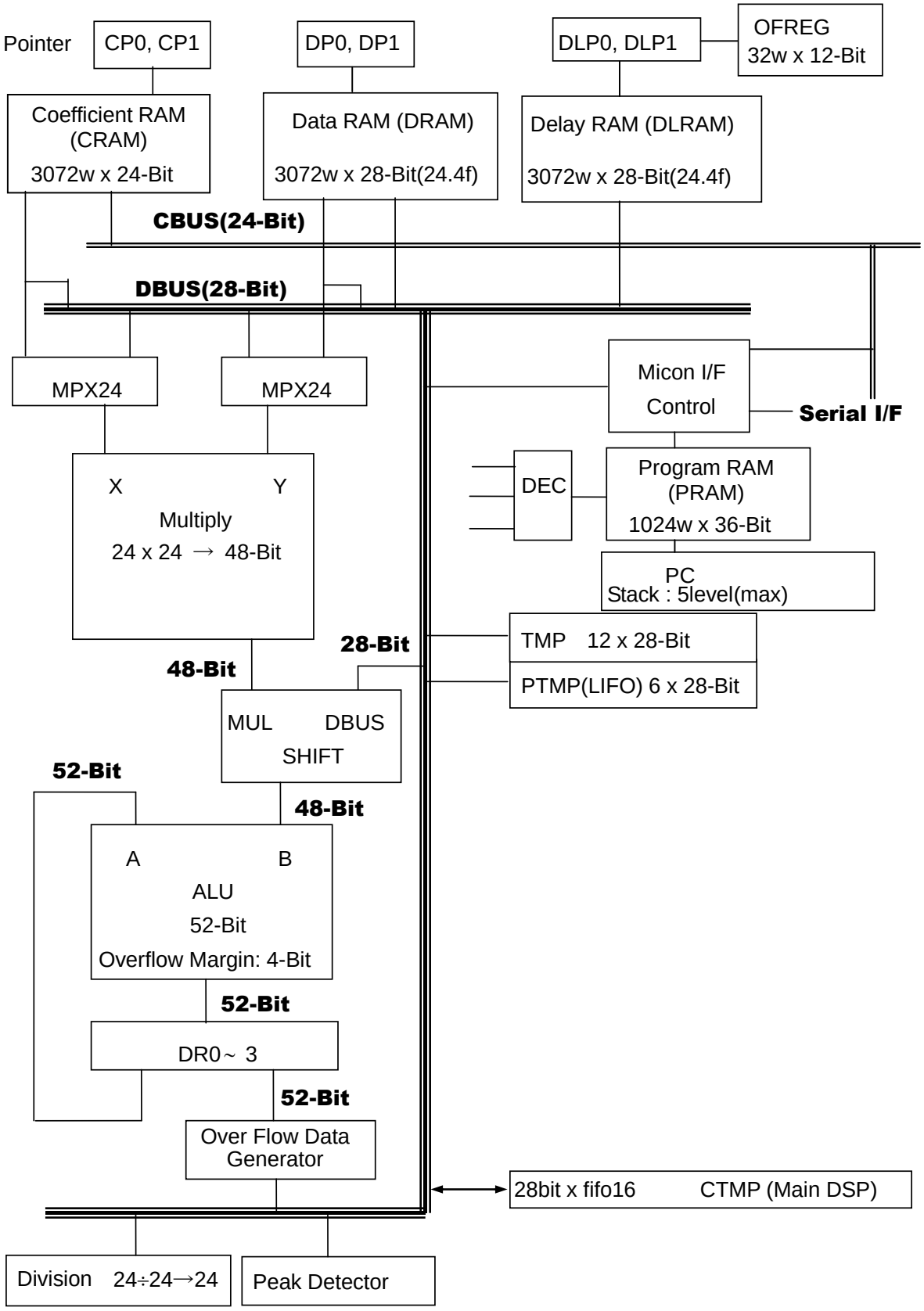


Figure 3. Sub DSP Block Diagram

5. Pin Configurations and Functions

5.1. Pin Configurations

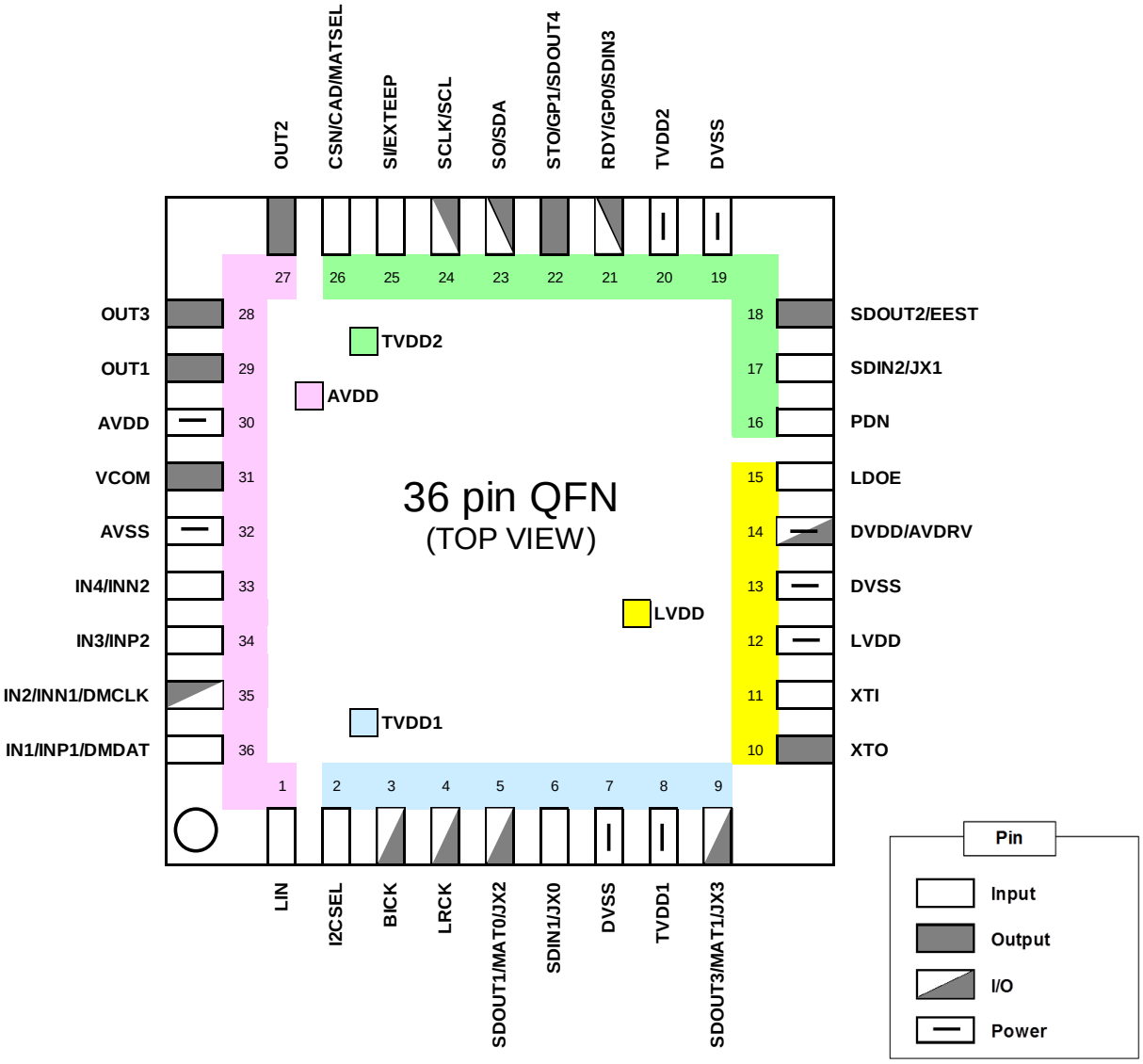


Figure 4. Pin Configurations

5.2. Pin Function

No.	Name	I/O	Function
1	LIN	I	Line Input Pin
2	I2CSEL	I	I^2C-BUS Select Pin ▪ I2CSEL pin = "L": SPI Interface ▪ I2CSEL pin = "H": I^2C-bus Interface The I2CSEL pin must be fixed to "L" (DVSS) or "H" (TVDD1).
3	BICK	I/O	Serial Bit Clock Output Pin (Internal pull-down)
4	LRCK	I/O	LR Channel Select Pin (Internal pull-down)
5	SDOUT1	O	Serial Data Output1 Pin (SDOUT1E bit = "1")
	MAT0	I	EEPROM Download Mat Select Address0 (Internal pull-down) (I2CSEL pin = EXTEEP pin = MATSEL pin = "H")
	JX2	I	External Conditional Jump2 Pin (Internal pull-down) (SDOUT1E bit = "0" & (D1JX2E bit = "1" or D2JX2E bit = "1"))
6	SDIN1	I	Serial Data Input1 Pin (SDIN1SEL bit = "0")
	JX0	I	External Conditional Jump0 Pin (SDIN1SEL bit = "1" & (D1JX0E bit = "1" or D2JX0E bit = "1"))
7	DVSS	-	Ground Pin 0V
8	TVDD1	-	Digital IO Power Supply1 Pin: 1.7~3.6V (typ.3.3V)
9	SDOUT3	O	Serial Data Output3 Pin (SDOUT1E bit = "1")
	MAT1	I	EEPROM Download Mat Select Address1 (Internal pull-down) (I2CSEL pin = EXTEEP pin = MATSEL pin = "H")
	JX3	I	External Conditional Jump3 Pin (Internal pull-down) (SDOUT3E bit = "0" & (D1JX3E bit = "1" or D2JX3E bit = "1"))
10	XTO	O	Crystal Oscillator Output Pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, connect an external clock or leave this pin as open.
11	XTI	I	Crystal Oscillator Input Pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, connect this pin to the external clock or open.
12	LVDD	-	Power Supply Pin for Digital Core: 3.0~3.6V (typ.3.3V)
13	DVSS	-	Digital Ground Pin 0V
14	DVDD	-	Power Supply Pin for Digital Core: 1.14~1.3V (typ. 1.2V) (LDOE pin = "L")
	AVDRV	O	LDO Output Pin (LDOE pin = "H") Connect a 2.2uF (±30%) capacitor between this pin and DVSS. This pin must not be connected to an external circuit.
15	LDOE	I	LDO Select Pin LDOE pin = "L": 14 pin External 1.2V Power Supply LDOE pin = "H": 14 pin LDO Output (LDO Drive) The LDOE pin must be fixed to "L (DVSS)" or "H (LVDD)".
16	PDN	I	Power-down N Pin ▪ The AK7758 can be powered-down by this pin. ▪ Set this pin to "L" upon power-up the AK7758.
17	SDIN2	I	Serial Data Input2 Pin (SDIN2SEL bit = "0")
	JX1	I	External Conditional Jump1 Pin (SDIN2SEL bit = "1" & (D1JX1E bit = "1" or D2JX1E bit = "1"))
18	SDOUT2	O	Serial Data Output2 Pin (SDOUT2E bit = "1")
	EEST	O	EEPROM Interface Status (for downloading data from EEPROM)
19	DVSS	-	Digital Ground Pin 0V
20	TVDD2	-	Digital IO Power Supply2 Pin: 1.7~3.6V (typ. 3.3V)

21	RDY	O	RDY Pin (RDYE bit = “1” & RDYSEL bit = “0”)
	GP0	O	General Purpose Output 0 Pin (RDYE bit = “1” & RDYSEL bit = “1”)
	SDIN3	I	Serial Data Input3 Pin (Internal pull-down) (SDIN3SEL bit = “1” & RDYE bit = “0”)
22	STO	O	Status Output Pin (STOE bit = “1” & STOSEL [1:0] bits = “00”)
	GP1	O	General Purpose Output 1 Pin (STOE bit = “1” & STOSEL [1:0] bits = “01”)
	SDOUT4	O	Serial Data Output4 Pin (STOE bit = “1” & STOSEL [1:0] bits = “10”)
23	SO	O	SO pin (I2CSEL pin = “L”)
	SDA	I/O	SDA pin I^2C BUS Interface (I2CSEL pin = “H”)
24	SCLK	I	Serial Data Clock Pin for SPI Interface (I2CSEL pin = “L”) ▪ Set this pin to “H” when there is no clock input.
	SCL	I/O	SCL pin I^2C-BUS Interface Pin (I2CSEL pin = “H”) EEPROM Download This becomes an output pin when EXTEEP pin = “H”.
25	SI	I	Serial Data Input Pin for SPI Interface (I2CSEL pin = “L”) ▪ Set this pin to “L” when not used.
	EXTEEP	I	EEPROM Download Control Pin (I2CSEL pin = “H”)
26	CSN	I	Chip Select N Pin for SPI Interface (I2CSEL pin = “L”) ▪ Set this pin to “H” when the AK7758 is in power-down mode or when the microprocessor I/F is not used.
	CAD	I	I^2C-BUS Address Pin (I2CSEL pin = “H”)
	MATSEL	I	EEPROM Mat Select Pin (I2CSEL pin = EXTEEP pin = “H”)
27	OUT2	O	Line Output 2 Pin
28	OUT3	O	Line Output 3 Pin
29	OUT1	O	Line Output 1 Pin
30	AVDD	-	Analog Power Supply Pin: 3.0~3.6V (typ.3.3V)
31	VCOM	O	Common Voltage Output Pin of Analog Block ▪ Connect a 2.2μF capacitor between AVSS. ▪ Do not connect to an external circuit.
32	AVSS	-	Ground Pin 0V
33	IN4/INN2	I	ADC Input Pin (AINE bit = “1”)
34	IN3/INP2	I	ADC Input Pin (AINE bit = “1”)
35	IN2/INN1	I	ADC Input Pin (AINE bit = “1”)
	DMCLK	O	Digital MIC Clock Output Pin (DMIC bit = “1”)
36	IN1/INP1	I	ADC Input Pin (AINE bit = “1”)
	DMDAT	I	Digital MIC Data Input 1 Pin (DMIC bit = “1”)

Note 1. The exposed pad on the bottom surface of the package must be open or connected to the ground.

Note 2. All digital input pins must not be allowed to float. If analog input pins are not used, leave them open.

Note 3. The description of (Internal Pull-down) above indicates the pin status just after power-down is released (PDN pin = “H”).

5.3. Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN, IN1/INP1, IN2/INN1, IN3/INP2, IN4/INN2, OUT1, OUT3, OUT2	Open
Digital	BICK, LRCK, SDOUT1/MAT0/JX2, SDOUT3/MAT1/JX3, XTO, XTI SDOUT2/EEST, RDY/GP0/SDIN3, STO/GP1/SDOUT4, DMDAT, DMCLK	Open
	SDIN1/JX0, SDIN2/JX1	Connect to DVSS

Table 1. Handling of Unused Pin

Note 4. It is recommended to connect the LRCK pin or the BICK pin to DVSS. However, it is no problem to be open since they are internally pulled-down pin.

5.4. Relationship between Power Supplies and Digital Pins

Power Supply	Digital Pins
AVDD	DMDAT, DMCLK
TVDD1	I2CSEL, BICK, LRCK, SDOUT1/MAT0/JX2, SDIN1/JX0, SDOUT3/MAT1/JX3
TVDD2	CSN/CAD/MATSEL, SI/EXTEEP, SCLK/SCL, SO/SDA, STO/GP1/SDOUT4, RDY/GP0/SDIN3, SDOUT2/EEST, SDIN2/JX1, PDN
LVDD	XTO, XTI, LDOE

Table 2. Relationship between Power Supplies and Digital Pins

5.5. Power-down and Power-down Release Pin Statuses

No.	Pin Name	I/O	PDN pin = "L"			PDN pin = "H" (default)	
			I/O	Status		I/O	Status
				LDOE pin="L"	LDOE pin="H"		
1	LIN	I	I	"Hi-Z"	"Hi-Z"	I	Analog Input
3	BICK	I/O	I	Pull Down(46kΩ)	Pull Down(50kΩ)	I	Pull Down(46kΩ)
4	LRCK	I/O	I	Pull Down(46kΩ)	Pull Down(50kΩ)	I	Pull Down(46kΩ)
5	SDOUT1	O	I	Pull Down(46kΩ)	Pull Down(50kΩ)		
	MAT0	I				I	Pull Down(46kΩ)
	JX2	I					
9	SDOUT3	O	I	Pull Down(46kΩ)	Pull Down(50kΩ)		
	MAT1	I				I	Pull Down(46kΩ)
	JX3	I					
10	XTO	O	O	"H"	"H"	O	Inverted XTI Input
14	AVDRV	O	O	-	Pull Down(70Ω)	O	Output (LDOE pin="H")
18	SDOUT2	O	O	"L"	Pull Down(50kΩ)	O	"L"
	EEST	O				O	"L"
21	RDY	O	I	Pull Down(46kΩ)	Pull Down(50kΩ)	-	-
	GP0	O				-	-
	SDIN3	I				I	Pull Down(46kΩ)
22	STO	O	O	"H"	Pull Down(50kΩ)	O	"H"
	GP1	O					
	SDOUT4	O					
23	SO	O	-	"Hi-Z" (@CSN="H")	"Hi-Z"	-	"Hi-Z" (@CSN="H")
	SDA	I/O	-	"Hi-Z"	"Hi-Z"	-	"Hi-Z"
24	SCLK	I	I	"Hi-Z"	"Hi-Z"	I	Input (I2CSEL pin="L")
	SCL	I	I	"Hi-Z"	"Hi-Z"	I	Input (I2CSEL pin="H", EXTEEP pin="L")
		O	O	"Hi-Z"	"Hi-Z"	O	Output (I2CSEL pin="H", EXTEEP pin="H")
27	OUT2	O	O	"Hi-Z"	"Hi-Z"	O	"Hi-Z"
28	OUT3	O	O	"Hi-Z"	"Hi-Z"	O	"Hi-Z"
29	OUT1	O	O	"Hi-Z"	"Hi-Z"	O	"Hi-Z"
31	VCOM	O	O	"L"	"L"	O	Analog Output
33	IN4/INN2	I	I	"Hi-Z"	"Hi-Z"	I	Analog Input (AINE bit="1")
34	IN3/INP2	I	I	"Hi-Z"	"Hi-Z"	I	Analog Input (AINE bit="1")
35	IN2/INN1	I	I	"Hi-Z"	"Hi-Z"	I	Analog Input (AINE bit="1")
	DMCLK	O	O	"Hi-Z"	"Hi-Z"	O	Digital Output (DMIC bit="1")
36	IN1/INP1	I	I	"Hi-Z"	"Hi-Z"	I	Analog Input (AINE bit="1")
	DMDAT	I	I	"Hi-Z"	"Hi-Z"	I	Digital Input (DMIC bit="1")

Table 3. Power-down and Power-down Release Pin Statuses

6. Absolute Maximum Ratings

(AVSS=DVSS=0V: Note 5)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core:LVDD)	LVDD	-0.3	4.3	V
Digital2(I/F1)	TVDD1	-0.3	4.3	V
Digital3(I/F2)	TVDD2	-0.3	4.3	V
Digital4(Core:DVDD)	VD12	-0.3	1.6	V
DVSS-AVSS (Note 5)	ΔGND	-0.3	0.3	V
AVDD-LVDD (Note 6)	ΔAVDD	-0.3	0.3	V
AVDD-TVDD1	ΔTVDD1	-0.3	4.3	V
Input Current (except power supply pins)	IIN	–	±10	mA
Analog Input Voltage (Note 7)	VINA	-0.3	(AVDD+0.3) ≤ 4.3	V
Digital Input Voltage (Note 8)	VIND1	-0.3	(LVDD+0.3) ≤ 4.3	V
Digital Input Voltage (Note 9)	VIND2	-0.3	(TVDD1+0.3) ≤ 4.3	V
Digital Input Voltage (Note 10)	VIND3	-0.3	(TVDD2+0.3) ≤ 4.3	V
Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 5. All voltages are with respect to ground. AVSS and DVSS must be connected to the same ground.
Note 6. AVDD and LVDD must be the same voltage.
Note 7. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 8. The maximum digital input voltage of the XTI pin or the LDOE pin is smaller value between (LVDD+0.3)V and 4.3V.
Note 9. The maximum digital input voltage of the I2CSEL, BICK, LRCK, MAT0/JX2, SDIN1/JX0 and MAT1/JX3 pins is smaller value between (TVDD1+0.3)V and 4.3V.
Note 10. The maximum digital input voltage of the CSN/CAD/MATSEL, SI/EXTEEP, SCLK/SCL, SDA, SDIN3, SDIN2/JX1, and PDN pins is smaller value between (TVDD2+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V: Note 5)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core:LVDD)	LVDD	3.0	3.3	3.6	V
Digital2(I/F:TVDD1)	TVDD1	1.7	3.3	3.6	V
Digital3(I/F:TVDD2)	TVDD2	1.7	3.3	3.6	V
Digital4(Core:DVDD)	VD12	1.14	1.2	1.3	V

Note 11. AVDD, LVDD, TVDD1 and TVDD2 must be powered up first before DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-up sequence with AVDD, LVDD, TVDD1 and TVDD2 is not critical. The PDN pin should be held "L" when power is supplied. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

Note 12. When using the I^2C interface, (I2CSEL pin = "H"), do not turn off the power supply of the AK7758 with the power supply of the surrounding device turned on. Pull-up of SDA and SCL pins must not exceed TVDD2.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

8.1. Analog Characteristics

8.1.1. MIC Amp Gain

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”)

	Parameter		Min.	Typ.	Max.	Unit
MIC Amp Gain	MGNL[3:0]	MGNR[3:0]				
	0x0	0x0	-1	0	1	dB
	0x1	0x1	1	2	3	dB
	0x2	0x2	3	4	5	dB
	0x3	0x3	5	6	7	dB
	0x4	0x4	7	8	9	dB
	0x5	0x5	9	10	11	dB
	0x6	0x6	11	12	13	dB
	0x7	0x7	13	14	15	dB
	0x8	0x8	15	16	17	dB
	0x9	0x9	17	18	19	dB
	0xA	0xA	20	21	22	dB
	0xB	0xB	23	24	25	dB
	0xC	0xC	26	27	28	dB
	0xD	0xD	29	30	31	dB
	0xE	0xE	32	33	34	dB
	0xF	0xF	35	36	37	dB

8.1.2. Line-in Amp Gain

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”)

	Parameter	Min.	Typ.	Max.	Unit
Line-in Amp Gain	LIGN[3:0]				
	0x0	-1	0	1	dB
	0x1	-4	-3	-2	dB
	0x2	-7	-6	-5	dB
	0x3	-10	-9	-8	dB
	0x4	-13	-12	-11	dB
	0x5	-16	-15	-14	dB
	0x6	-19	-18	-17	dB
	0x7	-22	-21	-20	dB
	0x8		N/A		dB
	0x9	+2	+3	+4	dB
	0xA	+5	+6	+7	dB
	0xB	+8	+9	+10	dB
	0xC	+11	+12	+13	dB
	0xD	+14	+15	+16	dB
	0xE	+17	+18	+19	dB
	0xF	+20	+21	+22	dB

(N/A : Not available)

8.1.3. MIC Amp + ADC

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz~20kHz)

	Parameter			Min.	Typ.	Max.	Unit
MIC Amp	Input Impedance			14	20		kΩ
MIC Amp + ADC	Resolution					24	bit
	Dynamic Characteristics (Differential Input mode)						
	S/(N+D) (-1dBFS)	fs=48kHz (Note 16)		80	91		dB
		fs=48kHz (Note 17)			88		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) (Note 16)		94	102		dB
		fs=48kHz (A-weighted) (Note 17)			93		dB
	S/N	fs=48kHz (A-weighted) (Note 16)		94	102		dB
		fs=48kHz (A-weighted) (Note 17)			93		dB
	Inter-Channel Isolation (Note 13)			90	105		dB
	DC Accuracy (Differential Input)						
	Channel Gain Mismatch				0.0	0.3	dB
	Analog Input						
	Input Voltage (Differential Input) (Note 14)		(Note 16)	±2.0	±2.2	±2.4	Vp-p
			(Note 17)		±0.277		Vp-p
	Input Voltage (Single-ended Input) (Note 15)		(Note 16)	2.0	2.2	2.4	Vp-p
			(Note 17)		0.277		Vp-p

Note 13. Indicates inter-channel isolation between Lch and Rch when –1dBFS signal is input.
Note 14. INP1/INN1 and INP2/INN2 pins.
Note 15. IN1, IN2, IN3 and IN4 pins.
Note 16. MGNL/R[3:0] bits = 0x0 (0dB)
Note 17. MGNL/R[3:0] bits = 0x9 (18dB)

8.1.4. ATT Amp + MIC Amp + ADC

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz~20kHz)

	Parameter		Min.	Typ.	Max.	Unit
ATT Amp	Feedback Resistance (Rf)		10		30	kΩ
	Load Capacitance (CL)				20	pF
	Phase compensation capacitance (Cc) (Note 18)		10			pF
ATT Amp + MIC Amp + ADC	Resolution				24	bit
	Dynamic Characteristics					
	S/(N+D) (-1dBFS) (Note 19)	fs=48kHz	74	84		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	88	98		dB
	S/N	fs=48kHz (A-weighted)	88	98		dB
	Inter-Channel Isolation (Note 20)		90	99		dB
	DC Accuracy					
	Channel Gain Mismatch			0.0	0.3	dB

Note 18. This is the value of external capacitors between the IN1pin and the IN2 pin, and the IN3 pin and the IN4 pin. They are necessary when using the ATT amplifier.

Note 19. In the case of inputting 5.76 Vpp signal when the external input resistance (Ri) is 47 kΩ, the Feedback resistance (Rf) is 16 kΩ, external capacitance (Cc) is 47pF and the MIC amplifier gain is set to 0dB (GMNL/R[3:0] bits = 0x0). (5.76 Vpp x 16kΩ / 47kΩ = 1.96Vpp @ -1dBFS)

Note 20. Indicates inter-channel isolation between Lch and Rch when –1dBFS signal is input.

Note 21. Microphone amplifier gain should be set to 0dB when using the path of ATT-Amp + MIC-Amp + ADC. ADC operation is not guaranteed if the microphone amplifier gain is 4dB or more.

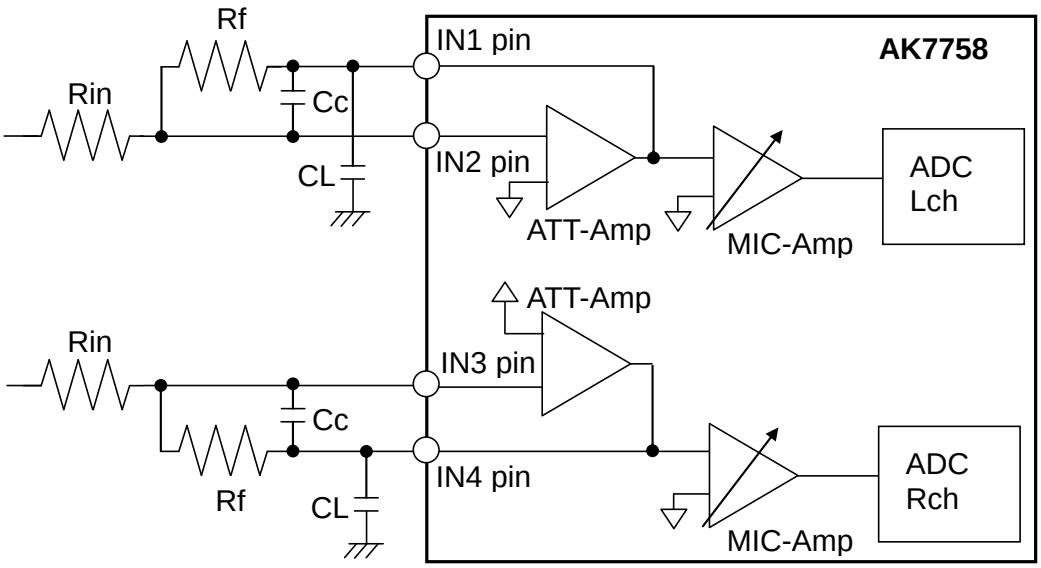


Figure 5. Connection Diagram when using ATT-AMP

8.1.5. Line-in Amp + Line-out Amp

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”
Signal Frequency 1kHz; Measurement Frequency =20Hz~20kHz)

	Parameter		Min.	Typ.	Max.	Unit
Line-in Amp	Input Impedance		14	20		kΩ
Line-in Amp + Line-out Amp	Dynamic Characteristics					
	S/(N+D) (0dBFS)	(Note 23)	77	81		dB
		(Note 24)		82		dB
	Dynamic Range (-60dBFS) (A-weighted)	(Note 23)	95	103		dB
		(Note 24)		92		dB
	S/N (A-weighted)	(Note 23)	95	103		dB
		(Note 24)		92		dB
	Analog Input					
	Input Voltage (Note 22)	(Note 23)	2.28	2.51	2.74	Vp-p
		(Note 24)		0.316		Vp-p

Note 22. LIN pin. These are the values when the output voltage of the OUT3 pin is 0dBFS (AVDD x 0.76).
Note 23. LIGN[3:0] bits = 0x0 (0dB), LOVOL3[3:0] bits = 0xF(0dB), LO3SW1 bit =“0”, LO3SW2 bit = “0”, LO3SW3 bit = “1”
Note 24. LIGN[3:0] bits = 0xE (+18 dB), LOVOL3[3:0] bits = 0xF(0dB), LO3SW1 bit =“0”, LO3SW2 bit = “0”, LO3SW3 bit = “1”

8.1.6. Line-out Amp Gain

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”)

	Parameter			Min.	Typ.	Max.	Unit
Line-out Amp	LOVOL1[3:0]	LOVOL2[3:0]	LOVOL3[3:0]				
	0x0	0x0	0x0		mute		dB
	0x1	0x1	0x1	-29	-28	-27	dB
	0x2	0x2	0x2	-27	-26	-25	dB
	0x3	0x3	0x3	-25	-24	-23	dB
	0x4	0x4	0x4	-23	-22	-21	dB
	0x5	0x5	0x5	-21	-20	-19	dB
	0x6	0x6	0x6	-19	-18	-17	dB
	0x7	0x7	0x7	-17	-16	-15	dB
	0x8	0x8	0x8	-15	-14	-13	dB
	0x9	0x9	0x9	-13	-12	-11	dB
	0xA	0xA	0xA	-11	-10	-9	dB
	0xB	0xB	0xB	-9	-8	-7	dB
	0xC	0xC	0xC	-7	-6	-5	dB
	0xD	0xD	0xD	-5	-4	-3	dB
	0xE	0xE	0xE	-3	-2	-1	dB
	0xF	0xF	0xF	-1	0	1	dB

8.1.7. DAC + Lineout Amp

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz~20kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC + Lineout Amp	Resolution				24	bit
	Dynamic Characteristics (OUT1,OUT2,OUT3)					
	S/(N+D) (0 dBFS)	fs=48kHz	80	89		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	106		dB
	S/N	fs=48kHz (A-weighted)	100	106		dB
	Inter-Channel Isolation (f=1kHz) (Note 25)		90	110		dB
	DC Accuracy					
	Channel Gain Mismatch			0.0	0.5	dB
	Analog Output					
	Output Voltage (Note 26)		2.28	2.51	2.74	Vp-p
	Load Resistance		10			kΩ
	Load Capaitance				30	pF

Note 25. Indicates inter-channel isolation between Lch and Rch of DAC.
Note 26. Full-scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.76).

8.1.8. MIC Amp + Line-out Amp

(Ta= 25°C; AVDD=LVDD=TVDD1/2=3.3V; AVSS=DVSS=0V; LDOE pin =“H”
Signal Frequency 1kHz; Measurement Frequency =20Hz~20kHz)

	Parameter		Min.	Typ.	Max.	Unit
MIC Amp + Line-out Amp	Dynamic Characteristics (differential Input)					
	S/(N+D) (0dBFS)	(Note 29)	77	82		dB
		(Note 30)		82		dB
	Dynamic Range (-60dBFS) (A-weighted)	(Note 29)	101	104		dB
		(Note 30)		93		dB
	S/N (A-weighted)	(Note 29)	101	104		dB
		(Note 30)		93		dB
	Analog Input					
	Input Voltage (differential Input) (Note 27)	(Note 29)	±2.28	±2.51	±2.74	Vp-p
		(Note 30)		±0.316		Vp-p
	Input Voltage (single-ended Input) (Note 28)	(Note 29)	2.28	2.51	2.74	Vp-p
		(Note 30)		0.316		Vp-p

Note 27. The INP1/INN1 and INP2/INN2 pins
Note 28. The IN1, IN2, IN3 and IN4 pins
Note 29. MGNL/R[3:0] bits = 0x0 (0dB)
Note 30. MGNL/R[3:0] bits = 0x9 (18dB)

8.2. DC Characteristics

(Ta= -40~85°C, AVDD=3.3V, DVDD=1.2V, LVDD=3.0 ~ 3.6V, TVDD1/2=1.7 ~ 3.6V, AVSS=DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage		VIH	80%LVDD 80%TVDD1 80%TVDD2			V
Low Level Input Voltage		VIL			20%LVDD 20%TVDD1 20%TVDD2	V
SCL, SDA High Level Input Voltage		VIH2	70%TVDD2			V
SCL, SDA Low Level Input Voltage		VIL2			30%TVDD2	V
DMDAT High Level Input Voltage (DMIC bit = “1”)		VIH3	65%AVDD			V
DMDAT Low Level Input Voltage (DMIC bit = “1”)		VIL3			35%AVDD	V
High Level Output Voltage Iout= -100μA (Note 31)		VOH	TVDD1-0.3 TVDD2-0.3			V
Low Level Output Voltage Iout=100μA (Note 32)		VOL			0.3	V
SCL, SDA Low Level Output Voltage Iout=3mA	TVDD2 ≥ 2.0V	VOL2			0.4	V
	TVDD2 < 2.0V	VOL2			20%TVDD2	V
DMCLK High Level Output Voltage Iout = -80μA (DMIC bit = “1”)		VOH3	AVDD-0.4			V
DMCLK Low Level Output Voltage Iout = 80μA (DMIC bit = “1”)		VOL3			0.4	V
Input Leak Current (Note 33)		Iin			±10	μA
Input Leak Current at Pulled-down Pins LDO Mode (LDOE pin = “H”) and Power-down (PDN pin = “L”) (Note 34)		Iid		66		μA
Input Leak Current at Pulled-down Pins Power-down Release (PDN pin = “H”) (Note 35)		Iid		77		μA
Input Leak Current at the XTI pin		Iix		17		μA

Note 31. Except XTO pin
Note 32. Except SDA and XTO pins.
Note 33. Internal Pulled-down pins, except the XTI pin
Note 34. LRCK, BICK, SDOUT1/MAT0/JX2, SDOUT3/MAT1/JX3, RDY/GP0/SDIN3, SDOUT2/EEST, STO/GP1/SDOUT4 pin (Typ. 50 kΩ@3.3V)
Note 35. LRCK, BICK, SDOUT1/MAT0/JX2, SDOUT3/MAT1/JX3, RDY/GP0/SDIN3 pin (Typ. 46kΩ@3.3V)

8.3. Power Consumptions

(Ta=25°C, AVDD=LVDD=3.0~3.6V (Typ.=3.3V, Max.=3.6V), DVDD=1.14~1.3V (Typ.=1.2V, Max.=1.3V), TVDD1/2=1.7~3.6V (Typ.=3.3V, Max.=3.6V), AVSS=DVSS=0V, fs=48kHz, BICK=64fs, SDOUT1~4 / LRCK / BICK = Output, CL=20pF)

	Parameter	Min.	Typ.	Max.	Unit
Power consumptions in operation 1 (LDOE pin = “L”) (Note 36)	AVDD+LVDD		19	27	mA
	TVDD1+TVDD2		1.4	2	mA
	DVDD		29	85	mA
Power consumptions in operation 2 (LDOE pin = “H”) (Note 36)	AVDD+LVDD		51	110	mA
	TVDD1+TVDD2		1.4	2	mA
Power consumptions in power-down 1 (PDN pin = “ L”, LDOE pin = “L”)	AVDD+LVDD		10		μA
	TVDD1+TVDD2		10		μA
	DVDD		400		μA
Power consumptions in power-down 2 (PDN pin = “L”, LDOE pin = “H”)	AVDD+LVDD		1.5		μA
	TVDD1+TVDD2		1		μA

Note 36. DVDD power consumption will be changed depending on DSP programs.

8.4. Digital Filter Characteristics

8.4.1. ADC

(Ta= -40~85°C; AVDD＝LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, fs=48kHz (Note 37))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 38)	+0.14dB ~ −0.12dB	PB	0		20.7	kHz
	-0.87dB			21.6		kHz
	-3.0dB			22.8		kHz
Stopband (Note 39)		SB	28.4			kHz
Passband Ripple (Note 38)		PR			±0.14	dB
Stopband Ripple (Note 39, Note 40)		SA	65			dB
Group Delay Distorsion		ΔGD		0		μs
Group Daley (Ts=1/fs)		GD		12.5		Ts

Note 37. The passband and stopband frequencies scale with “fs” (system sampling rate). The characteristic of the high pass filter is not included.
Note 38. The passband is from DC to 18.9kHz when fs=48kHz.
Note 39. The stopband is 28kHz to 3.044MHz when fs=48kHz.
Note 40. When fs = 48kHz, the analog modulator samples the input signal at 3.072MHz. There is no attenuation of an input signal in band (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

8.4.2. DAC

(Ta=-40~85°C; AVDD＝LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, fs=48kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 41)	(±0.05dB)	PB	0		21.7	kHz
	(-6.0dB)			24		kHz
Stopband (Note 41)		SB	26.2			kHz
Passband Ripple		PR			±0.05	dB
Stopband Ripple		SA	64			dB
Group Daley (Ts=1/fs) (Note 42)		GD		24		Ts
Digital Filter + Analog Filter						
Amplitude Characteristics 20Hz~20.0kHz				±0.5		dB

Note 41. The passband and stopband frequencies are proportional to “fs” (system sampling rate), and represents PB=0.4535 × fs(@±0.05dB) and SB=0.5465 × fs, respectively.
Note 42. The digital filter delay is calculated as the time from setting data into the input register until an analog signal is output.

8.5. Switching Characteristics

8.5.1. System Clock
(Ta= -40~85°C; AVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
with Crystal Oscillator						
Input Frequency		fXTI	11.2896		18.432	MHz
with External Clock						
Duty Cycle			40	50	60	%
Input Frequency		fXTI	11.0		18.6	MHz
LRCK Frequency	(Note 43)	fs	8		48	kHz
BICK Frequency	(Note 44)					
Normal Interface	High Level Width	tBCLKH	128			ns
	Low Level Width	tBCLKL	128			ns
	Frequency	fBCLK	0.23	3.072	3.1	MHz
TDM Interface	High Level Width	tBCLKH	32			ns
	Low Level Width	tBCLKL	32			ns
	Frequency	fBCLK	1.8	12.288	12.3	MHz

Note 43. LRCK frequency and sampling rate (fs) should be the same.
Note 44. When BICK is the source of the master clock, it should be synchronized to LRCK and have stable frequency.

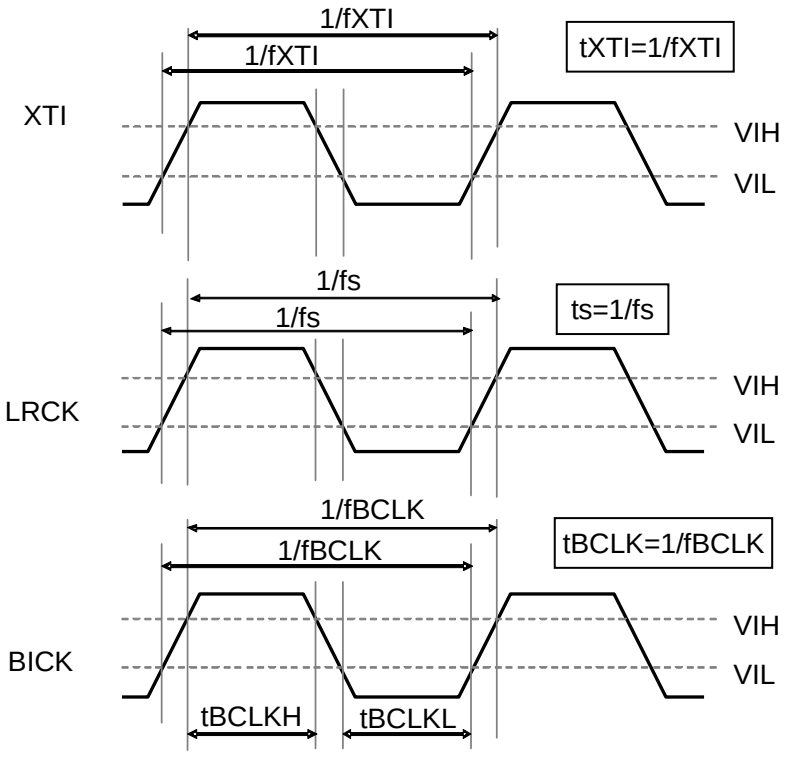


Figure 6. System Clock Timing

8.5.2. Power Down

(Ta= -40~85°C; AVDD=LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (Note 45)	tRST	600			ns

Note 45. The PDN pin must be set "L" when power up the AK7758.

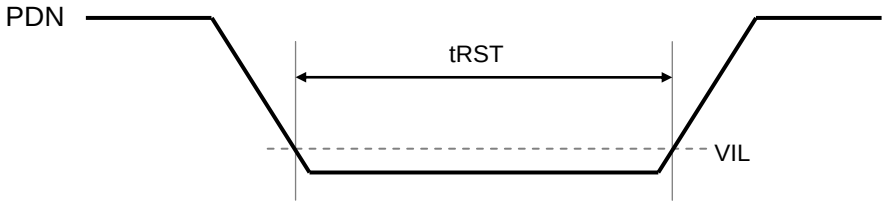


Figure 7. Reset Timing

8.5.3. Serial Data Interface (SDIN1/2/3, SDOUT1/2/3/4) Power Down

(Ta= -40~85°C; AVDD=LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (Note 46)	tBLRD	20			ns
Delay Time from LRCK to BICK "↑" (Note 46)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from LRCK to Serial Data Output (Note 47)	tLRD			30	ns
Delay Time from BICK "↓" to Serial Data Output (Note 48)	tBSOD			30	ns
Master Mode					
BICK Frequency	fBCLK		32,48,64, 128,256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK (Note 48)	tMBL	-12		12	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (Note 47)	tLRD			20	ns
Delay Time from BICK "↓" to Serial Data Output (Note 48)	tBSOD			20	ns
SDINx → SDOUTy (x=1,2,3, y=1,2,3,4,)					
Delay Time from SDINn to SDOUTn Output	tIOD		2		fs

Note 46. BICK edge must not occur at the same time as LRCK edge.
If BICK polarity was inverted, the counting edge of BICK will be "↓".
Note 47. Except I^2S.
Note 48. When the polarity of BICK is inverted, delay time is from BICK "↑".
Note 49. SDINx(x=1~3) and SDOUTy (y=1~4) should be set to the same Sync Domain. There are the values when the input data of SDOUTy is set to SDINx.

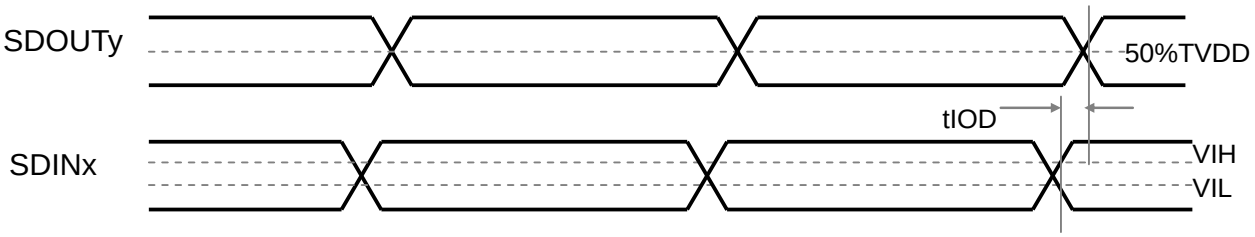


Figure 8. Serial Interface Delay Time from SDINx to SDOUTy Output

8.5.3.1. Slave Mode

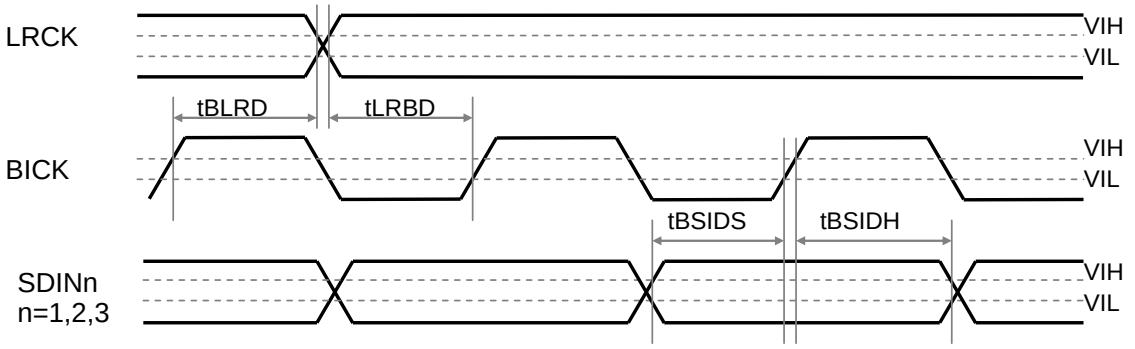


Figure 9. Serial Interface Input Timing in Slave Mode

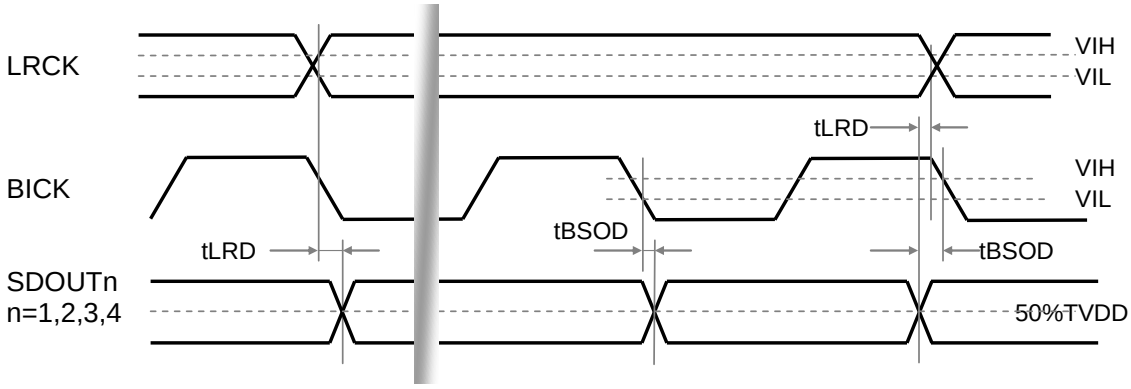


Figure 10. Serial Interface Output Timing in Slave Mode

8.5.3.2. Master Mode

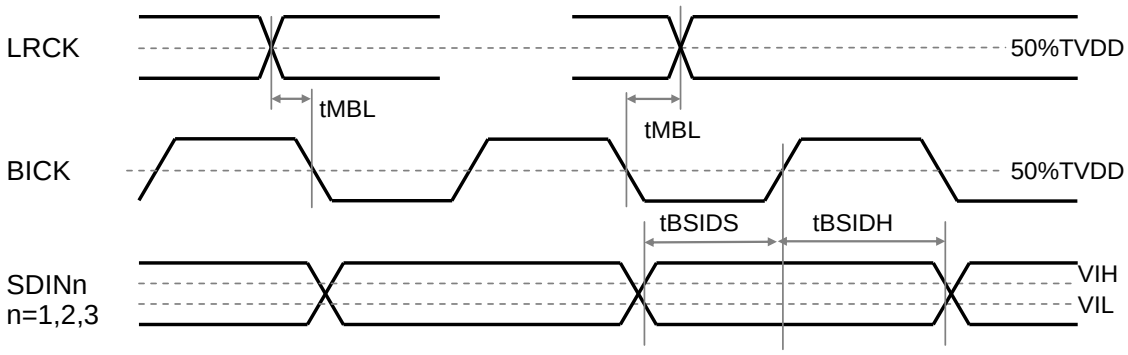


Figure 11. Serial Interface Input Timing in Master Mode

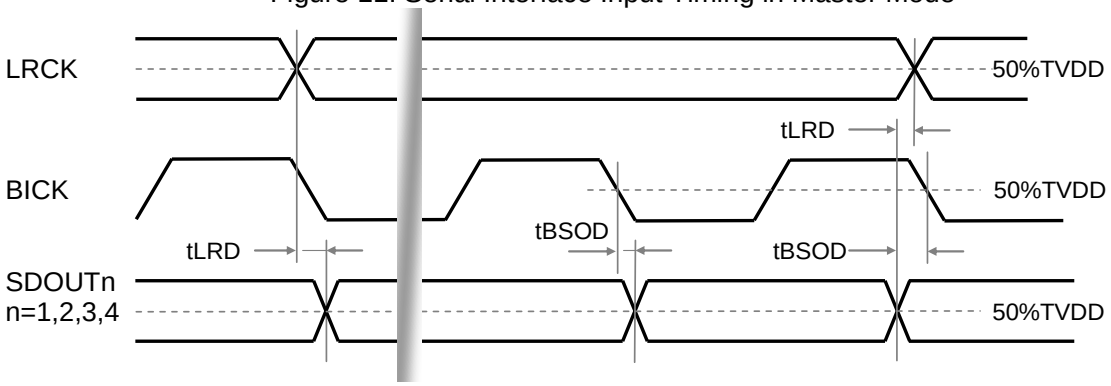


Figure 12. Serial Interface Output Timing in Master Mode

8.5.4. SPI Interface

8.5.4.1. Clock Reset (CKRESTN bit = “0”)

(Ta= -40~85°C; AVDD=LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Microcontroller Interface Signal					
SCLK Frequency (Note 50)	fSCLK			3.5	MHz
SCLK Low Level Width	tSCLKL	120			ns
SCLK High Level Width	tSCLKH	120			ns
Microcontroller → AK7758					
CSN High Level Width	tWRQH	300			ns
Time from CSN “↑” to PDN “↑”	tRST	360			ns
Time from PDN“↑” to CSN “↓”	tIRRQ	1			ms
Time from CSN“↓” to SCLK“↓”	tWSC	360			ns
Time from SCLK“↑” to CSN“↑”	tSCW	480			ns
SI Latch Setup Time	tSIS	40			ns
SI Latch Hold Time	tSIH	40			ns
AK7758 → Microcontroller					
SO Output Delay Time from SCLK “↓”	tSOS			40	ns

Note 50. SCLK frequency becomes 7 MHz when accessing control registers.

8.5.4.2. PLL Lock (CKRESTN bit = “1”)

(Ta= -40~85°C; AVDD=LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Microcontroller Interface Signal					
SCLK Frequency (Note 51)	fSCLK			7	MHz
SCLK Low Level Width	tSCLKL	60			ns
SCLK High Level Width	tSCLKH	60			ns
Microcontroller → AK7758					
CSN High Level Width	tWRQH	150			ns
Time from CSN “↑” to PDN “↑”	tRST	180			ns
Time from PDN“↑” to CSN “↓”	tIRRQ	1			ms
Time from CSN“↓” to SCLK“↓”	tWSC	150			ns
Time from SCLK“↑” to CSN“↑”	tSCW	240			ns
SI Latch Setup Time	tSIS	20			ns
SI Latch Hold Time	tSIH	20			ns
AK7758 → Microcontroller					
SO Output Delay Time from SCLK “↓”	tSOS			40	ns

Note 51. It takes 10ms at maximum until PLL is locked, after setting CKRESTN bit to “1” from “0”.

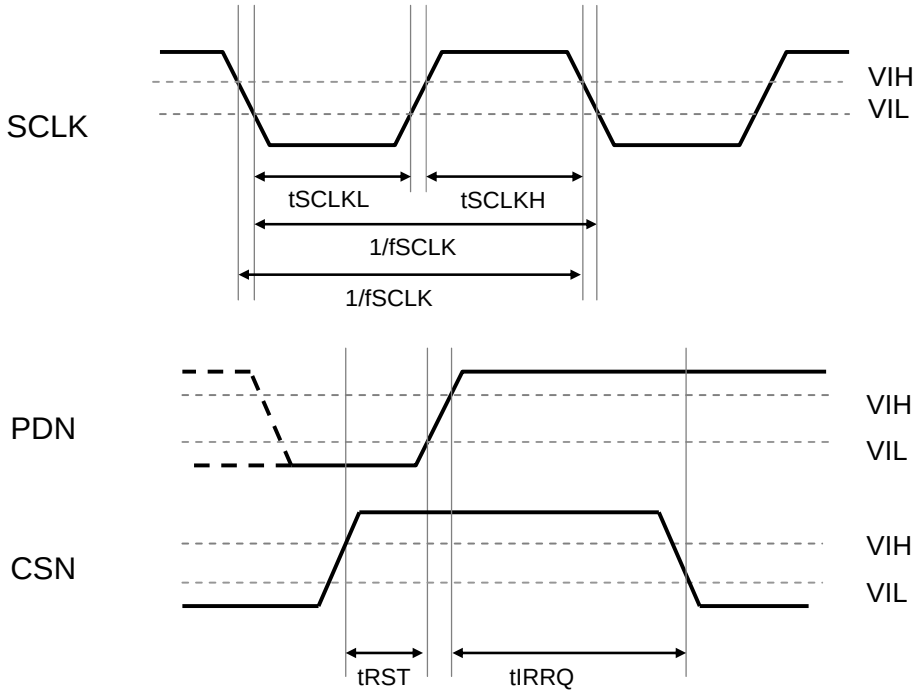


Figure 13. SPI Interface Timing 1

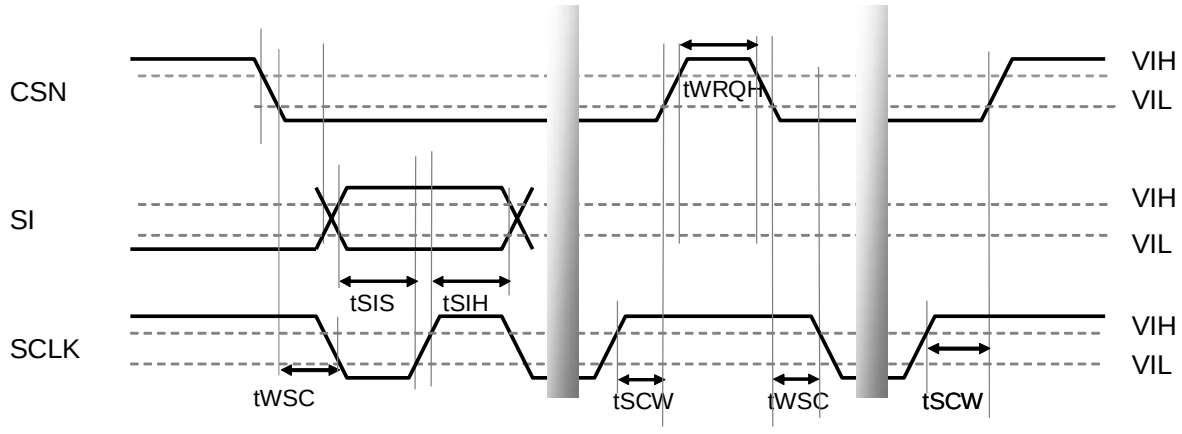


Figure 14. SPI Interface Timing 2 (Microcontroller → AK7758)

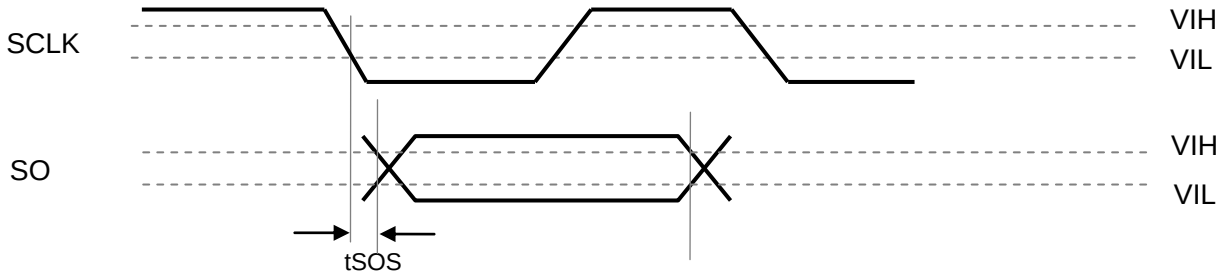


Figure 15. SPI Interface Timing 3 (AK7758 → Microcontroller)

8.5.5. I²C-BUS Interface

(Ta= -40~85°C; AVDD=LVDD=3.0~3.6V, TVDD1/2=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

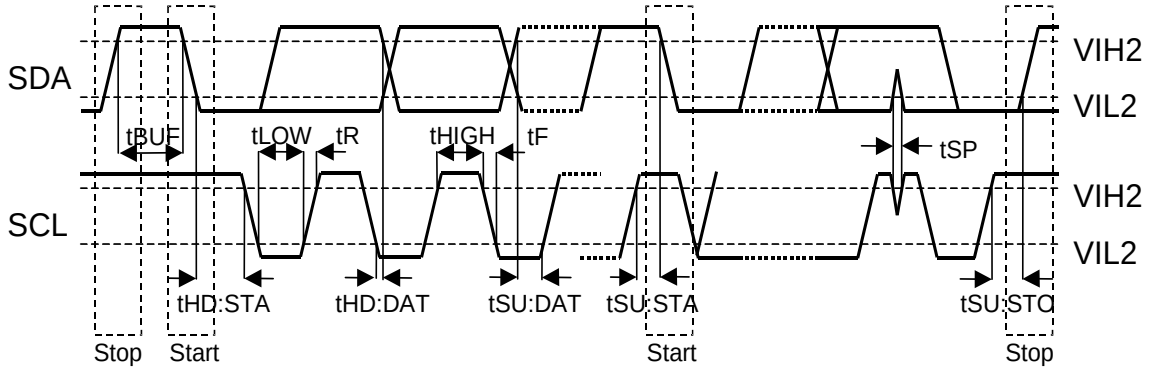


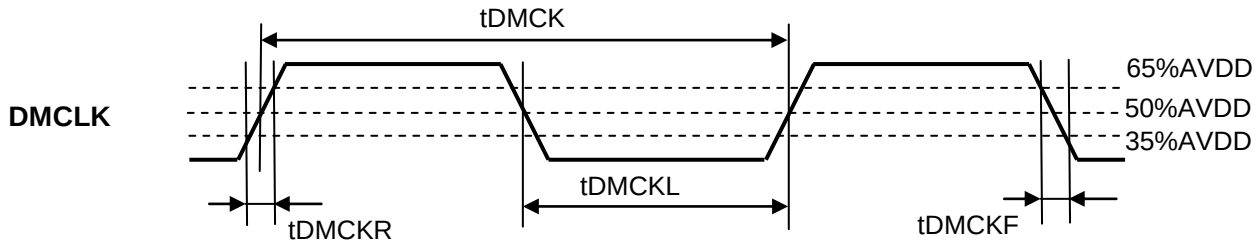
Figure 16. I²C BUS Interface Timing

8.5.6. Digital Microphone Interface

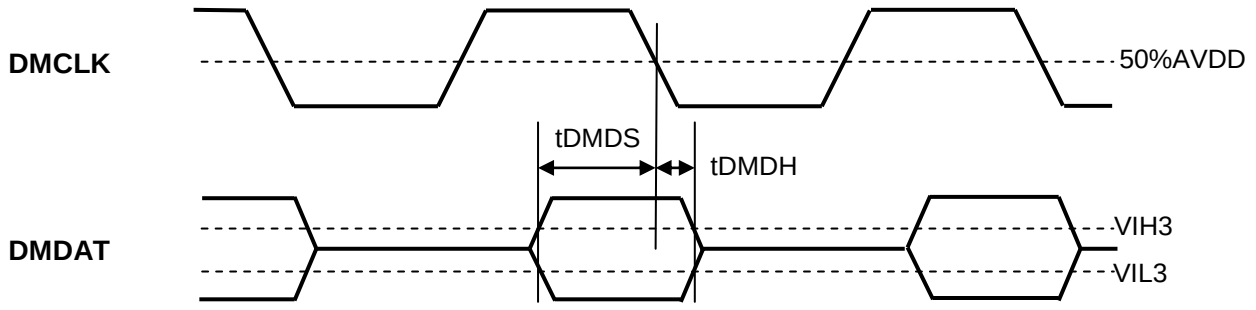
(Ta = -40°C~85°C, AVDD = LVDD = 3.0~3.6V, TVDD1/2 = 1.7~3.6V, DVDD = 1.14~1.3V, AVSS=DVSS= 0V; CL=100pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DMDAT					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK					
Clock Frequency (Note 52)	fDMCK	0.5	64fs	3.1	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise Time	tDMCKR			10	ns
Fall Time	tDMCKF			10	ns

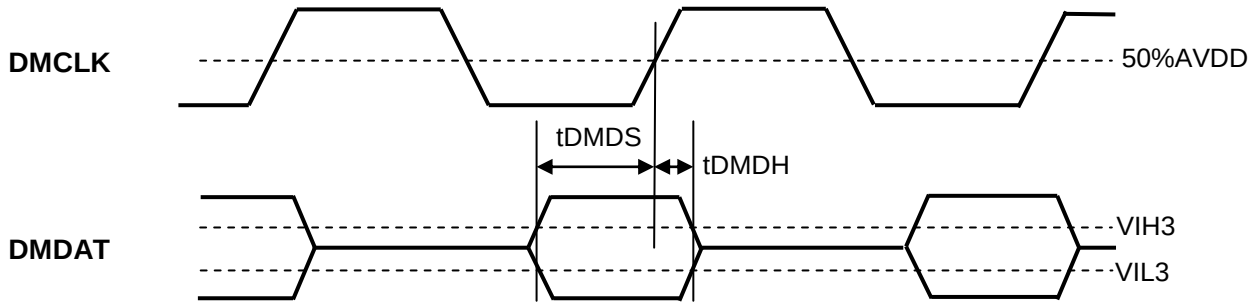
Note 52. Clock frequency is determined by the sampling rate (fs) selected by SDALL[2:0] bits.



fDMCK = 1 / tDMCK
dDMCK = 100 x tDMCKL / tDMCK



DMCLKP bit = “1”

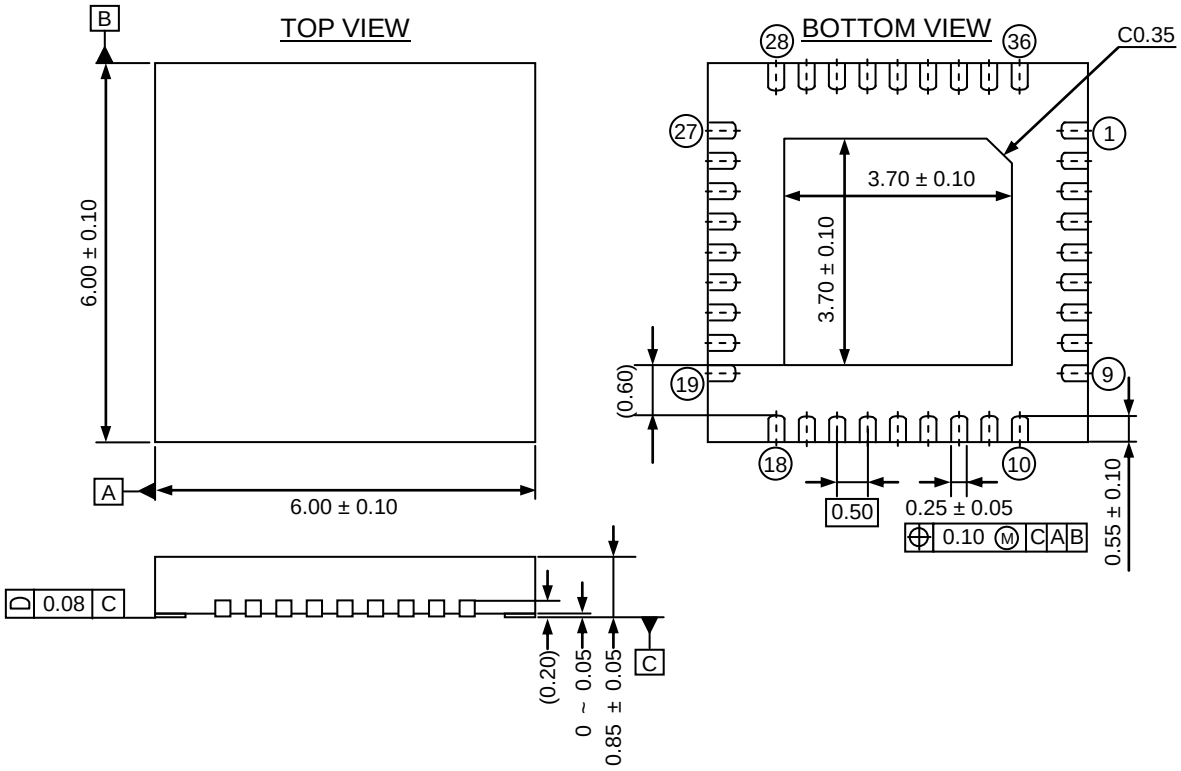


DMCLKP bit = “0”

Figure 17. Digital Microphone Interface Timing Wave Form

9. Pakcage

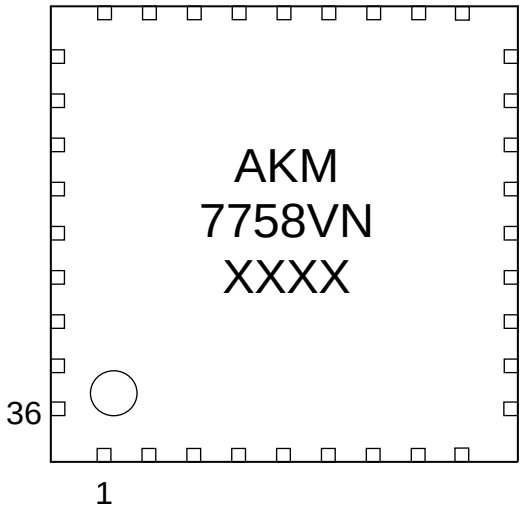
9.1. Outline Dimensions



9.2. Material and Lead Finish

Package: Epoxy
Lead frame: Copper
Pin surface treatment: Soldering (Pb free) plate

9.3. Marking



1) Pin #1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 7758VN
4) Asahi Kasei Logo

10. Ordaring Guide

AK7758VN	-40 ~ +85°C	36-pin QFN (0.5mm pitch)
AKD7758	Evaluation Board for AK7758	

11. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/03/22	00	First Edition		
16/04/22	01	Error Correction	9	5.2. Pin Function Description of LDOE: LDO Select Pin was corrected. "H (TVDD)" → "H (LVDD)"
			13	6. Absolute Maximum Ratings Description of Note 8 was corrected. (TVDD+0.3)V → (LVDD+0.3)V
		Description Addition	11	Relationship between Power Supplies and Digital Pins The SDOUT3/MAT1/JX3 pin was added to TVDD1.
			13	Note 10: The SDA pin was added to the description.
16/09/07	02	Error Correction	11	5.3. Handling of Unused Pin Digital: I2CSEL, CSN/CAD/MATSEL, LDOE and SI/EXTEEP pins were delated.
			12	5.5 Power-down and Power-down Release Pin Statuses The status of SO pin was corrected when PDN pin = "L" & LDOE pin = "L". "Hi-Z" → "Hi-Z"(@CSN = "H")

Date (Y/M/D)	Revision	Reason	Page	Contents
16/09/07	02	Error Correction	24	8.5.3. Serial Data Interface Description of Master Mode BICK Frequency “192fs” was deleted.
			26	8.5.4. SPI Interfase Description of “tWSC” was corrected. Time from RQN“↓” to SCLK“↓” → Time from CSN“↓” to SCLK“↓”

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.