**GENERAL DESCRIPTION**

The AKD4128A-A is an evaluation board for AK4128A, the digital sample rate converter. The AKD4128A-A has the digital audio interface and can achieve the interface with digital audio system via optical or coaxial connector.

**Ordering guide**

AKD4128A-A --- Evaluation board for AK4128A

(A cable for connecting with USB port of IBM-AT compatible PC a control software are packed with this.)

**FUNCTION**

- DIR/DIT with optical or coaxial input/output
- 10pin Header for AKM AD/DA evaluation board

![Diagram](image-url)

Figure 1. AKD4128A-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.
■ Operation sequence

1) Set up the power supply lines.

<table>
<thead>
<tr>
<th>Name of jack</th>
<th>Color of jack</th>
<th>Voltage</th>
<th>Used for</th>
<th>Open / Connect</th>
<th>Default Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>Orange</td>
<td>+5V</td>
<td>Regulator T1, T2, T3: AVDD and DVDD of AK4128A, AK4114, Digital Logic</td>
<td>Should be always connected when default setting.</td>
<td>+5V</td>
</tr>
<tr>
<td>AVDD</td>
<td>Red</td>
<td>+3.3V</td>
<td>AVDD of AK4128A</td>
<td>Should be always connected when AVDD of AK4128A is not supplied from regulator T1. In this case “JP1” is set to “AVDD” side.</td>
<td>Open</td>
</tr>
<tr>
<td>DVDD</td>
<td>Red</td>
<td>+3.3V</td>
<td>DVDD of AK4128A</td>
<td>Should be always connected when DVDD of AK4128A is not supplied from regulator T1. In this case “JP2” is set to “DVDD” side.</td>
<td>Open</td>
</tr>
<tr>
<td>D3.3V-1</td>
<td>Red</td>
<td>+3.3V</td>
<td>AK4114, Digital Logic</td>
<td>Should be always connected when AK4114 and Digital Logic is not supplied from regulator T2. In this case “JP3” is set to “D3.3V-1” side.</td>
<td>Open</td>
</tr>
<tr>
<td>D3.3V-2</td>
<td>Red</td>
<td>+3.3V</td>
<td>AK4114, Digital Logic</td>
<td>Should be always connected when AK4114 and Digital Logic is not supplied from regulator T3. In this case “JP4” is set to “D3.3V-2” side.</td>
<td>Open</td>
</tr>
<tr>
<td>GND</td>
<td>Black</td>
<td>0V</td>
<td>Ground</td>
<td>Should be always connected</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table 1. Set up the power supply lines

Each supply line should be distributed from the power supply unit.
2) Set up the jumper pin of power supply unit.

(1). Setup the AVDD of AK4128A.
   a). When using AVDD jack.
      b). When using Regulator.

(2). Setup the DVDD of AK4128A.
   a). When using DVDD jack.
      b). When using Regulator.

(3). Setup the D3.3V-1(AK4114 and Digital Logic).
   a). When using D3.3V-1 jack.
      b). When using Regulator.

(4). Setup the D3.3V-2(AK4114 and Digital Logic).
   a). When using D3.3V-2 jack.
      b). When using Regulator.
3) Set up the evaluation mode, jumper pins. (See the followings.)
   (1). Setting for Input port
       (1)-1. When using DIR function of AK4114 (U2, U3, U4 and U5)
       (1)-2. When using all clocks are fed through the 10pin port
   (2). Setting for Output port
       (2)-1. When using DIT function of AK4114 (U6)
       (2)-2. When using all clocks are fed through the 10pin port(PORT5).
   (3). Other jumper pins setup.

4) Power on.
   The AK4128A should be reset once bringing SW2 (PDN) “L” upon power-up.
Set up the evaluation mode, jumper pins.

(1). Setting for Input port

(1)-1. When using DIR function of AK4114 (U2, U3, U4 and U5)

When using J1-4(COAX) and PORT6-9(OPT), nothing should be connected to PORT1-4.

(1)-1-1. Setup the RX.

(a) Select to Optical jack (Default)

(b) Select to BNC jack

* "x" contains a number (1 - 4).

(1)-1-2. Setup the IBICK1-4, ILRCK1-4 and SDTI1-4.

When using J1-4(COAX) and PORT6-9(OPT), nothing should be connected to PORT1-4.

* "x" contains a number (1 - 4).
(1)-1-3. Setup the SDTI1, SDTI2, SDTI3 and SDTI4.

Select to input signal for SDTI1, SDTI2, SDTI3 and SDTI4 of AK4128A(U1).

(a). When using “Synchronous Mode” (INAS pin = “L”). (Default)

(b). When using “Asynchronous Mode” (INAS pin = “H”).

(c). Connect to GND.
(1)-2. When using all clocks are fed through the 10pin port

(1)-2-1. Setup the RX.

When using PORT1-4, nothing should be connected to J1-4 (COAX) and PORT6-9 (OPT).

(1)-2-2. Setup the IBICK1-4, ILRCK1-4 and SDTI1-4.

When using PORT1-4, nothing should be connected to J1-4 (COAX) and PORT6-9 (OPT).

```
JP27
IMCLK-SEL

EXT  IBICKx  ILRCKx  SDTIx
DSP1
DIR
```

* "x" contains a number (1 - 4).

(1)-2-3. Setup the SDTI1, SDTI2, SDTI3 and SDTI4.

Select to input signal for SDTI1, SDTI2, SDTI3 and SDTI4 of AK4128A(U1).

(a). When using “Synchronous Mode” (INAS pin = “L”). (Default)

```
JP5
SDTI1-SEL

Asynchronous  Synchronous  GND

JP6
SDTI2-SEL

Asynchronous  Synchronous  GND

JP7
SDTI3-SEL

Asynchronous  Synchronous  GND

JP8
SDTI4-SEL

Asynchronous  Synchronous  GND
```

(b). When using “Asynchronous Mode” (INAS pin = “H”).

```
JP5
SDTI1-SEL

Asynchronous  Synchronous  GND

JP6
SDTI2-SEL

Asynchronous  Synchronous  GND

JP7
SDTI3-SEL

Asynchronous  Synchronous  GND

JP8
SDTI4-SEL

Asynchronous  Synchronous  GND
```

(c). Connect to GND.

```
JP5
SDTI1-SEL

Asynchronous  Synchronous  GND

JP6
SDTI2-SEL

Asynchronous  Synchronous  GND

JP7
SDTI3-SEL

Asynchronous  Synchronous  GND

JP8
SDTI4-SEL

Asynchronous  Synchronous  GND
```
(2). Setting for Output port

(2)-1. When using DIT function of AK4114 (U6)

(2)-1-1. Setup the TX.

(a) Select to Optical jack (Default)

(b) Select to BNC jack

(2)-1-2. Setup the TXI.

Select to input signal for XTI/OMCLK pin of AK4128A(U1) and XTI pin of AK4114(U6).

(a) When using X’Tal(X1). In this case, X’Tal(X2) is “open”.

(b) When using X’Tal(X2). In this case, X’Tal(X1) is “open”.

(c) When using J8(EXT-CLK). In this case, X’Tal(X1 and X2) is “open”.

[AKD4128A-A]
(2)-1-3. Setup the OBICK, OLRCK and SDTO.

(2)-1-3-1. When using OBICK, OLRCK of AK4114(U6), and SDTO of AK4128A(U1).

(2)-1-3-2. When using OBICK, OLRCK and SDTO of AK4128A(U1).
(2)-1-4. Selection of SDTO1, SDTO2, SDTO3 and SDTO4.

(a) Select to SDTO1
(b) Select to SDTO2
(c) Select to SDTO3
(d) Select to SDTO4

(2)-2. When using all clocks are fed through the 10pin port(PORT5).

(2)-2-1. Setup TX.
As Optical connector:PORT10(OPT) and BNC connector:J5(COAX) are not used, please don’t connect anything.

(2)-2-2. Setup the OBICK, OLRCK and SDTO.

(2)-2-2-1. When using OBICK and OLRCK of 10pin port, and SDTO of AK4128A(U1).
(2)-2-2-2. When using OBICK, OLRCK and SDTO of AK4128A(U1).

(2)-2-2-3. Selection of SDTO1, SDTO2, SDTO3 and SDTO4.

(a) Select to SDTO1
(b) Select to SDTO2
(c) Select to SDTO3
(d) Select to SDTO4
(3). Other jumper pins setup.

[ JP9 (SEL1) ] : The selection of input signal to IMCLK pin.
  IMCLK : Connect to MCLK signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP10 (ILRCK2-SEL) ] : The selection of input signal to ILRCK2 pin.
  ILRCK2 : Connect to LRCK2 signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP11 (ILRCK3-SEL) ] : The selection of input signal to ILRCK3 pin.
  ILRCK3 : Connect to LRCK3 signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP12 (IBICK3-SEL) ] : The selection of input signal to IBICK3 pin.
  IBICK3 : Connect to BICK3 signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP13 (ILRCK4-SEL) ] : The selection of input signal to ILRCK4 pin.
  ILRCK4 : Connect to LRCK4 signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP14 (IBICK4-SEL) ] : The selection of input signal to IBICK4 pin.
  IBICK4 : Connect to BICK4 signal of DIR or 10 pin PORT. (Default)
  GND : Connect to GND

[ JP15 (SEL2) ] : The selection of input signal to INAS pin.
  INAS : Connect to INAS signal (Default)
  GND : Connect to GND

[ JP16 (UNLOCK) ] : The selection of connection to UNLOCK pin and LE1.
  OPEN : Unconnection.
  SHORT : Connection. (Default)

[ JP21 (TST0) ] : The selection of connection to TST0 pin and SW17(TST0).
  OPEN : Unconnection.
  SHORT : Connection. (Default)

[ JP22 (TST1) ] : The selection of connection to TST1 pin and SW3(TST1).
  OPEN : Unconnection.
  SHORT : Connection. (Default)

[ JP23 (TST2) ] : The selection of connection to TST2 pin and SW3(TST2).
  OPEN : Unconnection.
  SHORT : Connection. (Default)

[ JP24 (SEL4) ] : The selection of input signal to SDA pin.
  SDA : Connect to SDA signal of 10 pin PORT(PORT11). (Default)
  GND : Connect to GND

[ JP25 (TST3) ] : The selection of connection to TST3 pin and SW17(TST3).
  OPEN : Unconnection.
  SHORT : Connection. (Default)
  OPEN : J7(EXT-CLK) connector is use.
  SHORT : J7(EXT-CLK) connector is not use. (Default)
* If “JP31(EXT-CLK)” is set to “OPEN”, JP27 is set to “EXT”.
**Set up the DIP SW.**

(1). Setup the AK4128A(U1).

(1-1). SW3 setting

Upper-side is “H” and lower-side is “L”.

<table>
<thead>
<tr>
<th>SW3 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IDIF2</td>
<td>Audio Interface Format Setting for Input PORT</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>IDIF1</td>
<td>Refer to Table 3</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>IDIF0</td>
<td></td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SPB</td>
<td>Serial Control Mode</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>TST1</td>
<td>TEST Pin</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>TST2</td>
<td>Fixed to &quot;L&quot;</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>SMSEMI</td>
<td>Semi-auto Mode</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CAD0</td>
<td>Chip Address 0 bit=“1”</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. SW3 Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>IDIF2 pin</th>
<th>IDIF1 pin</th>
<th>IDIF0 pin</th>
<th>SDTI1-4 Format</th>
<th>IBICK Freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>16bit, LSB justified</td>
<td>( \geq 32\text{FSI} )</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>20bit, LSB justified</td>
<td>( \geq 40\text{FSI} )</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>24bit, MSB justified</td>
<td>( \geq 48\text{FSI} )</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>24/16bit, ( \text{I}^2\text{S} ) Compatible</td>
<td>( \geq 48\text{FSI or} \ 32\text{FSI} )</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>24bit, LSB justified</td>
<td>( \geq 48\text{FSI} )</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

Table 3. AK4128A Audio Interface Format Setting for Input PORT
(1)-2. SW3 setting

Upper-side is “H” and lower-side is “L”.

<table>
<thead>
<tr>
<th>SW4 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OBIT1</td>
<td>Output PORT Audio Interface Format Setting 2</td>
<td>Refer to Table 6</td>
<td>H</td>
</tr>
<tr>
<td>2</td>
<td>OBIT0</td>
<td></td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>TDM</td>
<td>TDM mode</td>
<td>Stereo mode</td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>CM2</td>
<td>Clock Select or Mode Select pin for Output PORT</td>
<td>Refer to Table 7</td>
<td>H</td>
</tr>
<tr>
<td>5</td>
<td>CM1</td>
<td></td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CM0</td>
<td></td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>ODIF1</td>
<td>Output PORT Audio Interface Format Setting 1</td>
<td>Refer to Table 5</td>
<td>H</td>
</tr>
<tr>
<td>8</td>
<td>ODIF0</td>
<td></td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

Table 4. SW4 Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>TDM pin</th>
<th>OBIT1 pin</th>
<th>OBIT0 pin</th>
<th>SDTO1-4 Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>LSB justified</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>H</td>
<td>(Reserved)</td>
<td>(Default)</td>
</tr>
<tr>
<td>2</td>
<td>H</td>
<td>L</td>
<td>MSB justified</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>H</td>
<td>H</td>
<td>I’S Compatible</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>L</td>
<td>L</td>
<td>(Reserved)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>H</td>
<td>TDM256 mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24bit MSB justified</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>TDM256 mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24bit I’S Compatible</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. Output PORT Audio Interface Format Setting 1

<table>
<thead>
<tr>
<th>Mode</th>
<th>TDM pin</th>
<th>Master / Slave setting</th>
<th>OBIT1 pin</th>
<th>OBIT0 pin</th>
<th>SDTO1-4</th>
<th>OLRCK</th>
<th>OBICK</th>
<th>OBICK Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Master (CM2-0 = “HLL” or “HHL”)</td>
<td>L</td>
<td>L</td>
<td>16bit</td>
<td>Input</td>
<td>Input</td>
<td>64FSO</td>
</tr>
<tr>
<td>0</td>
<td>L</td>
<td>Slave</td>
<td>L</td>
<td>L</td>
<td>16bit</td>
<td>Input</td>
<td>Input</td>
<td>≥ 32FSO</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>Slave</td>
<td>L</td>
<td>H</td>
<td>18bit</td>
<td>Input</td>
<td>Input</td>
<td>≥ 36FSO</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>Slave</td>
<td>H</td>
<td>L</td>
<td>20bit</td>
<td>Input</td>
<td>Input</td>
<td>≥ 40FSO</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>Slave</td>
<td>H</td>
<td>H</td>
<td>24bit</td>
<td>Input</td>
<td>Input</td>
<td>≥ 48FSO</td>
</tr>
<tr>
<td>4</td>
<td>L</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>L</td>
<td>L</td>
<td>16bit</td>
<td>Output</td>
<td>Output</td>
<td>64FSO</td>
</tr>
<tr>
<td>5</td>
<td>L</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>L</td>
<td>H</td>
<td>18bit</td>
<td>Output</td>
<td>Output</td>
<td>64FSO</td>
</tr>
<tr>
<td>6</td>
<td>L</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>H</td>
<td>L</td>
<td>20bit</td>
<td>Output</td>
<td>Output</td>
<td>64FSO</td>
</tr>
<tr>
<td>7</td>
<td>L</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>H</td>
<td>H</td>
<td>24bit</td>
<td>Output</td>
<td>Output</td>
<td>64FSO</td>
</tr>
<tr>
<td>8</td>
<td>H</td>
<td>Slave</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Input</td>
<td>Input</td>
<td>256FSO</td>
</tr>
<tr>
<td>9</td>
<td>H</td>
<td>Slave</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Output</td>
<td>Output</td>
<td>256FSO</td>
</tr>
<tr>
<td>10</td>
<td>H</td>
<td>Slave</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Input</td>
<td>Input</td>
<td>256FSO</td>
</tr>
<tr>
<td>11</td>
<td>H</td>
<td>Slave</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Output</td>
<td>Output</td>
<td>256FSO</td>
</tr>
<tr>
<td>12</td>
<td>H</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Input</td>
<td>Input</td>
<td>256FSO</td>
</tr>
<tr>
<td>13</td>
<td>H</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Output</td>
<td>Output</td>
<td>256FSO</td>
</tr>
<tr>
<td>14</td>
<td>H</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Input</td>
<td>Input</td>
<td>256FSO</td>
</tr>
<tr>
<td>15</td>
<td>H</td>
<td>Master (Not CM2-0 = “HLL” or “HHL”)</td>
<td>*</td>
<td>*</td>
<td>TDM256 mode 24bit</td>
<td>Output</td>
<td>Output</td>
<td>256FSO</td>
</tr>
</tbody>
</table>

Table 6. Output PORT Audio Interface Format Setting 2
Table 7. Output PORT Master/Slave/Bypass Mode Control Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>CM2 pin</th>
<th>CM1 pin</th>
<th>CM0 pin</th>
<th>Master / Slave</th>
<th>OMCLK/XTI Input</th>
<th>MCKO Output</th>
<th>FSO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Master</td>
<td>256FSO</td>
<td>256FSO</td>
<td>8k ~ 108kHz</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Master</td>
<td>384FSO</td>
<td>384FSO</td>
<td>8k ~ 96kHz</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Master</td>
<td>512FSO</td>
<td>512FSO</td>
<td>8k ~ 54kHz</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>Master</td>
<td>768FSO</td>
<td>768FSO</td>
<td>8k ~ 48kHz</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>Slave</td>
<td>In External Clock Mode, 1.024MHz~36.864MHz. In X’tal Mode, X’tal oscillation frequency.</td>
<td>OMCLK Input Clock</td>
<td>8k ~ 216kHz (Default)</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Master</td>
<td>128FSO</td>
<td>128FSO</td>
<td>8k ~ 216kHz</td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>Slave (Bypass)</td>
<td>Not used. (note)</td>
<td>IMCLK Input Clock</td>
<td>8k ~ 216kHz</td>
</tr>
<tr>
<td>7</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Master</td>
<td>128FSO</td>
<td>128FSO</td>
<td>8k ~ 216kHz</td>
</tr>
</tbody>
</table>

(1)-3. SW5 setting

Upper-side is “H” and lower-side is “L”.

Table 8. SW5 Setting

<table>
<thead>
<tr>
<th>SW4 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INAS</td>
<td>Asynchronous mode</td>
<td>Synchronous mode</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>DITHER</td>
<td>Dither ON</td>
<td>Dither OFF</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>SMT1</td>
<td>Soft Mute Timer Setting</td>
<td>Refer to Table 9</td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>SMT0</td>
<td>Refer to Table 9</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DEM0</td>
<td>De-emphasis Filter Setting</td>
<td>Refer to Table 10</td>
<td>H</td>
</tr>
<tr>
<td>6</td>
<td>DEM1</td>
<td>Refer to Table 10</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PM2</td>
<td>Channel Mode Setting</td>
<td>Refer to Table 11</td>
<td>H</td>
</tr>
<tr>
<td>8</td>
<td>PM1</td>
<td>Refer to Table 11</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

Table 9. Soft Mute Cycle Setting

<table>
<thead>
<tr>
<th>SMT1 pin</th>
<th>SMT0 pin</th>
<th>Period</th>
<th>FSO=48kHz</th>
<th>FSO=96kHz</th>
<th>FSO=192kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>1024/fso</td>
<td>21.3ms</td>
<td>10.7ms</td>
<td>5.3ms</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>2048/fso</td>
<td>42.7ms</td>
<td>21.3ms</td>
<td>10.7ms</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>4096/fso</td>
<td>85.3ms</td>
<td>42.7ms</td>
<td>21.3ms</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>8192/fso</td>
<td>170.7ms</td>
<td>85.3ms</td>
<td>42.7ms</td>
</tr>
</tbody>
</table>

Table 10. De-emphasis Filter Setting

<table>
<thead>
<tr>
<th>DEM1 pin</th>
<th>DEM0 pin</th>
<th>Mode (SDTI1-4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>44.1kHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>OFF</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>48kHz</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>32kHz</td>
</tr>
<tr>
<td>PM2 pin</td>
<td>PM1 pin</td>
<td>PDN pin</td>
</tr>
<tr>
<td>----------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

Table 11. Channel Mode Setting

(1)-4. SW17 setting

Upper-side is “H” and lower-side is “L”.

<table>
<thead>
<tr>
<th>SW17 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TST3</td>
<td>TEST Pin</td>
<td></td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>TST0</td>
<td>Fixed to ”L”</td>
<td></td>
<td>L</td>
</tr>
</tbody>
</table>

Table 12. SW17 Setting
(2). Setup the AK4114 (U2,U3,U4,U5,U6)

(2)-1. SW6(U2), SW7(U3), SW8(U4), SW9(U5) setting.

Upper-side is “H” and lower-side is “L”.

<table>
<thead>
<tr>
<th>SW6 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIR1-OCKS1</td>
<td>Master Clock Frequency Setting</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIR1-OCKS0</td>
<td>Refer to Table 16</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIR1-DIF0</td>
<td>24bit, I’S Compatible</td>
<td>24bit, Left justified</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 13. SW6 Setting

<table>
<thead>
<tr>
<th>SW7 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIR2-OCKS1</td>
<td>Master Clock Frequency Setting</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIR2-OCKS0</td>
<td>Refer to Table 16</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIR2-DIF0</td>
<td>24bit, I’S Compatible</td>
<td>24bit, Left justified</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 14. SW7 Setting

<table>
<thead>
<tr>
<th>SW8 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIR3-OCKS1</td>
<td>Master Clock Frequency Setting</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIR3-OCKS0</td>
<td>Refer to Table 16</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIR3-DIF0</td>
<td>24bit, I’S Compatible</td>
<td>24bit, Left justified</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 15. SW8 Setting

<table>
<thead>
<tr>
<th>SW9 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIR4-OCKS1</td>
<td>Master Clock Frequency Setting</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIR4-OCKS0</td>
<td>Refer to Table 16</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIR4-DIF0</td>
<td>24bit, I’S Compatible</td>
<td>24bit, Left justified</td>
<td>L</td>
</tr>
</tbody>
</table>

Table 16. SW9 Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>OCKS1 pin</th>
<th>OCKS0 pin</th>
<th>MCKO1</th>
<th>fs (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>H</td>
<td>256fs</td>
<td>96 kHz</td>
</tr>
<tr>
<td>2</td>
<td>H</td>
<td>L</td>
<td>512fs</td>
<td>48 kHz</td>
</tr>
<tr>
<td>3</td>
<td>H</td>
<td>H</td>
<td>128fs</td>
<td>192 kHz</td>
</tr>
</tbody>
</table>

Table 16. Master Clock Frequency Setting
(2)-2. **SW16(U6) setting.**

Upper-side is “H” and lower-side is “L”.

<table>
<thead>
<tr>
<th>SW16 No.</th>
<th>Name</th>
<th>ON (“H”)</th>
<th>OFF (“L”)</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIT-OCKS1</td>
<td>Master Clock Frequency Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DIT-OCKS0</td>
<td>Refer to Table 18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DIT-DIF2</td>
<td>Audio Interface Format Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DIT-DIF1</td>
<td>Refer to Table 19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DIT-DIF0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 17. SW16 Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>OCKS1 pin</th>
<th>OCKS0 pin</th>
<th>MCK01 fs (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>256fs 96 kHz</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>H</td>
<td>256fs 96 kHz</td>
</tr>
<tr>
<td>2</td>
<td>H</td>
<td>L</td>
<td>512fs 48 kHz</td>
</tr>
<tr>
<td>3</td>
<td>H</td>
<td>H</td>
<td>128fs 192 kHz</td>
</tr>
</tbody>
</table>

(Default)

Table 18. Master Clock Frequency Setting

<table>
<thead>
<tr>
<th>Mode</th>
<th>DIF2 pin</th>
<th>DIF1 pin</th>
<th>DIF0 pin</th>
<th>DAUX Format</th>
<th>LRCK</th>
<th>BICK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>24bit, I’S Compatible</td>
<td>L/H</td>
<td>O</td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>24bit, Left justified</td>
<td>H/L</td>
<td>O</td>
</tr>
<tr>
<td>7</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>24bit, I’S Compatible</td>
<td>L/H</td>
<td>O</td>
</tr>
</tbody>
</table>

(Default)

Table 19. Audio Interface format Setting
The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (AK4128-SMUTE) : Soft mute of AK4128A.
   When using Soft mute function, SW1 is “H”.

[SW2] (AK4128-PDN) : Resets the AK4128A. Keep “H” during normal operation.
   The AK4128A should be resets once bringing “L” upon power-up.

[SW10] (DIR1-PDN) : Resets the AK4114 (U2). Keep “H” during normal operation.
   The AK4114 (U2) should be resets once bringing “L” upon power-up.
   Keep “L” when AK4114 (U2) is not used.

[SW11] (DIR2-PDN) : Resets the AK4114 (U3). Keep “H” during normal operation.
   The AK4114 (U3) should be resets once bringing “L” upon power-up.
   Keep “L” when AK4114 (U3) is not used.

[SW12] (DIR3-PDN) : Resets the AK4114 (U4). Keep “H” during normal operation.
   The AK4114 (U4) should be resets once bringing “L” upon power-up.
   Keep “L” when AK4114 (U4) is not used.

[SW13] (DIR4-PDN) : Resets the AK4114 (U5). Keep “H” during normal operation.
   The AK4114 (U5) should be resets once bringing “L” upon power-up.
   Keep “L” when AK4114 (U5) is not used.

[SW14] (DIT-PDN) : Resets the AK4114 (U6). Keep “H” during normal operation.
   The AK4114 (U6) should be resets once bringing “L” upon power-up.
   Keep “L” when AK4114 (U6) is not used.

Indication for LED

[LE1] (UNLOCK) : Monitor UNLOCK pin of the AK4128A (U1).
   LED turns on when PDN pin = “L”. 
## Serial Control

The AKDUSBIF-B is connected to a PC with a USB cable and to an evaluation board with the 10pin flat cable installed in the AKDUSBIF-B (Note 1, Note 2).

Note 1. Only one AKDUSBIF-B can be connected to a PC. It cannot operate when connecting more than two AKDUSBIF-B’s.

Note 2. The red line of the 10pin flat cable should be connected with the 1pin of the 10pin Header of an evaluation board.

![Connection via the AKDUSBIF-B](image1.png)

**Figure 2. Connection via the AKDUSBIF-B**

![AKDUSBIF-B](image2.png)

**Figure 3. AKDUSBIF-B**
Control Soft Manual

**Evaluation Board and Control Soft Settings**

1. Set an evaluation board properly.
2. Connect a USB control box (AKUSBIF-B) and an evaluation board.
   - Pay attention about direction of the 10pin header when connecting to an AKUSBIF-B.
3. Connect a PC (IBM-AT compatible) and the USB control box (AKUSBIF-B).
   - The USB control box is recognized as HID (Human Interface Device) on the PC.
   - It is not necessary to install a new driver.
4. Start up the control program.
   - When the screen does not display “AKUSBIF-B” at bottom left, reconnect the PC and the USB control box, and push the [Port Reset] button.
5. Proceed evaluation by following the process below.

[Support OS]

Windows XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
64bit OS’s are not supported.
Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “Dialog Boxes” for details of each dialog box setting.

1. **Port Reset**: For when connecting to USB I/F board (AKDUSBIF-B)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-B).
2. **Write Default**: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.
3. **All Write**: Executing write commands for all registers displayed.
4. **All Read**: Executing read commands for all registers displayed.
5. **Save**: Saving current register settings to a file.
6. **Load**: Executing data write from a saved file.
7. **All Req Write**: “All Req Write” dialog box is popped up.
8. **Data R/W**: “Data R/W” dialog box is popped up.
9. **Sequence**: “Sequence” dialog box is popped up.
10. **Sequence(File)**: “Sequence(File)” dialog box is popped up.
11. **Read**: Reading current register settings and display on to the Register area (on the right of the main window).
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

Figure 4. Window of [FUNCTION]
Dialog Boxes

[All Req Write]

Click [All Reg Write] button in the main window to open register setting files. Register setting files saved by [SAVE] button can be applied.

![Figure 5. Window of [All Reg Write]](image)

- **Open (left)**: Selecting a register setting file (*.akr).
- **Write**: Executing register writing.
- **Write All**: Executing all register writings. Writings are executed in descending order.
- **Help**: Help window is popped up.
- **Save**: Saving the register setting file assignment. The file name is “*.mar”.
- **Open (right)**: Opening a saved register setting file assignment “*.mar”.
- **Close**: Closing the dialog box and finish the process.

*Operating Suggestions*

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.
[Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box. Data write is available to specified address.

Figure 6. Window of [Data R/W]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write] : Writing to the address specified by “Address” box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.
[Sequence]

Click [Sequence] button to open register sequence setting dialog box. Register sequence can be set in this dialog box.

Sequence Setting
Set register sequence by following process bellow.
(1) Select a command
Use [Select] pull-down to choose commands. Corresponding boxes will be valid.

< Select Pull-down menu >
- No_use : Not using this address
- Register : Register writing
- Reg(Mask) : Register writing (Masked)
- Interval : Taking an interval
- Stop : Pausing the sequence
- End : Finishing the sequence

(2) Input sequence
[Address] : Data address
[Data] : Writing data
[Mask] : Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[ Interval ] : Interval time
Valid boxes for each process command are shown bellow.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

Control Buttons

The function of Control Button is shown bellow.

- [Start] : Executing the sequence
- [Help] : Opening a help window
- [Save] : Saving sequence settings as a file. The file name is “*.aks”.
- [Open] : Opening a sequence setting file “*.aks”.
- [Close] : Closing the dialog box and finish the process.

Stop of the sequence

When “Stop” is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the “Start Step” box. When finishing the process until the end of sequence, “Start Step” will return to “1”.

The sequence can be started from any step by writing the step number to the “Start Step” box. Write “1” to the “Start Step” box and click [Start] button, when restarting the process from the beginning.
[Sequence(File)]

Click [Sequence(File)] button to open sequence setting file dialog box. Those files saved in the “Sequence setting dialog” can be applied in this dialog.

![Sequence by *.aks File](image)

**Figure 8. Window of [Sequence(File)]**

- **[Open (left)]**: Opening a sequence setting file (*.aks).
- **[Start]**: Executing the sequence setting.
- **[Start All]**: Executing all sequence settings. Sequences are executed in descending order.
- **[Help]**: Pop up the help window.
- **[Save]**: Saving sequence setting file assignment. The file name is “*.mas”.
- **[Open(right)]**: Opening a saved sequence setting file assignment “*.mas”.
- **[Close]**: Closing the dialog box and finish the process.

*Operating Suggestions*

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” is selected in the sequence the process will be paused and a pop-up message will appear. Click “OK” to continue the process.

![Sequence Pause](image)

**Figure 9. Window of [Sequence Pause]**
1. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

Figure 10. Window of [ REG]
**[Write]: Data Writing Dialog**

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or “0”. Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

![Register Set Window](image)

*Figure 11. Window of [ Register Set ]*

**[Read]: Data Read**

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.
2.[Tool]: Testing Tools

This tab screen is for evaluation testing tool. Click buttons for each testing tool.

Figure 12. Window of [Tool]
[Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

![Figure 13. Window of [ Repeat Test]](image)

[Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

![Figure 14. Window of [ Loop]](image)
## Measurement Results

### Measurement condition
- **Measurement unit**: Audio Precision, System Two Cascade
- **Power Supply**: AVDD=DVDD=3.3V
- **Band width**: 20Hz ~ FSO/2
- **INAS pin**: “L” (Synchronous Mode)
- **OMCLK/XTI Input**: Use X’Tal (X1)
- **Output PORT**: Slave Mode
- **Temperature**: Room

### Measurement Result

<table>
<thead>
<tr>
<th>SRC Characteristics</th>
<th>SDTO1</th>
<th>SDTO2</th>
<th>SDTO3</th>
<th>SDTO4</th>
<th>Unit</th>
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<tbody>
<tr>
<td></td>
<td>Lch</td>
<td>Rch</td>
<td>Lch</td>
<td>Rch</td>
<td>Lch</td>
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<td><strong>THD+N</strong></td>
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<tr>
<td>(Input = 1kHz, 0dBFS)</td>
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<tr>
<td>FSO/FSI = 44.1kHz/48kHz</td>
<td>130.4</td>
<td>130.4</td>
<td>130.3</td>
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<tr>
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<tr>
<td>FSO/FSI = 192kHz/48kHz</td>
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<td>Worst Case (FSO/FSI = 32kHz/176.4kHz)</td>
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<td>130.3</td>
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<td><strong>Dynamic Range</strong></td>
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<tr>
<td>(Input = 1kHz, −60dBFS)</td>
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<td>FSO/FSI = 44.1kHz/48kHz</td>
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<tr>
<td>FSO/FSI = 48kHz/44.1kHz</td>
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<tr>
<td>FSO/FSI = 192kHz/48kHz</td>
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<td>132.6</td>
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<td>Worst Case(FSO/FSI = 48kHz/32kHz)</td>
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<td><strong>Dynamic Range</strong></td>
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AKM

AK4128A FFT
AVDD=DVDD=3.3V, FSO/FSI=44.1kHz/48kHz, 1kHz/0dBFS Input

Figure 15. FFT Plot (Input = 0dBFS)

AKM

AK4128A FFT
AVDD=DVDD=3.3V, FSO/FSI=44.1kHz/48kHz, 1kHz/-60dBFS Input

Figure 16. FFT Plot (Input = -60dBFS)
Figure 17. THD+N vs. Input Level

Figure 18. THD+N vs. Input Frequency (Input = 0dBFS)
Figure 19. THD+N vs. Input Frequency (Input = -60dBFS)

Figure 20. Linearity
AKM

AK4128A Frequency Response (Yellow: FSI=44.1kHz, Blue: FSI=48kHz, Red: FSI=96kHz, Green: FSI=192kHz)
AVDD=DVDD=3.3V, FSO=44.1kHz, 0dBFS Input

Figure 21. Frequency Response (FSO=44.1kHz)

AKM

AK4128A Frequency Response (Blue: FSI=48kHz, Red: FSI=96kHz, Green: FSI=192kHz)
AVDD=DVDD=3.3V, FSO=48kHz, 0dBFS Input

Figure 22. Frequency Response (FSO=48kHz)
### Revision History

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<thead>
<tr>
<th>Date (YY/MM/DD)</th>
<th>Manual Revision</th>
<th>Board Revision</th>
<th>Reason</th>
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<td>10/08/24</td>
<td>KM104300</td>
<td>0</td>
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<td>10/09/30</td>
<td>KM104301</td>
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<td>Addition</td>
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<td>22-32</td>
<td>“Control Soft Manual” was changed.</td>
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AKD4128A-A Rev.0 Evaluation Board