AK9242/43
Reference Design

This document shows circuit and layout diagrams of the AK9242/43 as the reference design.

■ Circuit Diagram
It shows compositions of power supply decoupling capacitors.

Peripheral Parts/Pattern Details
C7,C8 : Decoupling Capacitor for VDD
C9,C10 : Decoupling Capacitor for DRVDD
C11,C12: Decoupling Capacitor for VREFP-VREFN
C13 : Decoupling Capacitor for LDO0
C14 : Decoupling Capacitor for LDO1

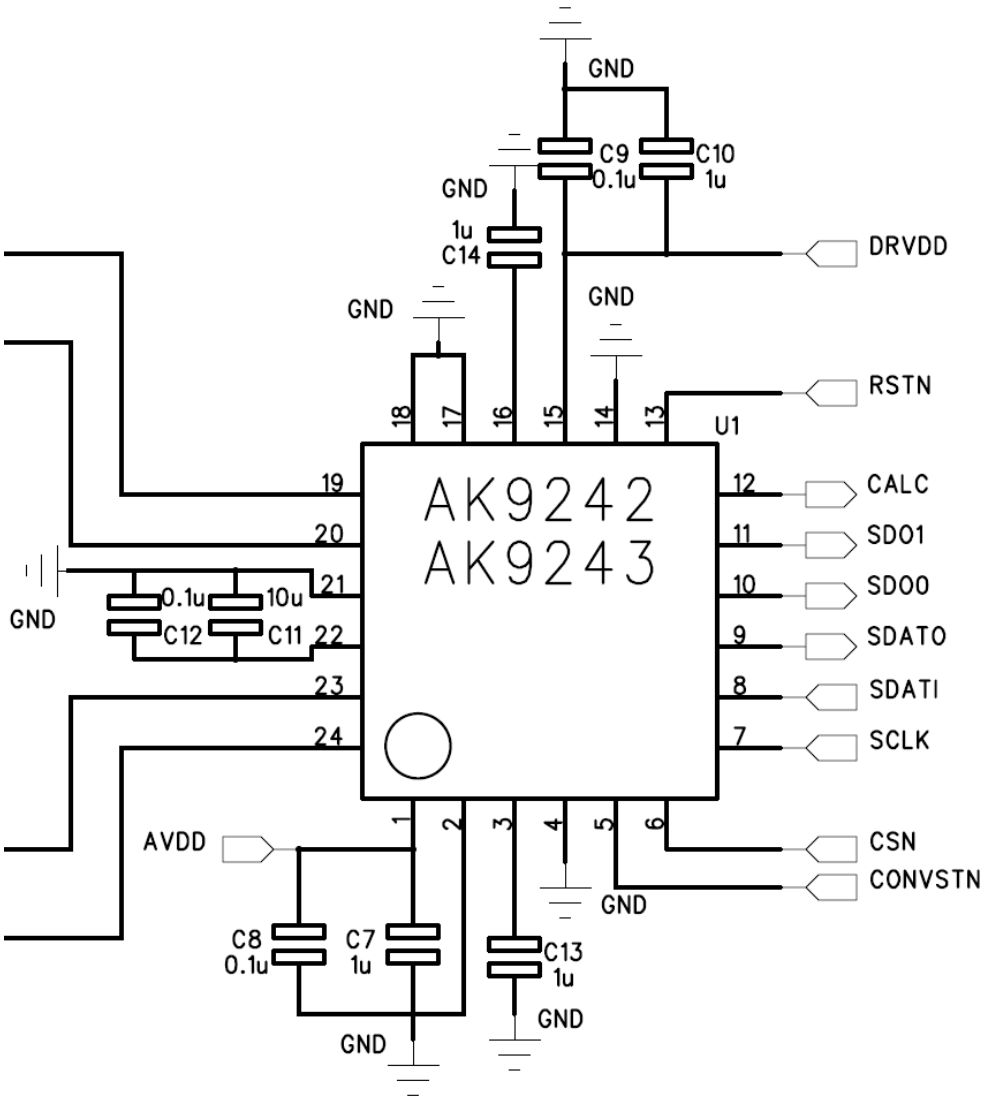

Figure 1 Circuit Diagram

■ **Layout**

Four layered printing board is used. The second layer is for the ground and the third layer is for power supply. VDD and DRVDD are separated on the power supply layer.
All areas except parts and wirings are GND in the first and the fourth layers.
All used chip parts here are located as 1005 (1.0mm x 0.5mm) size layout.

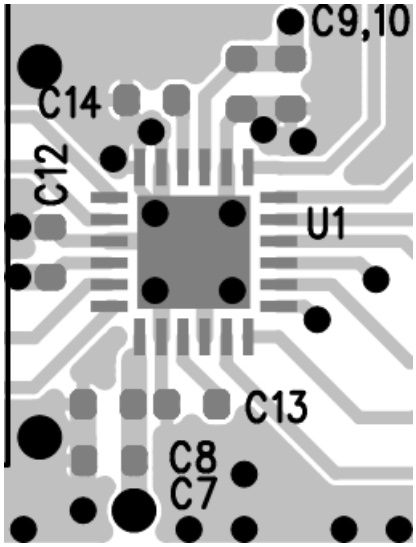

Figure 2 First Layer Layout

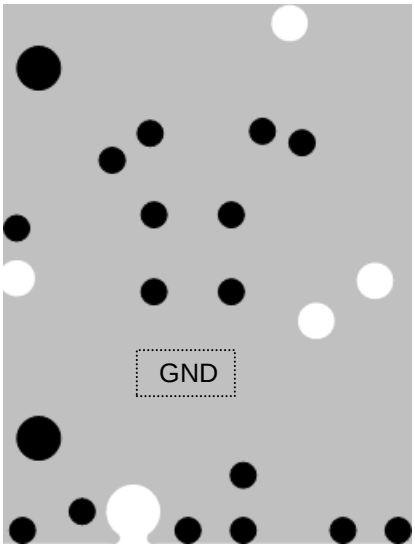

Figure 3 Second Layer Layout

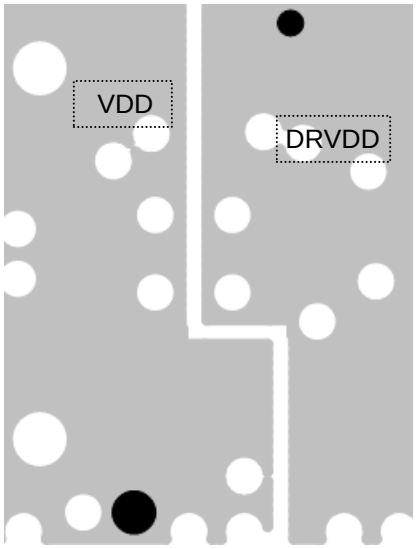

Figure 4 Third Layer Layout

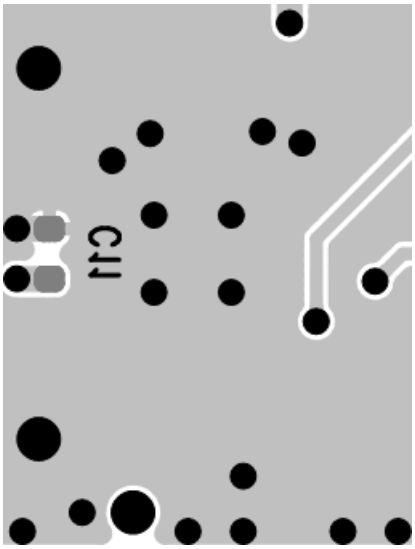

Figure 5 Fourth Layer Layout (Reverse Side)

Disclaimer

Please note that this document is written for reference only and it does not guarantee any information written in this document. Asahi Kasei Microdevices Corporations assumes no responsibility for any damages or losses resulting from the use of this document.

Inquiry

For any inquiries about this application note, please contact us from the link below.

<http://www.akm.com/akm/en/support/inquires>